6. INTERFACE UNITS

6.1 AIU ATM Interface Unit

6.1.1 General

AIU, ATM Interface Unit offers a partially filled STM-1 (155 Mbit/s) ATM customer interface to the Ericsson DXX-system. AIU helps DXX system to provide a managed ATM transport service for customers who need to access ATM backbone services with a low to moderate capacity (64 kbit/s- 16 Mbit/s) via a standard STM-1 interface.

AIU essentially offers the operator the low speed ATM access loop. AIU offers more than just backhauling cells from CPE to backbone interface because AIU provides a standard 155 Mbit/s interface and cell processing capability at the DXX network interface.

The ATM multiplexing feature will be needed at the backbone interface to aggregate several low speed AIU access loops to a single high speed backbone interface. The multiplexer feature is also provided by the AIU modules.

The notation AIU N:M with N for number of the ATM access interfaces and M for the number of the ATM virtual trunk interfaces is used throughout the document. AIU 1:1 and AIU 1:4 are currently supported.

The DXX integrated access concept is maintained at the transmission and management level. ATM access is integrated with TDM access by multiplexing at the transmission media layer.

AIU 1:1 offers a single ATM virtual trunk for the ATM access interface. The functionality of a flexible capacity ATM transport pipe through DXX network is available. The AIU 1:1 version can be used to implement a single ATM access loop between the ATM equipment in customer premises and the ATM service node.

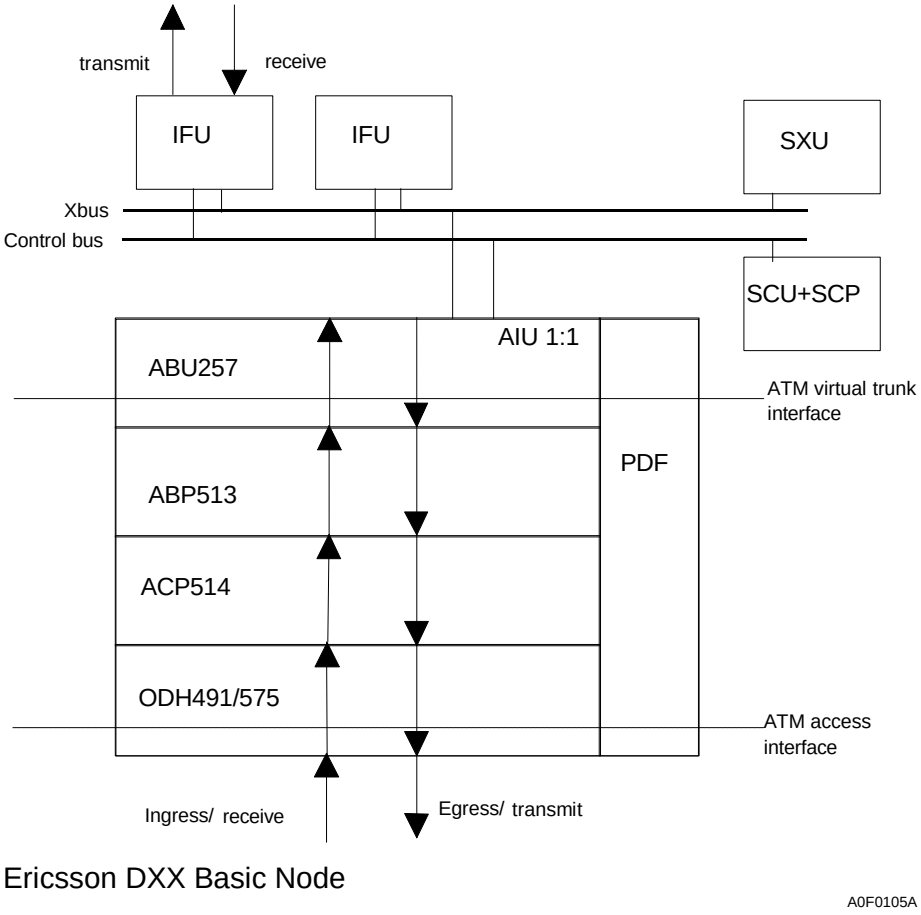


Fig. 1: AIU 1:1 Block Diagram

AIU 1:1 consists of

- STM-1-IO-13 or STM-1-IO-13S Optical STM-1 ATM Access Interface module
- ACP514 ATM Cell Processing module
- ABP513 Cell Switching and Buffering Block
- ABU257 ATM Base Unit
- PDF520 12, 5 and 3.3 Volt power supply module

AIU 1:4 offers four ATM virtual trunks for the ATM access interface. The functionality of an ATM access multiplexer is available with this AIU version. ATM-multiplexing feature is needed at the backbone interface to aggregate several low speed AIU access loops to a single high speed backbone interface.

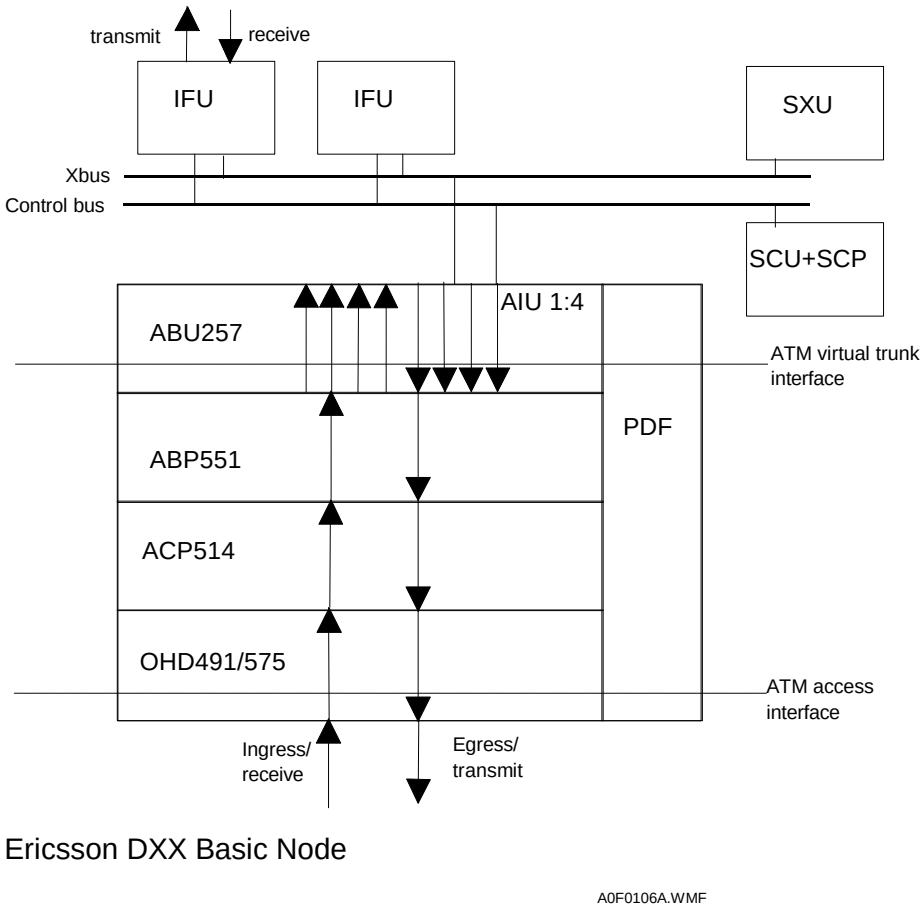


Fig. 2: AIU 1:4 Block Diagram

AIU 1:4 consists of

- STM-1-IO-13S or STM-1-IO-13 ATM Access Interface module
- ACP514 ATM Cell Processing module
- ABP551 Cell multiplexer and buffering module which completely replaces the ABP513
- ABU257 ATM Base Unit
- PDF520 12, 5 and 3.3 Volt power supply module

AIU 1:4 can be used as an access multiplexer to aggregate low speed ATM access loops to a single ATM service node interface as depicted in figure. In this application AIU 1:1 serves as customer service access ports and AIU 1:4 serves as the access multiplexer.

Fig. 3 represents an ATM access network (AN) with three AIU 1:1 and one AIU 1:4.

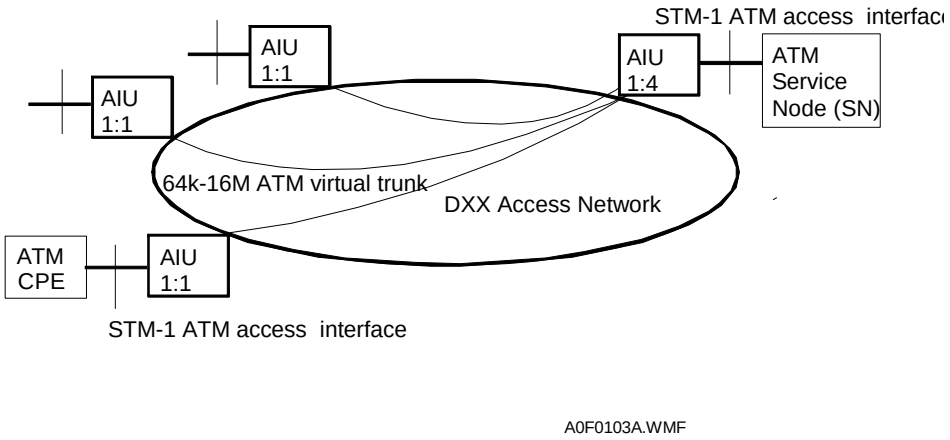


Fig. 3: AIU network configuration

The customer accesses network via the AIU ATM access interface which is NNI- or UNI-like interface. AIU adapts cells on VPI basis from ATM access interface to a single DXX ATM Virtual Trunk at ATM virtual trunk interface.

The service node accesses transport network via the AIU 1:4 ATM access interface which is NNI- or UNI-like interface. AIU 1:4 adapts cells on VPI basis from ATM access interface to 1 to 4 ATM virtual trunks at ATM virtual trunk interface. From the ATM service node point of view each customer ATM access interface is represented as a “virtual UNI” with a unique set of VPIs. Need to have separate physical UNIs at SN is eliminated.

The DXX access network maps the user VPIs to a set of VPIs at the service node interface. A single user VPI is associated with only one VPI at service node interface.

A network of AIU 1:4s can be used to realize an ATM leased line enterprise network. This application is depicted in the figure below. A fully meshed 64 k-16 Mbit/s ATM virtual trunk network supports maximum of five sites’ ATM equipment.

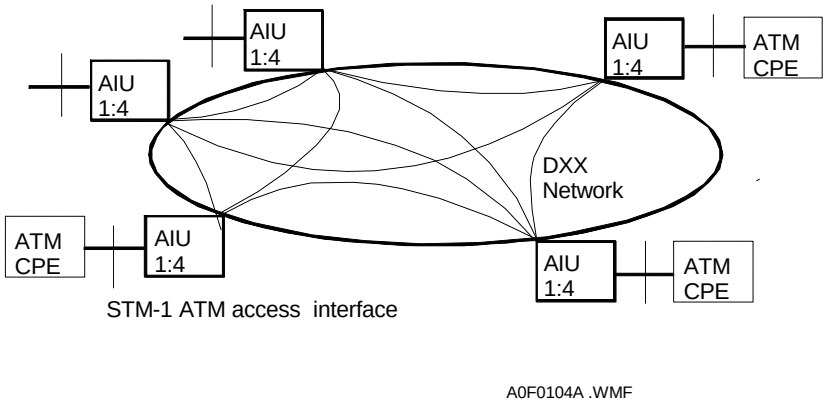


Fig. 4: An ATM leased line enterprise network

6.1.1.1 Unit List

Unit/Module ID	Product ID	Description	Equipping	Width
AIU	AIU1:1	ATM Interface Unit 1:1	1...8 / node	10T
	ABU257	ATM Base Unit	1/AIU	
	ACP514	ATM Cell Processing module	1/AIU	
ABP1:1	ABP513	1:1 multiplexer and buffer module	1/AIU	
	ABZ531	ABU257 sw product	1/AIU	
	ACZ7000	ACP514 application sw	1/AIU	
	ACZ7001	ACP514 boot sw	1/AIU	
[a]	[a]	ATM Access Interface module	1/AIU	
	PDF520	Unit 3V/5V/12V power supply module, -48V	1/AIU	
AIU	AIU1:4	ATM Interface Unit 1:4	1...8/node	10T
	ABU257	ATM Base Unit	1/AIU	
	ACP514	ATM Cell Processing module	1/AIU	
ABP1:4	ABP551	1:4 multiplexer and buffer module	1/AIU	
	ABZ531	ABU257 sw product	1/AIU	
	ACZ7000	ACP514 application sw	1/AIU	
	ACZ7001	ACP514 boot sw	1/AIU	
[a]	[a]	ATM Access Interface module	1/AIU	
	PDF520	Unit 3V/5V/12V power supply module, -48V	1/AIU	
STM-1-IO-13	ODH491	Optical intraoffice multimode 1.3 um STM-1 interface	1/AIU	
STM-1-IO-13S	ODH575	Optical intraoffice single mode 1.3 um STM-1 interface	1/AIU	
UTP-5	EDH390	Electrical UTP-5 STM-1 interface	1/AIU	

a ATM Access Interface modules

6.1.2 Operation of AIU ATM Interface Unit

6.1.2.1 AIU Mechanical Structure

The mechanical design of the AIU is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; the general recommendations for subrack equipping should, however, be followed.

The minimum configuration of the AIU unit consists of ATM base unit ABU257 with program memory ABZ 531, ATM buffer piggyback ABP513 or ABP551, ATM cell processor ACP514, unit power supply PDF 520 and ATM access interface modules STM-1-IO-13, STM-1-IO-13S or UTP-5.

The unit front panel houses two alarm LEDs. The front panel openings are suited for available interface modules.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the ABU card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for data transmission processing.

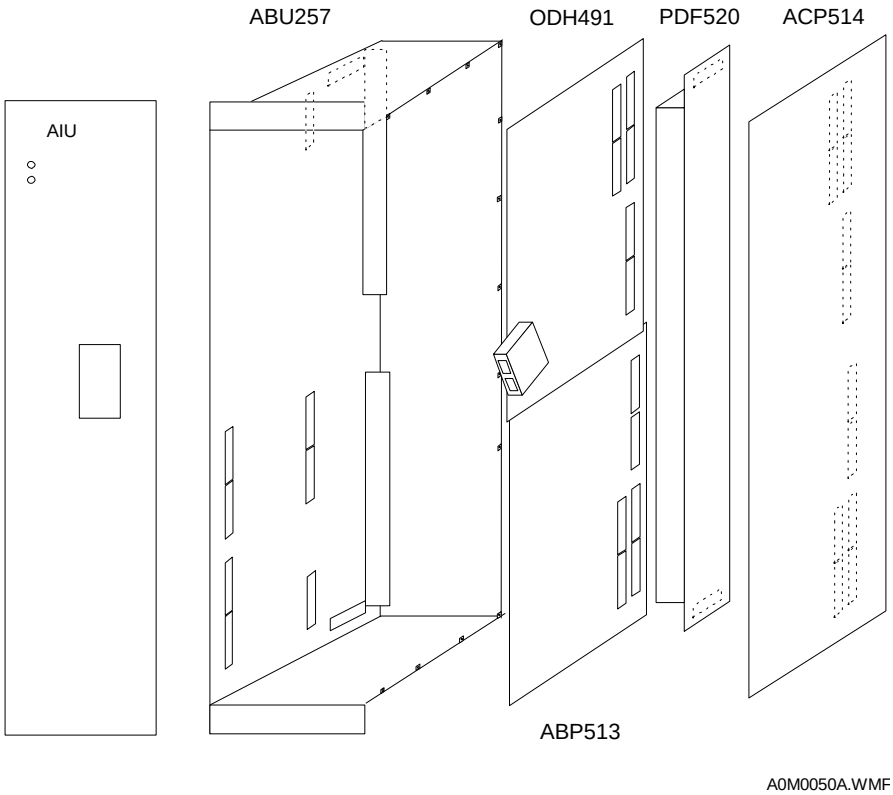


Fig. 5: Mechanical Structure of AIU ATM Interface Unit

AIU Functional Structure

The processors on ABU257 and ACP514 with their peripheral circuits control and monitor the functions of the unit. Control and monitoring information between the two processors is passed via a dual port memory. Information related to unit control and monitoring is transmitted on an internal VTP control bus of the subrack. Through this control bus the AIU can communicate with other units in the subrack as any DXX unit currently available.

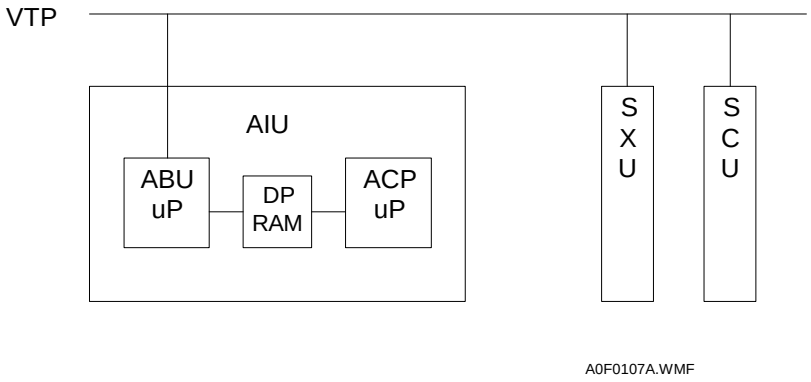


Fig. 6: Subrack Internal VTP Control Bus

AIU modules ODH, ABP and ACP are controlled by the ATM processor of the ACP module. The ATM processor runs ACZ7000 boot SW and ACZ7001 application SW packages.

SW package ABZ531 running on the ABU257 DXX-processor takes care of DXX general functions of the AIU unit including communication with other DXX-units and NMS. It supports configuration setting backup, fault information collection, application SW download and NMS message passing for the ATM processor.

AIU 1:1 and AIU 1:4 both support the same basic function: adapting cells from a partially filled STM-1 ATM access interface to a DXX circuit which is called ATM virtual trunk and at the other end of the trunk extracting cells from the ATM virtual trunk to the ATM access interface.

AIU 1:1 supports one ATM access interface and a single ATM virtual trunk of 64 k-16 Mbit/s capacity.

AIU 1:4 supports one ATM access interface and one to four ATM virtual trunks of 64 k-16 Mbit/s capacity with an aggregate throughput capacity of 16 Mbit/s.

AIU can be installed to interface unit slots of a DXX Basic Node, Cluster Node and Midi Node. AIU operation requires the configuration of the ATM access interface and ATM virtual trunk operational parameters and setup of VP-level connections over an AIU pair.

Proper operation requires the attached ATM equipment to control the aggregate cell rate sent to the AIU ATM access interface in proportion to the limits set by the configured ATM virtual trunk capacity. This can be accomplished by strict per VP peak cell rate control or by traffic shaping at the ATM level. Bursting in cells at full STM-1 capacity would cause AIU buffers to overflow and cells to be lost.

While in operational state AIU maintains cell transfer performance related data, informs about faults, and allows cell based OAM functions to be run.

6.1.2.2 AIU capacity

Type	AIU 1:1	AIU 1:4
Max. Throughput	16 Mbit/s	16 Mbit/s
Max. AVT Throughput	16 Mbit/s	16 Mbit/s
Max. No of AVTs	1	4
Max. No of VPCs	60	60
Max RX Cell buffers /ATM virtual trunk:	2000 cells	2000 cells

6.1.2.3 ATM virtual trunk interface

The DXX TDM p-p circuit between two AIUs reserved for ATM traffic is called an ATM virtual trunk. An ATM virtual trunk interface is the AIU DXX X-bus interface created by ABU257 Xbus interface circuitry and AIU ABP-modules.

The ATM virtual trunk capacity is available as AIU Xbus interface timeslot bytes to which ATM cells are mapped to and extracted from. A flexible number of timeslot bytes can be allocated for the ATM virtual trunk.

The number of ATM virtual trunks supported in the AIU depends on the type of the ABP-module. ABP513 supports one ATM virtual trunk and ABP551 supports four ATM virtual trunks.

Maximum throughput of the AIU is 16 Mbit/s. Maximum capacity of an individual ATM virtual trunk is 16 Mbit/s. If AIU1:4 is configured to have four ATM virtual trunks, the recommended maximum virtual trunk capacity is 4 Mbit/s.

Receive/ingress processing has the following features per each ATM virtual trunk:

— cells received from the ATM cell processor interface are buffered in SRAM according to their ATM virtual trunk identifier
— HEC byte is generated from header bytes and appended to cell header before sending to X-bus interface
— cell rate decoupling is performed via idle cell insertion
— specified XBI ASIC ports and timeslots are serviced with steady and uninterrupted flow of ATM cell bytes

The following features are optional and can be chosen by the NMS per each ATM virtual trunk:

— HEC scrambling with the coset (55_h)
— payload scrambling with $x^{43}+1$ self synchronising scrambler (ABP513 only)

Transmit/ egress cell processing has following features per ATM virtual trunk:

— extracts bytes from specified XBI ASIC ports and timeslots
— finds cell delineation based on HEC method (I.432.1)
— unassigned and idle cells are discarded
— cells with corrupted headers are discarded and discard events are counted (discarded HEC error cells)
— no header error correction is done
— cell delineation state is readable from the microcontroller
— trunk identifier is generated and inserted before the cell distinguishing VPs with same VPI on separate ATM virtual trunks from each other

The following features are optional and can be chosen by the NMS per each ATM virtual trunk:

— Payload descrambling for $x^{43}+1$ self synchronising scrambled data (ABP513 only)
— HEC descrambling with the coset (55_h)

Multiplexing structure

Receive/Ingress ATM cells with valid VPI values are byte synchronously mapped to the Xbus port timeslots associated with an appropriate ATM virtual trunk. The mapping preserves cell and byte sequence integrity. If there is no cell available for mapping an idle cell is transmitted instead.

The transport framing of the Xbus bytes carrying ATM cells is performed at the DXX trunk interface units (for example GMH, GMU). Standard (G.804, G.707) framing of cells to T1, E1 (30x64 k), VC-12, VC-2 and VC-2-mc can be supported as well as proprietary framing to E1 (31x64 k), nx64k, E2, VC-12-mc and DXX split trunks.

Transmit/Egress ATM cells are reconstructed from the X-bus bytes based on cell header error correction byte based cell alignment (I.432.1). Idle or unassigned cells are dropped and valid ATM cells are forwarded to the ATM cell processor module.

X-BUS interface ports

Sixteen 32x64 kbit/s ports can be used for ATM virtual trunk cell mapping. Any capacity from 64 kbit/s to 256x64 kbit/s can be allocated for one virtual trunk. Ports are reserved solely for one virtual trunk at a time, ports cannot be shared between ATM virtual trunks.

6.1.2.4 STM-1 ATM access interface

The AIU ATM access interface is designed as a factory replacable module which allows for a versatile selection of external physical media interface types. Single mode intraoffice type optical interface according to G.957, multimode intraoffice type optical interface according to ATMF UNI3.1 and UTP-5 category electrical interface according to ATMF af-phy.0015.000 are supported.

The STM-1 ATM access interface adapts a partially filled 155 Mbit/s STM-1 user equipment ATM-interface to AIU internal UTOPIA level 1 module interface.

ATM cell mapping for the STM-1 ATM access interface is specified in I.432.2 and G.707 is followed.

IF Performs transmission path termination TP_T and framing for the STM-1 interface and transmission path /virtual path adaptation TP/VP_A, extracts/maps the cell stream from/to the STM-1 VC4 container.

ATM cell payload scrambling and descrambling is based on self-synchronizing scrambler $x^{43}+1$ polynomial as per I.432.1. Scrambling can be set on/off.

HEC coset byte (55_h) as per I.432.1 adding can be set on/off on tx and rx directions separately.

Optical Interface

When the physical media is multimode fiber AIU is recommended to be equipped with STM-1-IO-13 ATM access interface module. When the physical media is single mode fiber AIU is recommended to be equipped with STM-1-IO-13S ATM access interface module.

The intra office G.957 optical STM-1 interface is supported for single mode version and intraoffice ATMF UNI 3.1 optical STM-1 interface is supported for multimode version.

The fiber connector type used in both optical modules is SC.

Electrical Interface

When the physical media is category 5 unshielded twisted pair AIU is recommended to be equipped with UTP-5 ATM access interface module. ATMF af-phy.0015.000 electrical STM-1 interface is supported for electrical version.

The electrical connector type used is RJ-45.

Multiplexing structure

Standard (I.432.2) mapping of ATM cells to STM-1 VC-4 is supported. The bit rate available for ATM cells is 149 760 kbit/s.

The egress ATM cell stream is first mapped into the C-4 and then to VC-4 along with the VC-4 overhead (POH). The ATM cell boundaries are aligned with the STM-1 octet boundaries. Cell may cross a C-4 boundary.

Cell rate decoupling type at the ATM access interface is based on idle cells.

Section Overhead (SOH) and Path Overhead (POH)

The bytes in the following table representing the nine row nine column structure of STM-1 frame SOH are processed at the STM-1 ATM access interface.

The following acronyms will be used:

A1, A2 = TX/RX frame bytes F6F6F6282828

J0 = Regenerator Section Trail Trace Identifier

NU = national use

B1 = TX generates BIP-8 for Regenerator Section, Rx counts RS BIP-8 errors

H1, H2 = TX normal new data flag 110 (1-4), SDH SS bits 10 (5-6), J1 pointer 10 (7-8), 0A (1-8)

H3 = pointer action 00 (1-8)

B2 = Tx generates BIP-24 for Multiplex Section, Rx counts MS BIP-24 errors

K2 = No alarm (6-8) 000, TX set L_RDI (6-8) 110 when LOS or LOF in RX, L_AIS 111 (6-8).

Z21, Z22 = TX FEBE when rx B2 errors

M1 = BIP-24 remote error indication

J1 = TX generates as null trace message 00hexa,

B3 = TX generates BIP-8 for Path Section, RX counts path BIP-8 errors

C2 = TX byte value 13_h (ATM cells), Rx valid codes 13_h and 01_h

G1 = TX generates FEBE (bits1-4=) on rx path B3 byte errors, TX generates P-RDI (bit5=1) when TP_RDI, RX

	Function	**Column**									**POH**
		1	2	3	4	5	6	7	8	9	1
1	Framing	A1	A1	A1	A2	A2	A2	J0 01h	NU1 AA	NU2 AA	J1
2	Error monitor-ing	B1 BIP-8							NU3	NU4	B3 BIP-8
3											C2 13h
4	VC-4 pointers, AU AIS	H1 AU-4	Y	Y	H2 AU-4	1* FF	1* FF	H3 action	H3 action	H3 action	G1 P-RDI
5	Error monitoring	B2 BIP-24	B2 BIP-24	B2 BIP-24	K1	U5	U6	K2 AIS/RD I	U7	U8	
6		D4 FF	U9	U10	D5 FF	U11	U12	D6 FF	U13	U14	
7		D7 FF	U15	U16	D8 FF	U17	U18	D9 FF	U19	U20	
8		D10 FF	U21	U22	D11 FF			D12 FF		U26	
9	Error reporting						M1 B2 err.		NU5	NU6	

6.1.2.5 ATM cross-connect

VP-level cross-connection between ATM access interface and ATM virtual trunks are performed. Cross-connections between ATM virtual trunk VPCs are not supported at the AIU matrix.

Setup of VPCs between AIUs requires information on planned VPI usage at the ATM access interfaces on both ends of the connection. The VPIs used are entered as valid VPIs to the AIU VP- table along with the cross-connect information telling to which ATM virtual trunk and VPL the cells are connected to.

6.1.2.6 AIU Cell Buffers

Buffering is required to handle momentary cell bursts from the ATM access interface which can be caused by subsequent cell arrival on several PCR-based VPCs.

In receive direction (demultiplexing) each of the ATM virtual trunks has a dedicated buffer in external RAM. Maximum size of buffer is 2000 cells. Buffer size and thresholds are configurable by NMS per ATM virtual trunk as ‘virtual buffer size’. In the demultiplexing direction each of the cell buffers is served with its associated ATM trunk capacity and small cell buffers allow for some buffering.

In transmit direction (multiplexing) no buffering is implemented except for cell alignment and multiplexing purposes (~ 2 cells per trunk). In the multiplexing direction all the cell buffers are to be served in less than one cell duration on the highest capacity ATM trunk (16 Mbit/s=37 kcps, cell duration is 27μs) so that no queues can be accumulated. Empty cell buffers are skipped.

AIU 1:1 ABP513 supports buffering for one ATM virtual trunk interface whereas AIU 1:4 supports buffering for four ATM virtual trunks in parallel. Cell buffers at ABP513 and ABP551 are implemented with four static RAMs giving an 8000 cell buffer capacity.

The following buffer related logic is supported per each ATM virtual trunk:

- If the buffer is full the cells arriving to buffer are discarded and discard events are counted (buffer overflows)
- SW control can enable (congestion reset enable) HW to truncate cell buffer to a specified level (congestion reset left over) if the buffer is found to be filled above specified threshold (congestion threshold) by SW. Oldest (blocking) cells are discarded and discard events are counted in SW (congestion resets). HW logic does not truncate buffers without triggering by SW.
- minimum buffer level (MinCellBufferFillLevel) from last microcontroller read is kept
- maximum buffer level (MaxCellBufferFillLevel) from last microcontroller read is kept
- cell transmits to ATM virtual trunk when buffer has been over a specified level can be counted (Casual Congestions)

No per VPI based buffering is supported so it is possible that one misbehaving VPC affects traffic flow on other VPCs.

6.1.2.7 ATM level OAM features

AIU can insert and extract standard F4-level OAM cells from any of the VPCs configured. OAM cells are handled both at the ATM access interface and at the ATM virtual trunk interface.

The format of F4-level OAM cells is specified in I.610. Each VPC is constantly monitored for standard OAM cells and user defined action is taken.

VPC segments creation, modification and deletion which is required for proper segment based OAM functionality is supported with NMS. Also one headed segments with other end outside DXX network are possible.

Continuity check

Continuity check (cc) lets the operator know if a particular virtual path connection or virtual path connection segment is constantly operational. VP segment and end-to-end level continuity check for AIU is available via the DXX NMS CLT-tool. For management VP end-to-end continuity check is available via AIU node manager window. The repetitive sending mechanism is selected to be supported (1c/s per cc-VP). When AIU is defined as a segment sink point it is able to detect and declare the loss of continuity defect (LOC). LOC is declared if no continuity check cells or user cells on the cc-VP is received.

AIU is able to support cc on all configured VPCs on virtual trunk side. On access interface side AIU supports maximum of 12 simultaneous continuity checks. Continuity check can be performed on all ATM virtual trunks simultaneously. It must be born in mind that repetitive cc-mechanism represents 424bit/s load on the VPCs and will thus affect VPC performance.

The continuity check must be specifically activated/deactivated on the VPC. The activation is done by the network management. Activation/deactivation can also be done with activation/deactivation cells from external equipment.

VP-AIS

VP-AIS is used for reporting defect indications in the forward direction.

VP-AIS cells will be sent periodically (1cps) by AIU when receiving transmission path-AIS defect indications from the Physical Layer. VP-AIS is also sent if a LOC defect is declared on cc-VP.

The VP-AIS is sent along all VP connections affected. So if TP-AIS is received from ATM access interface then VP-AIS is generated to all VPs on all ATM virtual trunks.

VP-AIS cells are nonintrusively monitored by AIU and this info is available for system management.

VP-AIS is not duplicated on a VP already forwarding VP-AIS.

VP-RDI

VP-RDI is used for reporting remote defect indications in the backward direction as per I.610.

VP-RDI is monitored at AIU ACP module and this info is available for system management. User VP-RDI is passed on to the VPC end point.

VP Cell loopback

Cell loopback lets the operator test any particular virtual circuit connection or segment operation by defining VP level loopback loops on the network equipment.

AIU loopbacks can be activated on both ATM access interface and ATM virtual trunk interface. Loopback source acts as a test cell generator/analyzer and loopback sink performs the looping function for the test cells.

AIU supports loopback location ID use. Loopback location ID has 16 octets reserved in the loopback cell payload and 16 octets for loopback source ID.

AIU supports segment and end to end loopback cells.

The cell loopbacks are ATM level loopbacks to be run on F4 OAM cells for VPCs. Cell loopbacks can be performed on all ATM virtual trunks simultaneously.

6.1.2.8 ATM traffic management

The AIU cell transfer performance is characterized by the cell buffering related information. Since AIU is adapting a high speed interface to a lower speed ATM virtual trunk(s) it needs to buffer cells. The AIU buffer fill level varies depending on how well the traffic shaping and VPC PCR-control at the ATM equipment utilizing AIU performs. Buffer fill variation will cause cell delay variation. Buffer overflow will cause cell loss. Large buffer fill will cause increased cell transfer delay at AIU. Buffering is supported in the ingress direction at AIU HW ABP buffering module on per virtual trunk basis.

ATM traffic is controlled only with relatively shallow cell buffers at the AIU ABP module in the ingress direction. All cells going to the same ATM trunk use the same cell buffer and single queue. UPC must be done on the ATM network side outside DXX transport network. No particular service classes or QoS classes are directly supported. User will be able to use individual VCs within the VPCs as long as none of the VCs is required to have a higher QoS than the ATM trunk (can be one or more VPCs). A rough QoS (MCTD, CDV and CLR dependent on incoming traffic shape) of an ATM trunk can be either explicitly specified at trunk creation time or is implicitly specified by the trunk buffer size and buffer related configurable logic.

The function of AIU in traffic handling is simply to adapt asynchronous ATM cell stream from STM-1 to wanted ATM trunk cell transport method (for example E1 circuit across DXX network). Cell burst handling is trusted up to attached ATM equipment traffic shaping function (TS).

There is an option of resetting the cell buffers if unacceptable CTD is experienced. The ABP HW supports buffer fill level to buffer threshold comparison which is used to tick a counter in case the threshold is exceeded. This counter value is read and interpreted by SW running on ACP module to set a fault condition. If buffer reset is allowed the ABP HW can reset the buffer to a level specified by SW settable parameter.

Cell discarding by resetting buffers is the only direct congestion control option for AIU. Discarding is based solely on the user definable threshold and in no way to CLP. No cell tagging is performed. No cell priority features will be implemented. No EFCI will be implemented.

The receive/ingress direction buffer size and the buffer thresholds are individually definable for each ATM virtual trunk as ‘virtual buffer size’. Maximum buffer size is 2000 cells.

6.1.2.9 AIU timing

Two timing modes are supported by the AIU:

1. In transmit timing mode the ATM access interface transmitter uses node clock as timing reference. (local timing)
2. In loop timing mode the ATM access interface transmitter uses timing received from line as reference. (rx timing)

AIU interface is not used as node clock synchronization reference.

6.1.2.10 Performance monitoring

AIU HW provides data for system performance records summarizing the AIU performance over a 24 hour or 15 minute period based on ACP cell statistics, buffer monitoring and OAM cell information available on VPL level.

VPC related data

Txed/cells	Transmitted user cells
Rcvd/cells	Received user cells (non-zero VCI)
Txed/OAM	Transmitted OAM cells
Rcvd/OAM	Received OAM cells
PVpAIS	Received VP-AIS cells
PVpRDI	Received VP-RDI cells

ATM access interface related data

Txed/cells	Transmitted user cells
Rcvd/cells	Received user cells (non-zero VCI)
DisHec	Discarded HEC errored cells
DisPro	Discarded Protocol errored cells
AtmOcdTm	Out of cell delineation events
BerPs	Path section BIP-8 error ratio

ATM virtual trunk related data

Txed/cells	Transmitted user cells
Rcvd/cells	Received user cells (non-zero VCI)
DisHec	Discarded HEC errored cells
DisPro	Discarded protocol errored cells
VtOutDis	Cells discarded due to congestion reset
AtmOcdTm	Out of cell delineation time
MxBFL	Maximum cell buffer fill level
MnBFL	Minimum cell buffer fill level
CngRes	Buffer resets due to congestion
Ovrfls	Lost cells due to cell buffer overflow
CaCngs	Cell transmission times when casual congestion situation has been active
CngSec	Congested seconds
PeCSec	Persistently congested seconds

6.1.2.11 Loops in AIU

STM-1 interface equipment loop can be activated for diagnostic purposes. ATM access interface module transmit data is turned back to receive data inside AIU.

User defined ATM OAM cell loops are available.

6.1.2.12 AIU protection

ATM virtual trunks are protected by the DXX network circuit protection means.

6.1.2.13 Network management control channels

DXX management channels are configured as usually in DXX networks. The DXX processor at AIU ABU257 module is responsible for DXX management communication.

6.1.2.14 ATM control functions

AIU does not directly support ILMI. Transparent transport of ILMI messages is supported. ILMI VCCs are multiplexed at AIU 1:4 according to ATMF UNI signalling 4.0 Annex 8: multiple signalling channels.

AIU does not directly support signalling. Transparent transport of signalling messages is supported. Signalling VCCs are multiplexed at AIU 1:4 according to ATMF UNI signalling 4.0 Annex 8: multiple signalling channels.

6.1.2.15 Node requirements

For installation of AIU into a Midi, a Basic or a Cluster Node hardware and software of other DXX units must have the following or later version

SCU Node Control Unit equipped with

— SCP211 (HDLC-4CH) Control Channel Expansion Module
— SCZ281, SCP211 software module V3.1
— SCZ280 software module V8.4

In Basic Node SXU-A or SXU-B Cross-connect Unit equipped with

— SXZ282, SXU software module V6.6

In Midi Node XCG Cross-connect Unit equipped with

— SMZ538, XCG software module V2.0

In Cluster Node SXU-C Cross-connect Unit equipped with

— SXZ289, SXU-C software module V2.7

6.1.3 Modules for AIU ATM Interface Unit

6.1.3.1 General

The optical and electrical interface modules used in the AIU units are:

— STM-1-IO-13

ATM interface unit consists of the modules in the following table and ATM access interface module.

MODULE CODE	FUNCTION	PCS/AIU
ABU257	ATM Base Unit	1
ABP513	ATM buffering and switching block	1 in AIU 1:1
ABP551	ATM buffering and switching block	1 in AIU 1:4
ACP514	ATM cell processing module	1
PDF520	12V, 5V and 3.3V power supply module	1

Module Structure

ABU257

The main functional blocks of the ABU257 are:

1. DXX processor of the unit
2. DP-RAM interface to ACP514 ATM processor
3. Xbus interface
4. VTP control bus interface
5. Power supply interface
6. AIU LEDs

ACP514 - ATM cell processor module

The main functional blocks of the ACP514 are:

1. ATM processor of the unit
2. DP-RAM interface to ABU257 DXX processor
3. ATM cell processing block
4. Utopia level 1 interface to the ATM access interface module
5. Utopia level 1 -like interface to the ATM virtual trunk interface

ATM virtual trunk interface modules

NAME	MODULE CODE	FUNCTION	PCS/AIU
ABP-1:1	ABP513	1:1 multiplexing and buffering module	1
ABP-1:4	ABP551	1:4 multiplexing and buffering module	1

The main functional blocks of the ABP-modules are:

1. Utopia level 1 -like interface to ACP514
2. ABU-XBI asic interface
3. TX ATM virtual trunk interface cell multiplexing CPLD
4. RX ATM virtual trunk interface cell demultiplexing CPLD
5. RX ATM virtual trunk specific cell buffers

ATM access interface modules

NAME	MODULE CODE	FUNCTION	PCS/AIU
STM-1-IO-13	ODH491	Optical intra office multimode 1.3um STM-1 interface	1
STM-1-IO-13S	ODH575	Optical intra office single mode 1.3um STM-1 interface	1
UTP-5	EDH390	Electrical UTP-5 STM-1 interface	1

Interface modules contain the following functional blocks:

1. Optical/electrical STM-1 line interface
2. Clock recovery
3. System clock to node clock locking
4. Transmit clock multiplication
5. STM-1 and VC-4 termination and ATM cell mapping
6. Utopia level 1 interface to ACP514

PDF520- Power module

The main function of the PDF520 to provide 12V, 5V and 3.3V power for AIU operation from the 48V battery voltage available. The operating voltages are monitored and a functional disturbance activates a fault message.

6.1.4 Faults and Actions in AIU ATM Interface Unit

6.1.4.1 AIU faults and actions

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Alarm
R = Red alarm LED
Y = Yellow alarm LED
VPAIS = VP-AIS cell insertion
MS-RDI = MS-RDI generation
P-RDI = P-RDI (AU-RDI) generation
VP-RDI = VP-RDI generation (applicable in Management VP only)

Common Logic Faults

Fault condition	Status	LED	Rx signal	Tx signal	Note
"Reset (DXXP/ABZ531)" there has been a unit reset	PMA, S	R	Bus IF off	Off	
"System clock missing" 19.44 MHz clock of the AIU is missing	PMA, S	R	-	-	
"16/20 Mhz clocks not locked" 19.44 MHz clcok of the AIU not locked with 16.896 MHz clock of the node.	PMA	R	-	-	
"F/MSYNC problem in XBUS" X-bus syncronization pulse transmitted by the SXU is missing.	PMA, S	R	-	-	
"IA alarm from IA monitoring" The IA addresses do not work correctly.	PMA, S	R	-	-	
"Backup unit fault" Extended backup unit is not responding.	PMA	Y	-	-	
"VB 1: +5 V (BUS 1)" The VB 1 voltage is below the threshold limit.	PMA	R	-	-	
"Power +12 V" The board 12 V supply voltage is below the threshold limit.	PMA	R	-	-	
"Reset (ATMP)" There has been a unit reset.	PMA, S	R	-	Off	
"Power +3.3 V" The board 3.3 V supply voltage is below the threshold limit.	PMA	R	-	-	
"Protected bus voltage" Protected bus voltages are above the threshold limit.	PMA	R	-	-	
"Node clock missing" 16.896 MHz node clock is missing.	PMA, S	R	-	-	
"Start permission denied" Most likely the unit does not belong to the node configuration.	PMA, S	R	Bus IF off	Idle pattern in the payload	
"ATMP not responding" Communication between AIU processor modules is not OK.	PMA	R	-	Off	

Fault condition	Status	LED	Rx signal	Tx signal	Note
"CPU Memory faults (abz531)" RAM fault EPROM fault EEPROM faults	PMA, S	R	-	-	
"CPU Memory faults (abz531)" Flash faults	PMA	R	-	-	
"DPRAM fault (abz531)"	PMA, S	R	-	-	
"Missing settings (abz531)" One of the setting structures has been corrupted in the non-volatile memory.	PMA, S	R	-	-	
"Settings corrupted" Fatal setup corruption.	PMA	R	-	-	
"Incompatible sw EPROM/flash" The downloaded sw is not compatible with the system sw on the EPROMs.	PMA, S	R	-	-	
"Chksum err in dwnlded sw (abz531)" The download sw has been corrupted.	PMA, S	R	-	-	
"Incompatible sw DXXP/ATMP" SW version mismatch between DXXP and ATMP.	PMA, S	R	-	-	
"Setup data mismatch" Conflict in the backup setting parameters.	PMA, S	R	-	-	
"Initialization error (abz531)" Initialization phase failed.	PMA, S	R	-	-	
"CPU memory faults (acz700x)" RAM fault EPROM fault	PMA, S	R	-	-	
"CPU memory faults (acz700x) EEPROM fault Flash faults	PMA	R	-	-	
"Missing settings (acz700x)" One of the setting structures has been corrupted in the non-volatile memory.	PMA, S	R	-	-	
"Cell Processor failure" Self-test failure in the ATM cell processor.	PMA, S	R	-	-	
"Cell Processor memory error" ATMC SRAM memory access failure.	PMA, S	R	-	-	
"Incompatible sw EPROM/flash" The downloaded sw is not compatible with the system sw on the EPROMs.	PMA, S	R	-	-	
"Checksum error in dwnlded sw" The downloaded sw has been corrupted.	PMA, S	R	-	-	
"Initialization error (acz700x)" Initialization of application sw unsuccessful.	PMA, S	R	-	-	
"Tx FPGA fault" Self-test failure in Tx FPGA.	PMA, S	R	-	-	
"Rx FPGA fault" Self-test failure in Rx FPGA.	PMA, S	R	-	-	
"RAM fault" ATM virtual trunk interface module SRAM test detected a memory fault.	PMA	R	-	-	
"Missing module" ATM virtual trunk or ATM access interface module is missing.	PMA, S	R	-	-	
"Conflict in module type" A conflict between the installed module and the settings.	PMA, S	R	-	-	

Fault condition	Status	LED	Rx signal	Tx signal	Note
"ATM access interface module internal loopback" An interface loop is created in the ATM accesss interface module.	MEI, S	Y	-	-	
"Rx buffer overflow" ATM virtual trunk interface module Rx buffer overflow detected.	DMA	-	-	-	
"Fault masked/test" Unit main block faults are masked.	MEI	Y	-	-	
"HW fault in module" A severe error in the ATM virtual trunk interface module.	PMA, S	R	-	-	
"ATM access interface ASIC failure" A severe ASIC failure in the ATM access interface module.	PMA, S	R	-	-	
"ATM access interface module EEPROM failure" Failure to access interface module EEPROM	PMA, S	R	-	-	

ATM Access Interface Faults

Fault condition	Status	LED	Rx signal	Tx signal	Note
"atmAccessportReceiveFifoAlarm" Receive FIFO full in the ATM access interface module	PMA	R	-	-	
"UnavailablityThresholdCrossed" A User-defined threshold value for unavailability is exceeded.	DMA	-	-	-	
"NumESsThresholdCrossed" A user-defined threshold value for errored seconds is exceeded.	DMA	-	-	-	
"NumSESsThresholdCrossed" A user-defined threshold value for severely errored seconds is exceeded.	DMA	-	-	-	
"Loss of Signal (LOS)" Loss of signal defect is declared when a supervised signal hasn't had any transitions for a period of time. See ITU-T G.783	PMA, S	R	VP-AIS	MS-RDI P-RDI VP-RDI	
"BIP-8 RS (B1) ThresholdCrossed" A user-defined threshold value for BIP error on regenerator section is exceeded.	DMA	-	-	-	
"BIP-24 MS (B2) ThresholdCrossed" A user-defined threshold value for BIP error on multiplexer section is exceeded.	DMA	-	-	-	
"BIP-8 PS (B3) ThresholdCrossed" A user-defined threshold value for BIP error on path section is exceeded.	DMA	-	-	-	
"Loss Of Frame (LOF)" Loss of frame detected. See ITU-T G.783	PMA, S	R	VP-AIS	MS-RDI P-RDI VP-RDI	
"Loss Of Pointer (AU_LOP)" Loss of AU-pointer detected. See ITU-T G.783	PMA, S	R	VP-AIS	P-RDI VP-RDI	
"Multiplex Section AIS (MS_AIS)" Multiplex section AIS detected. See ITU-T G.783 and G.707	MEI, S	Y	VP-AIS	MS-RDI P-RDI VP-RDI	
"Path AIS (AU_AIS)" Path (AU) AIS detected. See ITU-T G.783 and G.707	MEI, S	Y	VP-AIS	P-RDI VP-RDI	
"Multiplex Section RDI (MS_RDI)" Multiplex section RDI detected. See ITU-T G.783 and G.707	MEI	Y	-	-	
"Path RDI (AU_RDI)" Path (AU) RDI detected. See ITU-T G.783 and G.707	MEI	Y	-	-	
"PayLoad Mismatch (PLM)" Payload mismatch detected.	PMA, S	R	-	P-RDI VP-RDI	
"Fault masked/test" Interface fault mask setting is on.	MEI	Y	-	-	
"Loss of Continuity (LOC) in management VP." Loss of continuity detected in the management VP. See ITU-T I.610	MEI	Y	VP-AIS	-	
"excessivediscardedHecErrorCells" A user-defined threshold value for discarded HEC error cells exceeded.	DMA	-	-	-	
"excessivediscardedProtErrorCells" A user-defined threshold value for discarded protocol error cells exceeded.	DMA	-	-	-	
"Loss of Cell Delineation (LCD)" Out of cell delineation anomaly has persisted long enough to cause Loss of Cell Delineation defect.	PMA, S	R	VP-AIS	P-RDI VP-RDI	

ATM Virtual Trunk Interface Faults

Fault condition	Status	LED	Rx signal	Tx signal	Note
"Fault masked/test" Interface fault mask setting is on.	MEI	Y	-	-	
"Loss of Continuity (LOC) in management VP." Loss of continuity detected in the management VP. See ITU-T I.610	MEI	Y	VP-AIS	-	
"excessivediscardedHecErrorCells" A user-defined threshold value for discarded HEC error cells exceeded.	DMA	-	-	-	
"excessivediscardedProtErrorCells" A user-defined threshold value for discarded protocol error cells exceeded.	DMA	-	-	-	
"Loss of Cell Delineation (LCD)" Out of cell delineation anomaly has persisted long enough to cause Loss of Cell Delineation defect.	PMA, S	R	VP-RDI	VP-AIS	
"atmVTCasualCongestionAlarm" Temporary congestion in ATM virtual trunk interface detected.	MEI	-	-	-	
"atmVTCongestedSecondAlarm" A user-defined threshold value for congested seconds in ATM virtual trunk interface is exceeded.	MEI	-	-	-	
"atmVTPersistentlyCongested Alarm" A user-defined threshold value for persistently congested seconds in ATM virtual trunk interface is exceeded.	MEI	Y	-	-	

VPI fault in ATM Access Interface and Virtual Trunk Interface

Fault condition	Status	LED	Rx signal	Tx signal	Note
"VP defect" Virtual Path defect detected. VP-AIS or VP-RDI detected.	MEI	Y	VP-AIS	VP-RDI	

6.1.5 AIU Front Panel

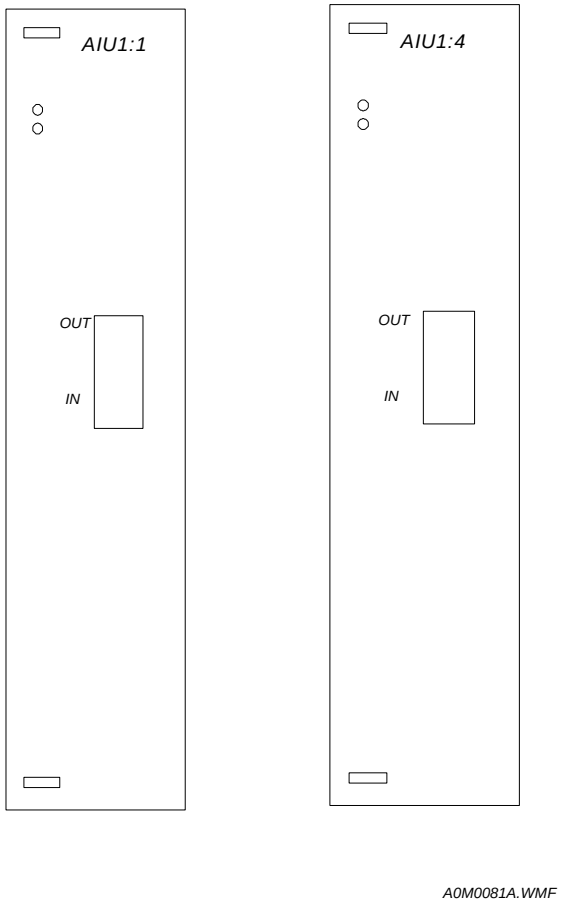


Fig. 7: AIU ATM Interface Unit Front Panel

6.1.6 Technical Specifications for AIU ATM Interface Unit

6.1.6.1 ATM Access Interfaces

- STM-1 single mode fiber optical intraoffice, G.957
- STM-1 multimode fiber optical intraoffice, ATMF UNI3.1
- STM-1 UTP-5 cable electrical, ATMF af-phy.0015.000

STM-1 MMF Optical Interface Intraoffice

Bit Rate	155.52 Mbit/s
Input tolerance	± 20 ppm
Code	NRZ
Pulse shape	ITU-T G.957 (fig.2)
Transmission media	multimode fiber
Optical transmitter	LED
Operating wavelength range	1261…1360 nm
Typical spectral RMS width	58 nm
Mean launched power - minimum - maximum	 - 20 dBm - 14 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	PIN diode
Receiver minimum sensitivity (BER 1E-10)	- 29 dBm
Receiver minimum overload	- 14 dBm
Connector type	SC

STM-1 SMF Optical Interface Intraoffice

Bit Rate	155.52 Mbit/s
Input tolerance	±20 ppm
Code	NRZ
Pulse shape	ITU-T G.957
Transmission media	Singlemode fiber
Optical transmitter	Class-1 Laser (IEC825)
Operating wavelength range	1260…1360 nm
Typical spectral RMS width	7.7 nm
Mean launched power - minimum - maximum	 -15 dBm -8 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	
Receiver minimum sensitivity (BER 1E-10)	- 28 dBm
Receiver minimum overload	- 8dBm
Connector type	SC

STM-1 UTP-5 Interface

Bit Rate	155.52 Mbit/s
Input tolerance	±20 ppm
Code	NRZ
Transmission media	UTP-5
Nominal impedance	100 Ω
Pulse shape	af-phy.0015.000
Jitter/Jitter tolerance	1.5ns peak-to-peak / af-phy.0015.000
Connector type	RJ-45/ISO/IEC 8877

6.1.6.2 ATM Cross-Connect

Matrix type[a]	1:N
Cross-connection level	Virtual Path
Connection types	bi-directional
Connection capacity	16 Mbit/s
Maximum number of VPCs	256-1024
Buffering	Output buffered per ATM virtual trunk

a Cross-connection between ATM Access Interface (1) and ATM virtual trunks (N). VP Cross-connection between ATM virtual trunks is not supported

ATM Access Interface Termination and Mapping

Frame structures	STM-1, G.707
ATM cell mapping	VC4, I.432.2 and G.707
SOH access	Limited

ATM Virtual Trunk Termination and Mapping

Frame structures	DXX interface unit framings
ATM cell mapping	Byte synchronous nx64k to X-bus

6.1.6.3 Other characteristics

Power supply	48 V DC
Power consumption	17 W
Unit size w x d x h (mm)	50x160x233
Unit width (T)	10

6.1.6.4 NMS restrictions

NMS release 9.0B is required. No other special requirements.

6.1.6.5 Relevant ATM standards

ITU-T recommendations

I.150	B-ISDN Asynchronous Transfer Mode Functional Characteristics	ITU-T 11/95
I.311	B-ISDN General Network Aspects	ITU-T 08/96
I.321	B-ISDN Protocol Reference Model and Its Application	ITU-T 1991
I.361	B-ISDN ATM Layer Specification	ITU-T 11/95
I.413	B-ISDN User Network Interface	ITU-T 03/93
I.432.1	B-ISDN User Network Interface Physical Layer Specification - General Characteristics	ITU-T 08/96
I.432.2	B-ISDN User Network Interface Physical Layer Specification for 155 520 kbit/s and 622 080 kbit/s	ITU-T 08/96
I.610	B-ISDN Operation and Maintenance Principles and Functions	ITU-T 11/95.
G.707	Network node interface for the SDH	ITU-T 03/96
G.803	Architectures of transport networks based on the SDH	ITU-T 03/93
G.804	ATM Cell Mapping into Plesiochronous Digital Hierarchy	ITU-T 11/93
G.810	Considerations on Timing and Synchronization Issues	ITU-T 08/96
G.957	Optical interfaces for equipments and systems relating to the SDH	ITU-T 07/95

ATM-Forum implementation agreements

af-phy.0010.002	UNI 3.1	ATM-Forum
af-phy.0015.000	ATM Physical Medium Dependent Interface Specification for 155 Mb/s over Twisted Pair Cable	ATM-Forum

6.2 CAE VF Interface Unit

6.2.1 General

The CAE offers voice frequency and signalling interfaces to DXX Cross-Connect System. It is used for trunks to analog PABXes or exchanges. Other applications are analog trunks between base stations and exchanges in mobile networks, direct tielines between analog PABXes and leased lines using VF carrier modems. CAE is functionally compatible with the ADPCM server unit EAE.

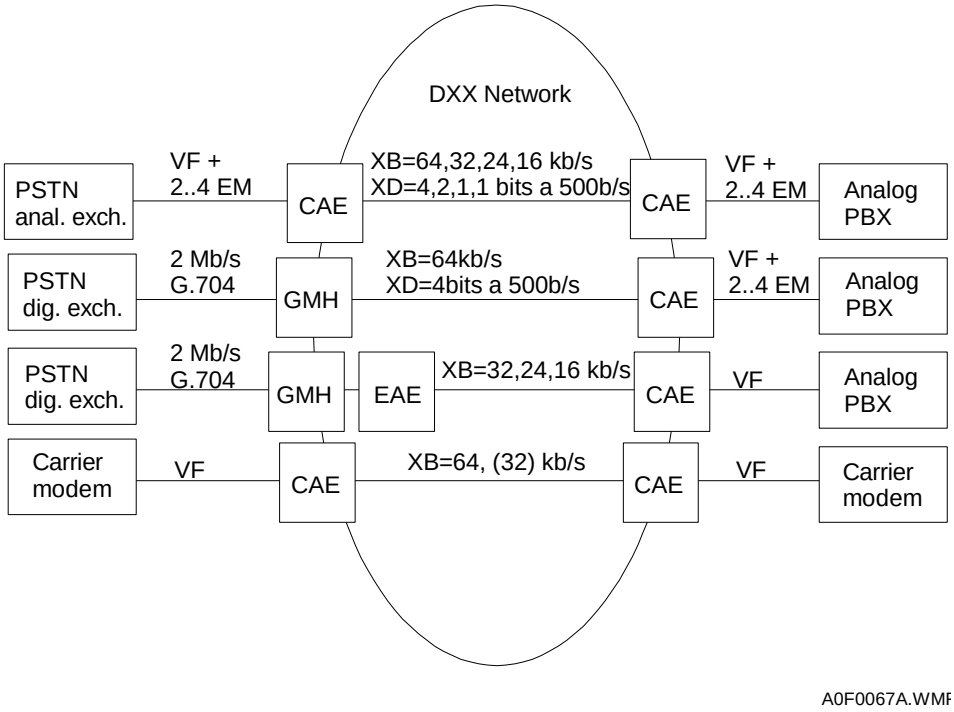


Fig. 8: Applications for CAE

6.2.2 Operation of CAE VF Interface Unit

6.2.2.1 Physical Structure

The body of the CAE consists of a base unit, a power supply and a CAZ 287 program memory. The available interface modules are:

— ADPCM-10VF
— PCM-10VF
— EM-2 x 10

The unit dimensions are 50 x 160 x 233 mm. The front panel houses two alarm LEDs, a red one and a yellow one, and for each interface module two 25-pin, female D-connectors (ISO2110). The back panel holds two euro connectors. The upper accesses the control bus and the lower the 64 Mbit/s data cross-connection bus of the subrack (X-bus). The back panel connectors also provide battery voltage for the power supply module.

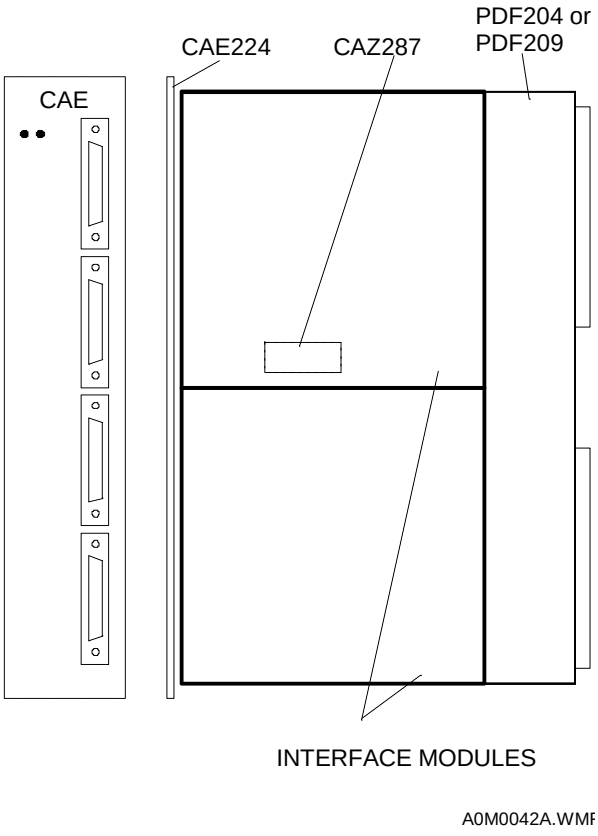


Fig. 9: CAE Unit Equipped with IF Modules

Provisioning

The number of available VF interfaces of the CAE depends on IF module equipment and provisioning. The provisioning is made by NMS; it defines how the interfaces of the unit will be used. Modification of the provisioning is not allowed if any of the interfaces are locked.

The provisioning alternatives depending on module equipment are:

Upper Module	Lower Module	Provisioning Alternatives
ADPCM-10VF	none	10 VF
PCM-10VF	none	10 VF
ADPCM-10VF/ PCM-10VF	EM-2 x 10	10 VF or 10 VF + 10 x 2 EM or 5 VF + 5 x 4 EM
ADPCM-10VF/ PCM-10VF	ADPCM-10VF/ PCM-10VF	10 VF or 20 VF

Functional Structure

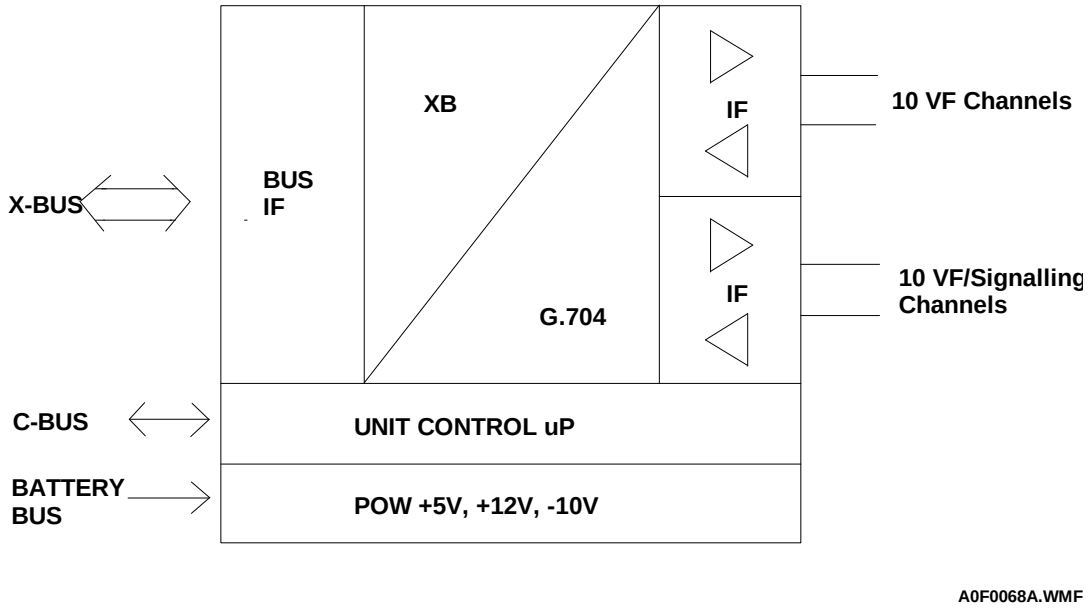


Fig. 10: Functional Structure of CAE Unit

The main functional blocks of the CAE unit are the power supply, unit controller including the processor and its peripheral circuits, PCM RAM and an X-bus interface common for each channels.

Block Diagram

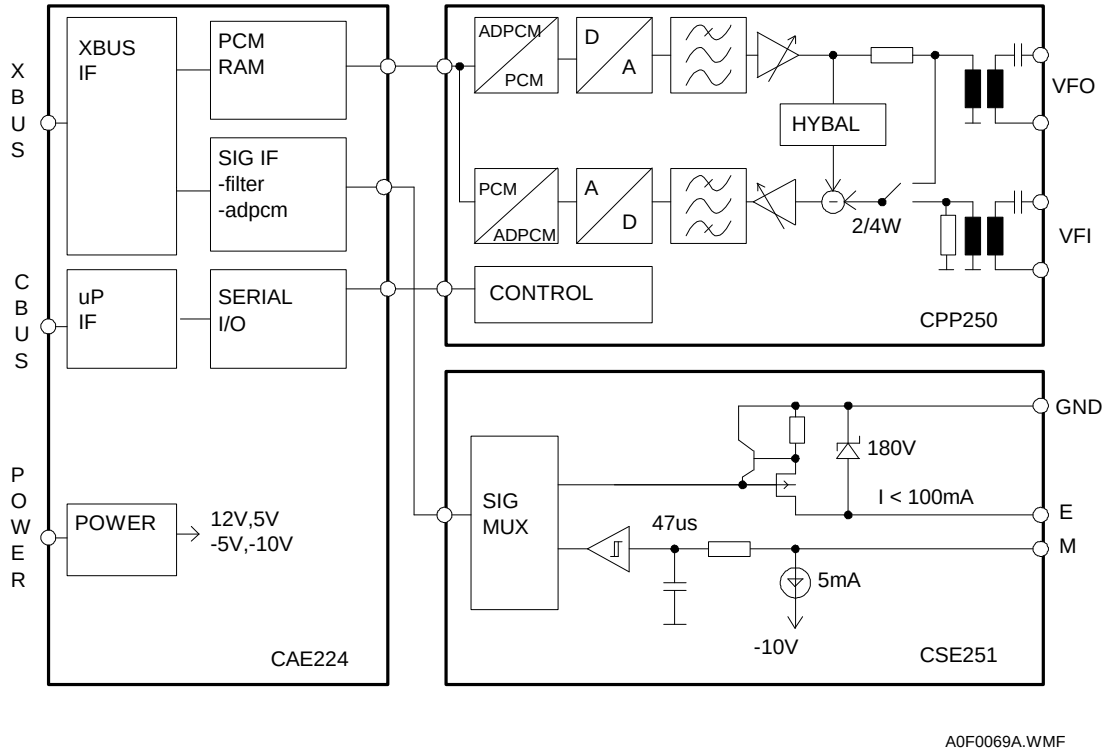


Fig. 11: CAE Block Diagram

6.2.2.2 Power Supply

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the battery bus. The operating voltages are monitored by a multichannel analog-to-digital converter (A/D). A functional disturbance activates a fault message.

A unit receives its operating voltage from the power supply module PDF 204 or PDF 209. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector.

The module provides the operating voltages +5V, +12V and -10V, operating voltage -5V is generated from -10V by a regulator on the base unit. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in a unit reset.

All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

6.2.2.3 Unit Controller

The 80C188 microprocessor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor generates HDLC messages.

The program is stored on the board in an interchangeable EPROM memory identified as CAZ 287. Part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in case of a power interruption, the unit is automatically reset to the conditions prevailing the interruption without specific parameterization. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC-links and for the frame control bus.

6.2.2.4 Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting, it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

6.2.2.5 X-bus Interface

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with the data bus DR2. The cross-connect unit decides with the aid of a bus test which bus to use, and this information is supplied to other units through the control bus. From the cross-connect unit the GMH unit receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are monitored also by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing, the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

6.2.2.6 Loops

The NMS is able to control several loops in the CAE unit. Loops are used to find a faulty section of the line and to calibrate the echo cancellation of 2-wire connection. All loops are loops back to X-bus, no loops are available back to interface.

There are three loop types available:

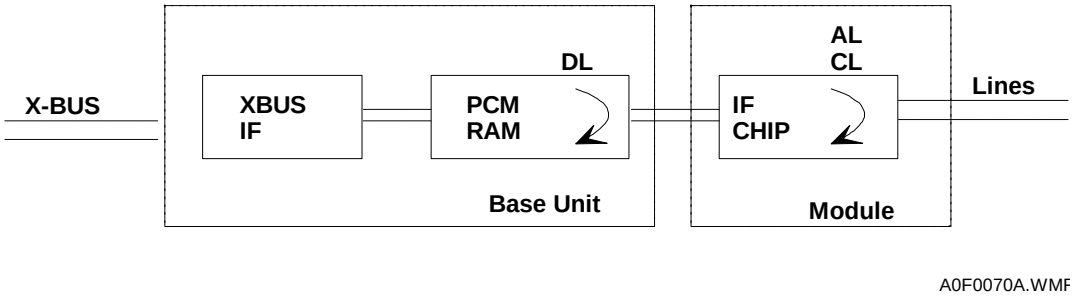


Fig. 12: Loops

— Digital loop DL, which means that data is looped back transparently in a digital section of the base unit.

— Analog loop AL, which means that data is looped back in an analog section of the interface chip in interface module. ADPC-PCM-ADPCM conversion is included if the module supports that function. Loop gain is 0 dB.

— Calibration loop CL, which is used in 2-wire connection to measure the echo cancellation. CL loop is also made in an analog section of the interface chip.

Each channel can be looped independently.

6.2.3 Interface Modules for CAE Data Interface Unit

6.2.3.1 General

The voice frequency and signalling interface modules used in the CAE unit are:

— ADPCM-10VF
— PCM-10VF
— EM-2 x 10

Interface modules

A unit is connected to a transmission line through interface modules. The interface modules contain the analog components required for the interface. The signals between the unit and the interface module are digital signals which are converted to the voice frequency signals in the module.

The processor bus is connected to both interface module connectors. Through this bus it is possible to detect the module type and to read data regarding the module status, e.g. a missing incoming signal.

In the receiving direction the interface module converts the voice frequency signal received from the transmission line in digital format by an A/D converter and maps the channel to the PCM frame. PCM data is written to PCM RAM and led to X-bus interface.

The data transmission channel interfaces convert analog voice frequency signals to/from PCM data of X-bus interface. In the transmitting direction PCM data pulses are converted into a form suitable for transmitting in the required format. In the receiving direction a signal attenuated by the transmission line is amplified. The voice frequency signal is converted in the digital format by an A/D converter. The line interfaces are realized as interface modules so that a unit can have two interface modules of different types at the same time. The available signal interfaces of the unit depend on which interface modules are used.

The PCM channels from interface modules are mapped to a G.704 frame and led to X-bus interface.

Voice Frequency Interface

The X-bus writes data into the PCM RAM using VF interface address IA_VF and time slot number ts, IA_VF is common for all VF channels. The PCM RAM is connected to the interface module through a 2 Mbit/s bus.

In the interface module there is one interface chip for each channel and each chip picks the data from its own time slot in 2Mbit/s bus. If the module supports ADPCM/PCM conversion, there is a converter chip for each channel between the interface chip and a 2Mbit/s bus.

Interface chips make the voice frequency compression which is selected by the NMS.

VF interfaces are equipped with transformers and DC blocking capacitors. The nominal impedance is 600 Ω. There is one transformer for receive and one for transmit direction. In 2-wire connection the receive signal is taken via the transmit transformer.

Signalling Interface

X-bus accesses the signalling interface SIG IF by using the signalling interface address IA_SIG and the 16-frame long multiframe. The signalling interface is connected to the interface module with a 2 Mbit/s bus and it holds the following functions:

— signalling bits coming from the DXX network can be filtered to remove spikes shorter than 8 ms (4 bits).
— ADPCM processing to signalling bits in accordance with G.761 (see Relevant Recommendations).
— loop-back
— µP interface to signalling

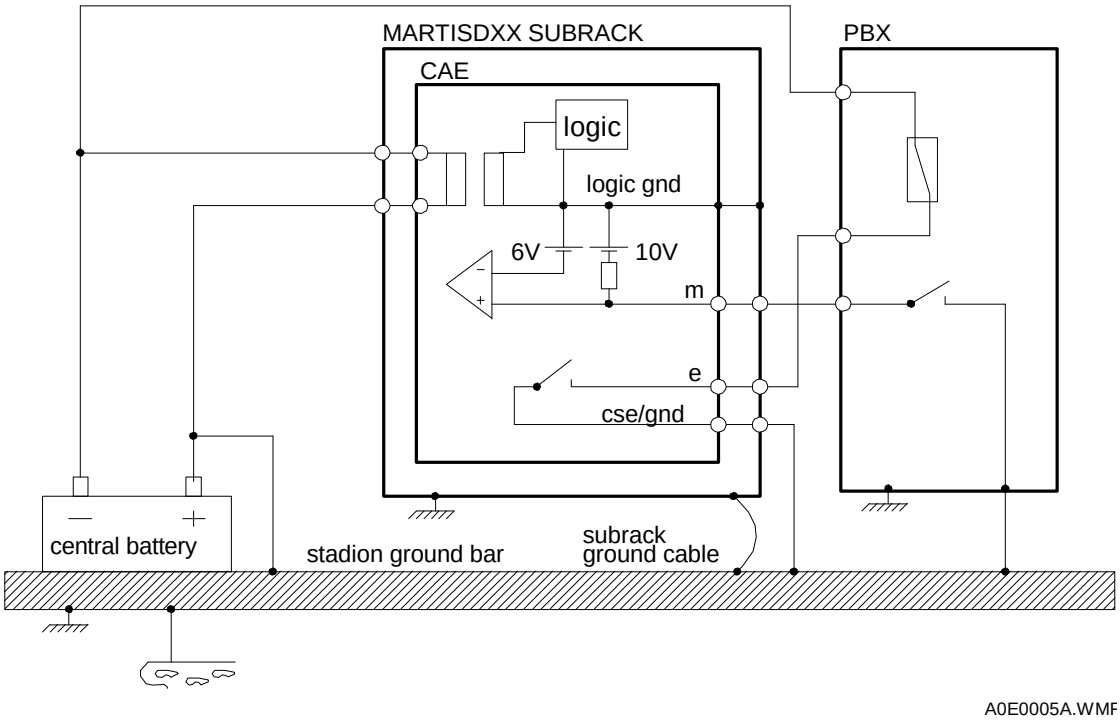


Fig. 13: EM Signalling Interface

The signalling interface operates in "Earth/Minus" manner (E & M). Its input is at negative (minus) potential and it senses when the M-wire is connected to the ground. It contains analogical filtering to remove spikes shorter than 30 ms. Signalling interface output connects the E-wire to the ground (Earth). It contains spark quenching to limit negative voltages in the E-wire to -180 V. The E-wire output current is limited to 100 m.

The E & M interface wires must not be taken outdoors in order not to be exposed to high noise voltages. The PBX signalling interface must be referenced to a ground voltage.

6.2.4 Fault Conditions in CAE VF Interface Unit

6.2.4.1 Common Faults

The following acronyms will be used in the table below:

PMA = Prompt Maintenance Alarm
S = Service Affecting Fault
MEI = Maintenance Event Information
R = Red alarm LED
Y = Yellow alarm LED

Fault Condition	Status	Front LEDs
Power supply: +5 V, -5 V, +12 V, -10 V +5 V back plane voltage	 PMA PMA	 R R
Memory faults: RAM, EPROM fault FLASH fault	 PMA, S PMA, S	 R R
Check sum error: - in FLASH memory - in downloaded SW	 PMA, S PMA, S	 R R
Operation status faults: Unit reset Unit unregistered Setup parameter error Conflict in module type	 PMA, S PMA, S PMA, S PMA, S	 R R R R
Fault masking	MEI	Y
Interface operation		
IF combo write/read fault	PMA, S	R
IF loop to DXX	MEI, S	Y
IF blocked	MEI, S	Y

6.2.5 Front Panel of CAE VF Interface Unit

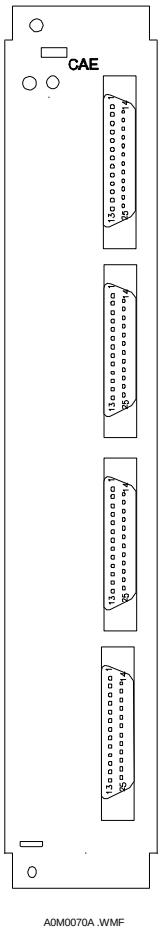


Fig. 14: Front Panel of CAE VF Interface Unit

Pin Usage for 20 x VF

	Upper Module		**Lower Module**	
Pin	J1	J2	J3	J4
1	[a]out1a	out6a	out11a	out16a
2	out1b	out6b	out11b	out16b
3	-	-	-	-
4	out2a	out7a	out12a	out17a
5	out2b	out7b	out12b	out17b
6	out3a	out8a	out13a	out18b
7	out3b	out8b	out13b	out18b
8	-	-	-	-
9	out4a	out9a	out14a	out19a
10	out4b	out9b	out14b	out19b

Pin Usage for 20 x VF

	Upper Module		**Lower Module**	
11	out5a	out10a	out15a	out20a
12	out5b	out10b	out15b	out20b
13	-	-	-	-
14	[b]in1a	in6a	in11a	in16a
15	in1b	in6b	in11b	in16b
16	-	-	-	-
17	in2a	in7a	in12a	in17a
18	in2b	in7b	in12b	in17b
19	in3a	in8a	in13a	in18b
20	in3b	in8b	in13b	in18b
21	-	-	-	-
22	in4a	in9a	in14a	in19a
23	in4b	in9b	in14b	in19b
24	in5a	in10a	in15a	in20a
25	in5b	in10b	in15b	in20b

a out = 4w output or 2w output/input

b in = 4w input

Pin Usage for 10 x VF + 10 x 2EM

	Upper Module		**Lower Module**	
Pin	J1	J2	J3	J4
1	[a]out1a	out6a	[b]e1a	e6a
2	out1b	out6b	e1b	e6b
3	-	-	ground	ground
4	out2a	out7a	e2a	e7a
5	out2b	out7b	e2b	e7b
6	out3a	out8a	e3a	e8b
7	out3b	out8b	e3b	e8b
8	-	-	ground	ground
9	out4a	out9a	e4a	e9a
10	out4b	out9b	e4b	e9b
11	out5a	out10a	e5a	e10a
12	out5b	out10b	e5b	e10b
13	-	-	ground	ground
14	[c]in1a	in6a	[d]m1a	m6a
15	in1b	in6b	m1b	m6b
16	-	-	ground	ground
17	in2a	in7a	m2a	m7a
18	in2b	in7b	m2b	m7b
19	in3a	in8a	m3a	m8b

Pin Usage for 10 x VF + 10 x 2EM

	Upper Module		**Lower Module**	
20	in3b	in8b	m3b	m8b
21	-	-	ground	ground
22	in4a	in9a	m4a	m9a
23	in4b	in9b	m4b	m9b
24	in5a	in10a	m5a	m10a
25	in5b	in10b	m5b	m10b

a out = 4w output or 2w output/input

b e = signalling output

c in = 4w input

d m = signalling input

Pin Usage for 5 x VF + 5 x 4EM

	Upper module		**Lower module**		
Pin	J1	J2	J3	J4	
1	[a]out1a	-	[b]e1a	e1c	
2	out1b	-	e1b	e1d	
3	-	-	ground	ground	
4	out2a	-	e2a	e2c	
5	out2b	-	e2b	e2d	
6	out3a	-	e3a	e3c	
7	out3b	-	e3b	e3d	
8	-	-	ground	ground	
9	out4a	-	e4a	e4c	
10	out4b	-	e4b	e4d	
11	out5a	-	e5a	e5c	
12	out5b	-	e5b	e5d	
13	-	-	ground	ground	
14	[c]in1a	-	[d]m1a	m1c	
15	in1b	-	m1b	m1d	
16	-	-	ground	ground	
17	in2a	-	m2a	m2c	
18	in2b	-	m2b	m2d	
19	in3a	-	m3a	m3c	
20	in3b	-	m3b	m3d	
21	-	-	ground	ground	
22	in4a	-	m4a	m4c	
23	in4b	-	m4b	m4d	
24	in5a	-	m5a	m5c	

Pin Usage for 5 x VF + 5 x 4EM

	Upper module		Lower module		
25	in5b	-	m5b	m5d	

a out = 4w output or 2w output/input

b e = signalling output

c in = 4w input

d m = signalling input

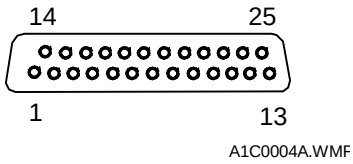


Fig. 15: D-type 25-pin female connector

6.2.6 Cabling for CAE Interface Unit

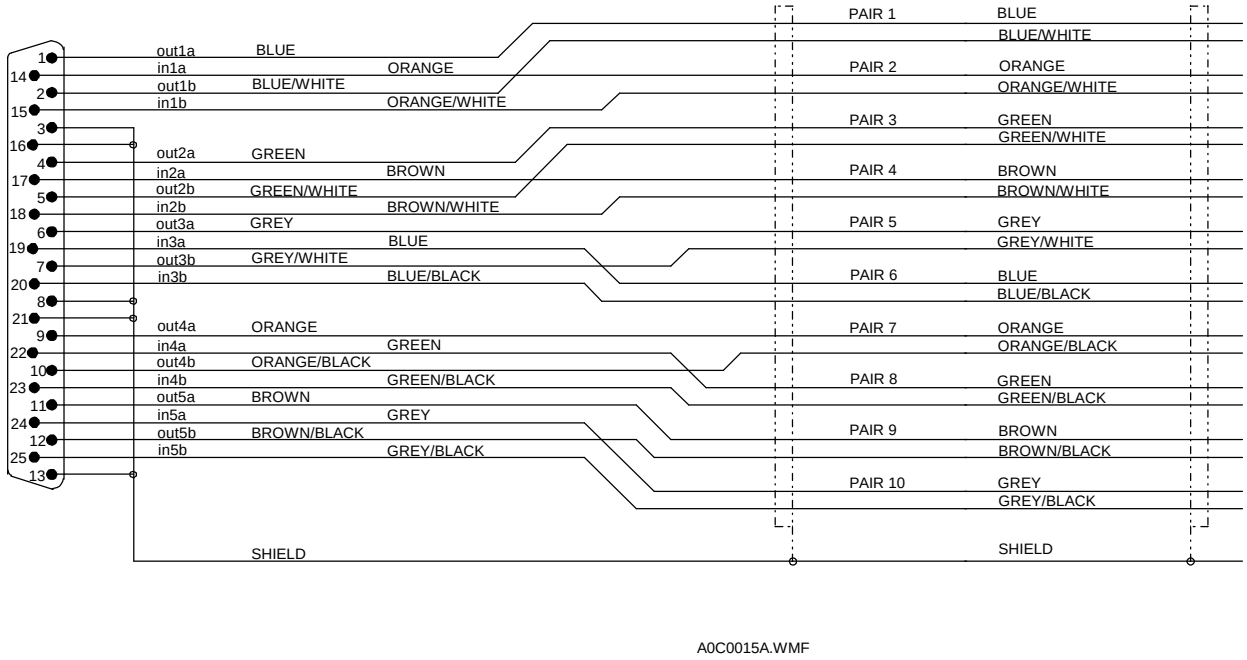


Fig. 16: Cable for CPP/CSE

6.2.7 G.704 Frame Structure Technical Specifications

2048 kbit/s Frame Structure

See Appendix A.

Multiframe Structure in the Signalling Time Slot

See Appendix A.

VF and Signalling in G.704

XB: VF Data	XD: CAS Signalling				EM Interface
64 kbits/s PCM	a	b	c	d	4 EM interfaces
64 kbits/s PCM	a	b	0	1	2 EM interfaces
32 kbit/s ADPCM	a	b[a]	-	-	2 EM interfaces
16 kbit/s ADPCM	a[a]	-	-	-	1 EM interfaces
24 kbit/s ADPCM	-	-	-	-	no EM interface

a Signalling bit is ADPCM processed in accordance with G.761

6.3 CCO and CCS Units

6.3.1 General

The unit pair CCO/CCS offers a connection of a PBX extension line through the DXX network. The CCO provides interfaces for up to 10 extension lines from the PBX. These lines can be routed through the DXX network to one or more CCS units. Each CCS provides interfaces for up to 10 subscriber telephone lines. A circuit from a CCS to another CCS can be created if a Hot Line feature is required.

A circuit in the DXX contains one interface in both CCO and CCS, and the connection between them. The connection is permanent, i.e. the DXX network does not function as a telephone switch. The circuit between the PBX and the subscriber transfers speech, calls, off-hook information, multifrequency dialing and loop disconnect dialing. The CCO has a software selectable voltage monitoring for the PBX line that is functional during on-hook. The CCO also detects overload condition during off-hook.

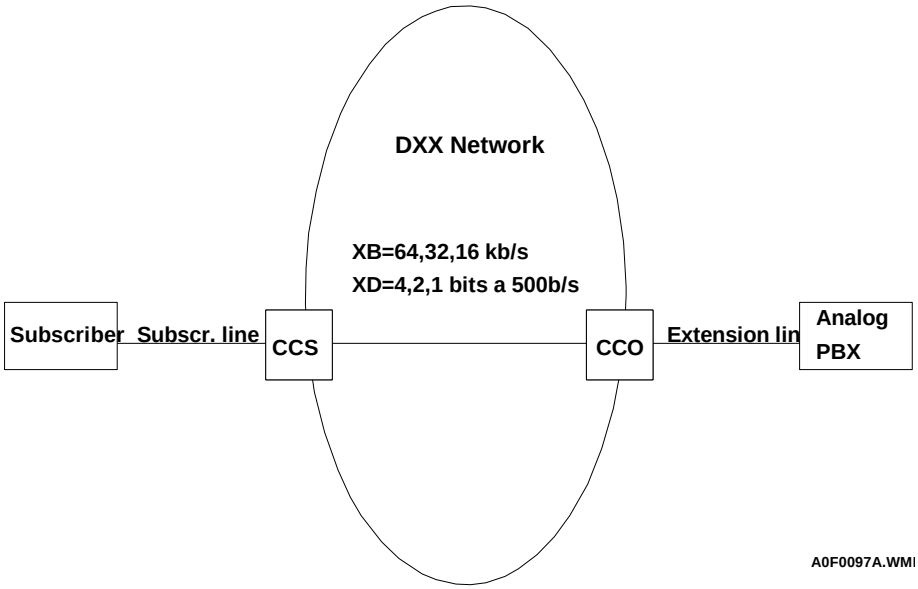


Fig. 17: PBX Extension Through DXX

6.3.2 Operation of CCO and CCS Units

6.3.2.1 Physical Structure

The CCO consists of a CAE 258 base unit and a CCZ 445 program memory. The CCO also has a power supply module PDF 202, an office interface module CCO 443 and a PCM codec CPP 492. If compression is required, the CPP 492 is replaced by an ADPCM converter CPP447.

The CCS consists of a CAE 227 base unit and a CCZ 445 program memory. The CCS has two power supply modules, PDF 202 and PDF 446. It also has a subscriber interface module CCS 444, a PCM codec CPP 493 and a filter module RCS 449. If compression is required, the CPP 493 is replaced by an ADPCM converter CPP 448.

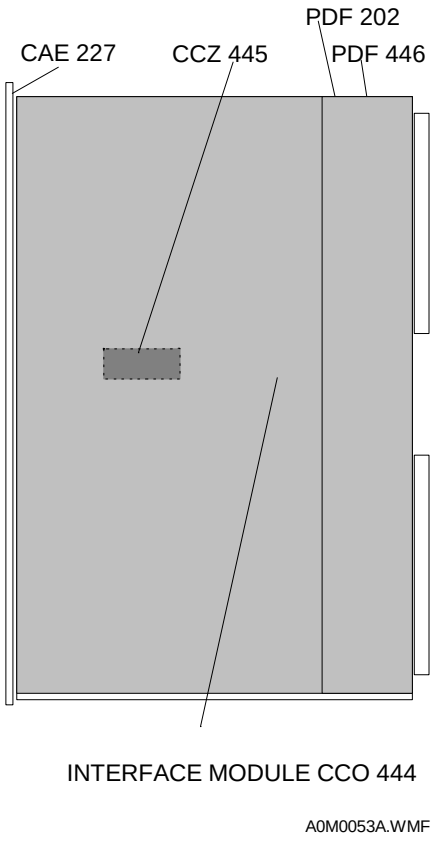


Fig. 18: CCS Unit

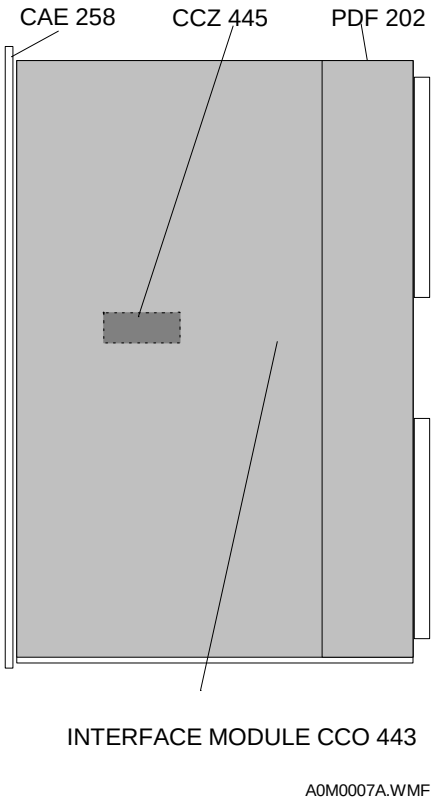


Fig. 19: CCO Unit

The dimensions for the CCO are 50 x 160 x 233 mm and for the CCS they are 73 x 160 x 233 mm. The front panels of both units house two alarm LEDs, a red and a yellow one, as well as a 25-pin, female D-connector (ISO2110). The back panels of the units hold two euro connectors. The upper one accesses the control bus and the lower one the 64 Mbit/s data cross-connection bus of the subrack (X-bus). The back panel connectors also provide battery voltage for the power supplies in both units.

Block Diagrams

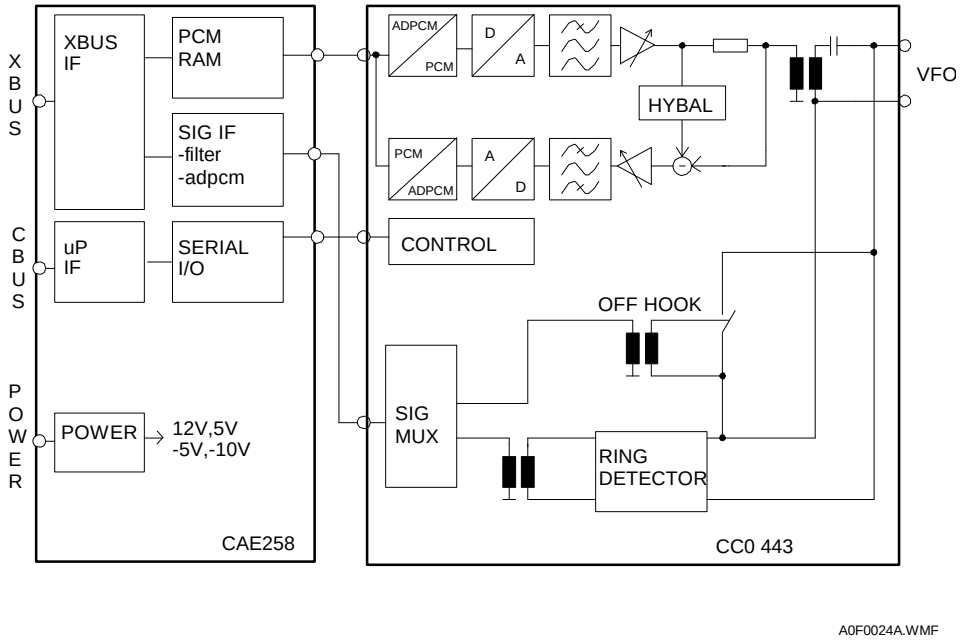


Fig. 20: CCO Block Diagram

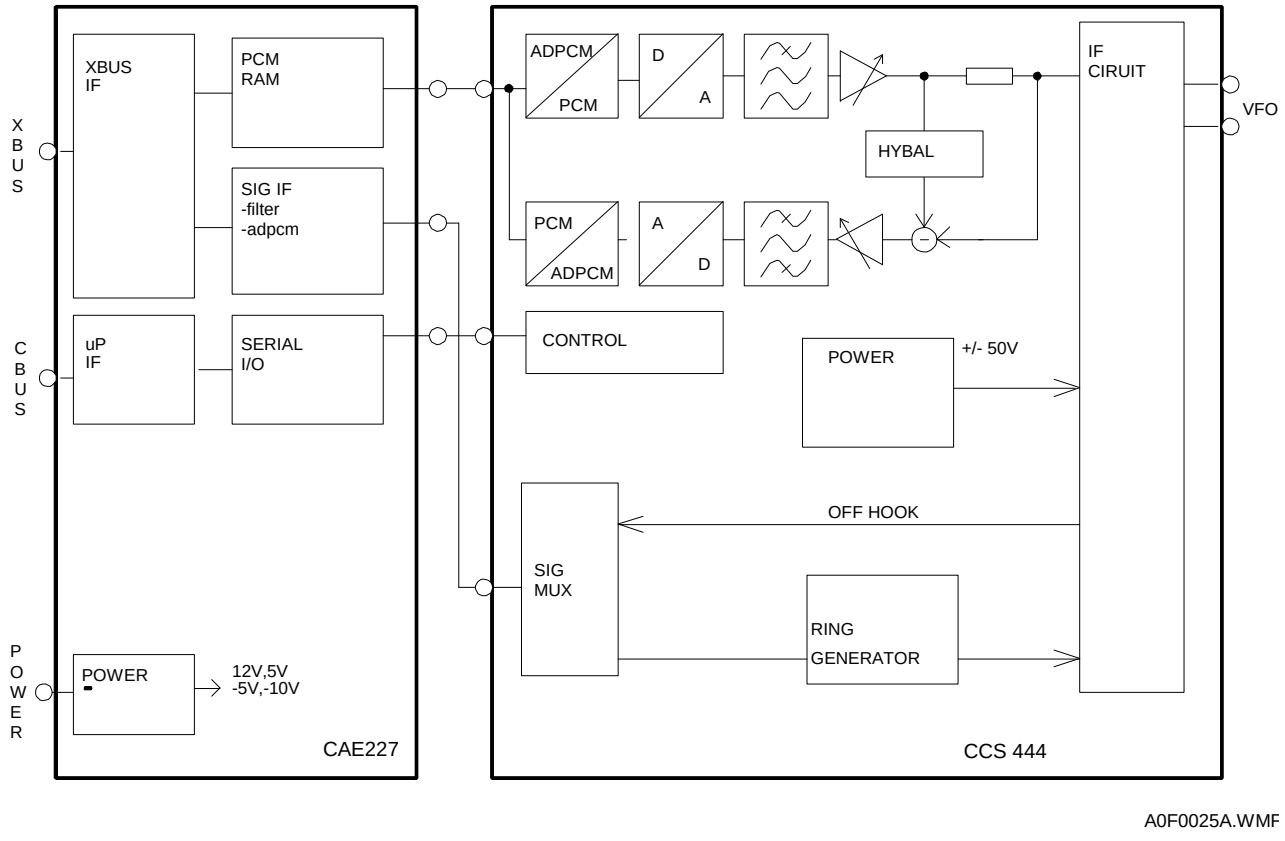


Fig. 21: CCS Block Diagram

6.3.2.2 Power Supply, CCO

A replaceable DC/DC unit power supply PDF 202 provides operation voltages 12, 5 and -10 V. A regulator generates -5 V from -10 V in CAE 258. The power supply operates directly on the station battery voltage that is supplied through the fuse unit (PFU) and through the back plane of the DXX subrack. The X-bus interface circuits are powered from the back plane of the subrack during the unit's start-up conditions. The operation voltages are continuously monitored by an A/D converter of the unit.

6.3.2.3 Power Supply, CCS

A DC/DC unit power supply PDF 446 attached to a CCS 444 provides operation voltages ± 50 V. In addition to that, a DC/DC unit power supply PDF 202 provides operation voltages 12, 5 and -10 V. A regulator generates -5 V from -10 V in CAE 227. The power supply operates directly on the station battery voltage that is supplied through the fuse unit (PFU) and through the back plane of the DXX subrack. The X-bus interface circuits are powered from the back plane of the subrack during the unit's start-up conditions. The logic operation voltages are continuously monitored by an A/D converter of the unit. With high voltages (± 50 V) only fault indication is available.

6.3.2.4 Unit Controller

Both units are controlled by an 80C188 microprocessor located in each CAE. The processor communicates with the other units of the subrack and with the service/management computers of the DXX network through a high-speed control bus interface (C-bus), including an HDLC controller. The basic unit software is stored in an interchangeable EPROM memory identified as CCZ 445. The application programs are stored in a non-volatile FLASH memory and can be downloaded.

6.3.2.5 Control Bus

The unit communicates with other units in the subrack via a subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to an SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus whenever there is no other traffic. When a unit is transmitting, it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by an SCU unit.

6.3.2.6 X-Bus Interface

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack; it is used to create clock frequencies for transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with a data bus DR2. The cross-connect unit decides with the aid of a Bus test which bus to use, and this information is supplied to other units through the control bus. From the cross-connect unit the CCO/CCS unit receives the time slot address which directs the bus data transmission to one selected time slot at a time.

The bus functions are also monitored by the interface units. When an interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm in case it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if the information is missing, the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

6.3.2.7 Loops

The NMS is able to control several loops in the CCO and CCS units. Loops are used to find a faulty section of the line and to calibrate the echo cancellation. All loops are loops back to X-bus, no loops are available back to interface.

There are three loop types available:

— digital loop DL whereby data is looped back transparently in a digital section of the base unit
— analog loop AL whereby data is looped back in an analog section of the interface chip in an interface module. ADPC-PCM-ADPCM conversion is included if the module supports that function. Loop gain is 0 dB.
— calibration loop CL which is used to measure the echo cancellation. The CL loop is also made in an analog section of the interface chip.

Each channel can be looped independently.

6.3.2.8 Relative Levels

The input relative levels are attenuation levels. If the input relative level in dBr is chosen equal to that of the analog input signal level in dBm (e.g. -4dBr and -4dBm), the digital signal level is 0dBm. In input the -4dBr results in 4dB amplification.

The output relative levels are amplification levels. If the digital signal level is 0dBm, the output relative level in dBr should be chosen equal to that of the desired analog output signal level in dBm, e.g -4dBr and -4dBm. In output the -4dBr results in 4dB attenuation.

6.3.2.9 Blocking

All channels can be blocked individually. When a channel is blocked, the VF data is attenuated and the signalling bits are set to blocking state values.

6.3.2.10 Power Feed For CCS Unit

The CCS unit must have a central battery DC feed.

NOTE! ***It is not allowed to use AC power supply (PAU unit) with the CCS.***

Restrictions

The CCO and CCS units are intended for use with station battery only.

The units support battery voltage range from 30 V to 60 V. A 24-V nominal battery is not supported.

The CCS unit draws up to 50 W from the battery bus. Therefore the maximum numbers of CCS units are as follows:

NOTE!

With PFU max. three (3) CCS units.

In case absolute minimum battery voltage of 40 V can be guaranteed with PFU, max. four (4) CCS units are allowed.

6.3.3 Modules for CCO and CCS Units

6.3.3.1 General

The PCM/ADPCM converter modules used in the CCO and CCS units are:

— CCO-ADPCM
— CCO-PCM
— CCS-ADPCM
— CCS-PCM

Voice Frequency Interface

The X-bus writes data into the PCM RAM using the VF interface address IA_VF and a time slot number (TS); the IA_VF is common for all VF channels. The PCM RAM is connected to the interface module through a 2-Mbit/s bus.

In the interface module there is one codec chip for each channel, and each chip picks the data from its own time slot in a 2-Mbit/s bus. If the module supports ADPCM/PCM conversion, there is a converter chip for each channel between the codec chip and the 2-Mbit/s bus.

Converter chips make the voice frequency compression which is selected by the NMS.

VF interfaces are equipped with circuitry to be connected to a PBX (CCO) or to an extension (CCS).

The µP configures the interface module using a serial I/O bus. The following parameters are independently programmable for each interface channel:

— G.761 (see Relevant Recommendations) processing for signalling bits during compression
— error filtering for signalling bits
— relative input/output levels 0.1 dB steps
— hybrid balance for test impedance
— VF coding: PCM or 16, 32 kbit/s ADPCM
— analog, digital or calibration loop back
— PBX voltage monitoring for CCO

The G.761 processing should be similarly configured throughout the connection.

6.3.4 Faults and Actions in CCO and CCS Units

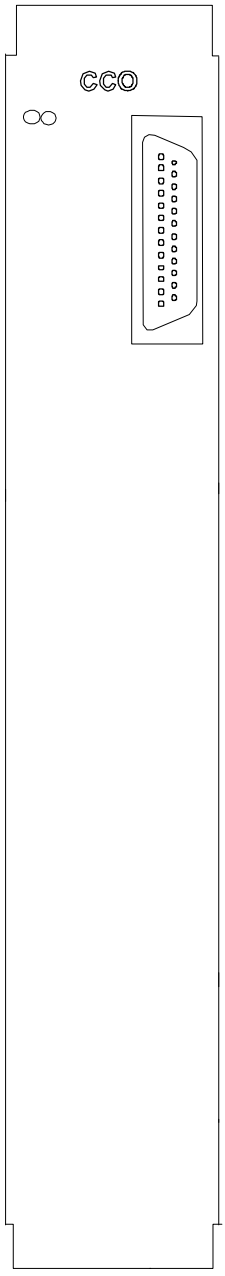
6.3.4.1 Fault Conditions

The following acronyms will be used in the table below:

PMA = Prompt Maintenance Alarm
S = Service Affecting Fault
MEI = Maintenance Event Information
R = Red alarm LED
Y = Yellow alarm LED

Fault Condition	Status	Front LEDs
Power supply		
+5 V, -5 V, +12 V, -10 V	PMA	R
+50 V, -50 V	PMA	R
+5 V back plane voltage	PMA	R
Memory faults		
RAM, EPROM fault	PMA, S	R
FLASH fault	PMA	R
Incompatible SW revisions	PMA, S	R
Check sum error		
- in FLASH memory	PMA, S	R
- in downloaded SW	PMA, S	R
Operation status faults		
Unit reset	PMA, S	R
Setup error	PMA, S	R
Conflict in module type	PMA, S	R
Start permission denied	PMA, S	R
Fault masking	MEI	Y
Interface operation		
IF loop to DXX	MEI, S	Y
IF blocked	MEI, S	Y
X-bus fault		
Timing fault	PMA, S	R
No interface activity (IA)	PMA, S	R
General faults		
ASIC error	PMA, S	R
Unit HW fault	PMA, S	R
Module type conflict	PMA, S	R
AIS from network	MEI, S	Y
PBX-related faults		
Overload	MEI, S	Y
Loss of PBX voltage	PMA, S	Y

6.3.5 Front Panel of CCS and CCO Units



A0M0072A.WMF

Fig. 22: Front Panel of CCO Unit

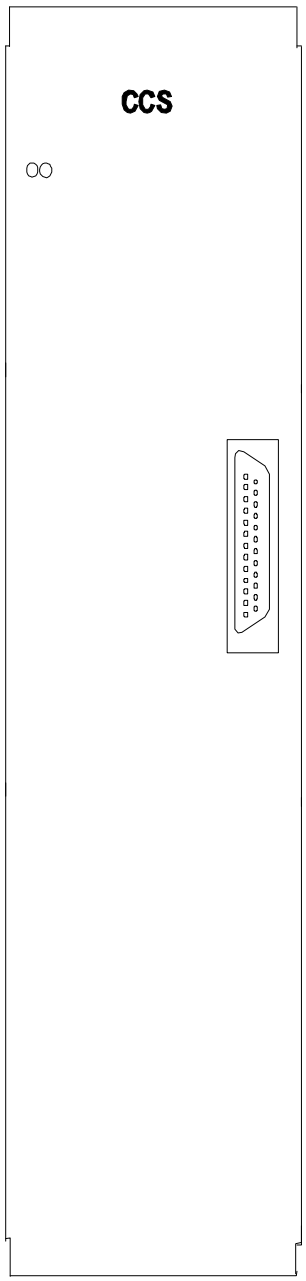


Fig. 23: Front Panel of CCS Unit

Pin Usage for CCO and CCS/ D-connector

Pin		Pin	
1	ch1a	14	ch6a
2	ch1b	15	ch6b
3	-	16	-
4	ch2a	17	ch7a
5	ch2b	18	ch7b
6	ch3a	19	ch8a
7	ch3b	20	ch8b
8	-	21	-
9	ch4a	22	ch9a
10	ch4b	23	ch9b
11	ch5a	24	ch10a
12	ch5b	25	ch10b
13	-		

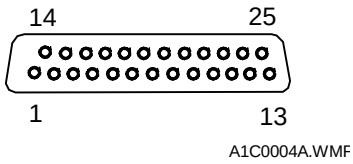


Fig. 24: D-type 25-pin female connector

6.3.6 Cabling for CCO and CCS Units

Cabling for both CCO and CCS unit must be provided by EricssonEricsson.

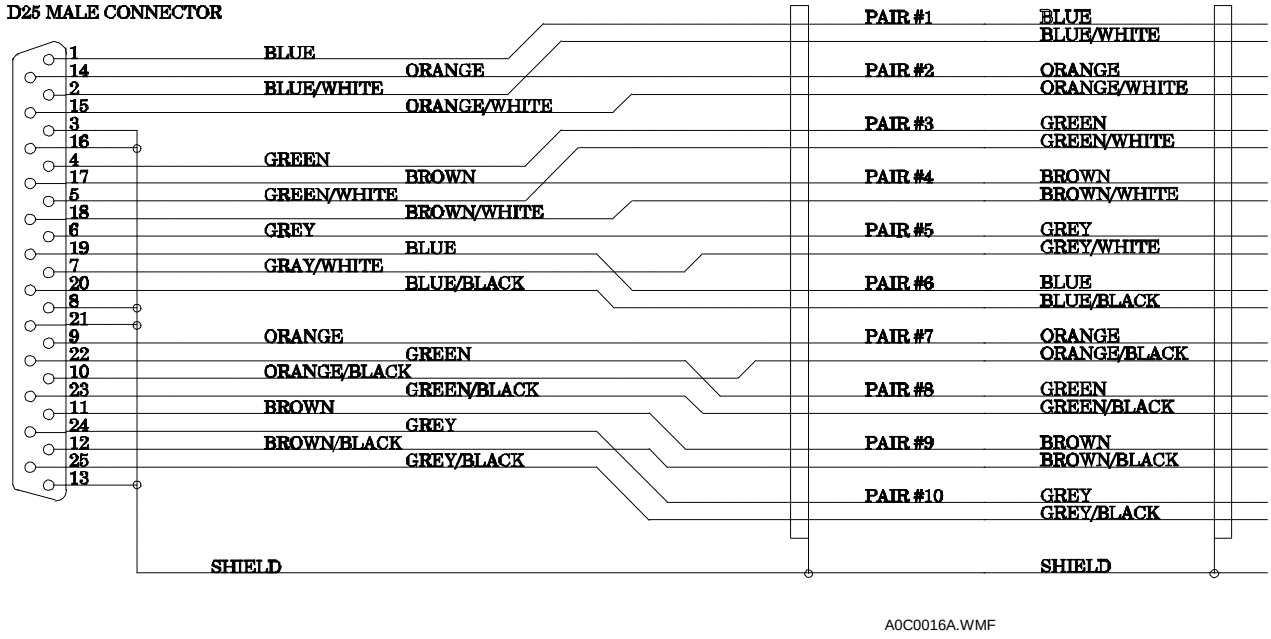


Fig. 25: Cabling for CCO and CCS Units

Cablepairs' numbering is different than channel numbering.

Numbering table

Pair number	Channel number
Pair#1	CH1
Pair#2	CH6
Pair#3	CH2
Pair#4	CH7
Pair#5	CH3
Pair#6	CH8
Pair#7	CH4
Pair#8	CH9
Pair#9	CH5
Pair#10	CH10

NOTE!

Make sure that CCS wires are not connected to ground. Do not install the phone between two different cablepairs.

If the phone is installed incorrectly, the CCS might seem to be working normally, conversation is possible and even ringing is passed, but the unit is getting hot and might stop working after a while.

6.3.7 Technical Specifications for Telephone Interfaces (CCO and CCS)

Transmission Characteristics

Number of channels per unit	10	
Type of encoding	64 kbit/s PCM (CCITT G.711 A-law) 16, 32 kbit/s ADPCM (ITU-T G.726)	
VF characteristics	G.712	
Nominal impedance	275 Ω + 850 Ω//150 nF	
Return loss 300Hz…600Hz	>15 dB	
Return loss 600Hz…3400Hz	> 20 dB	
Terminal balance return loss (TBRL)	> 20 dB	
Relative levels		
input	-12 dBr…+1 dBr	
output	-16 dBr…+1 dBr	
adjustability	0.1 dB/steps	
Longitudinal balance		
CCO	> 50 dB	
CCS	> 40 dB	
Out-of-band signals at channel output	< -30 dB	
Absolute channel delay @ 1 kHz		
VF to PCM	< 700 µs	
PCM to VF	< 700 µs	
PCM to ADPCM	< 400 µs	
ADPCM to PCM	< 400 µs	
Total distortion (CCITT G.712/G.713 method 1)		
64 kbit/s PCM	G.712	
Idle channel noise		
64 kbit/s PCM	< -75 dBmOp	
Noise in conversation state	CCO	CCS
input	< -66 dBmOp	< -64 dBmOp
output	< -75 dBmOp	< -67 dBmOp

DC Characteristics For Extension Unit, CCS

Voltage feed	
quiescent condition	48 Vdc + 20 %/-15 %
Current feed	
off-hook condition	48/(1650 + R) A min. 52/(1550 + R) A max. (R = 0…1800)
short circuit between a, b and earth, any combination	150 mA max.
Extension line resistance	
loop resistance including a telephone set in off-hook condition	1800 Ω max.

Signalling Characteristics For Extension Unit, CCS

Signalling states detection	
on-hook condition loop current	3 mA max.
off-hook condition loop current	10 mA min.
multifrequency signalling	transparently to PBX
loop disconnect signalling	supported
Ringing signal	
frequency	25 Hz ± 4 %
distortion	10 % THD
voltage:	
no load	75 V rms. max.
at terminals across 5.2 kW	52 Vrms. min.

Loop Termination for PBX Unit, CCO

PBX line interface	
high-ohmic condition	1 MΩ min.
low-ohmic condition	350 Ω max.
ringing signal detector impedance at 25 Hz	8 kΩ min
loop DC current	13 mA min. 40 mA max.

Signalling Characteristics for PBX Unit, CCO

ringing signal to be detected	30 V rms. min.
ringing signal frequency	25 Hz ± 12%
50 Hz ringing signal detection	supported
ringing signal not to be detected	10 V rms. max.

6.4 CCO-UNI Interface Unit

6.4.1 General Information

With plain old telephone system (POTS) interface units, an operator can build a voice connection from a private branch exchange (PBX) or local exchange (LE) through the DXX™ system into analog telephone terminal equipment.

The 30-channel CCS-UNI unit is used as an interface between analog telephone terminals and DXX network. If the analog connection is desired also for PBX, the CCO-UNI unit supports up to 30 analog extension lines from the PBX towards DXX network.

The connection through the DXX network is permanent: the DXX system does not function as a telephone switch. POTS interface units are fully integrated with the powerful DXX Network Management System (NMS).

6.4.2 Operation

6.4.2.1 Supported Features

The following analog office line interface's features are supported with CCO-UNI unit:

1. Transmitting of on-hook and off-hook condition
2. Termination of line current
3. Transmitting of pulse dialling
4. Detection of polarity reversal
5. Detection of ringing voltage
6. Detection of 12 or 16 kHz metering pulses, programmable frequency
7. Programmable level of metering sensitivity
8. Transmitting and receiving of voice frequencies with a 2 wire / 4 wire hybrid
9. Programmable receiving and transmitting levels of voice frequencies
10. Programmable line termination impedance
11. Calling line identification (CLI)
12. Over voltage protection

6.4.2.2 Mechanical Design

The mechanical design of CCO-UNI units is based on standard DXX system mechanics. The units can occupy any card slot in the subrack; however, general recommendations for subrack equipping should be followed. CCO-UNI unit is 10T (50.8 mm) wide.

— The CCO-UNI unit is build up by PBU560 control processor module, PDF553 power supply and two CCO555 subscriber line interface modules. Line interface modules are connected to control processor through power supply card PDF553, which delivers all operating voltages to unit. Unit is connected into the DXX subrack's X-bus through connectors at the rear edge of the PBU560. See Fig. 26.

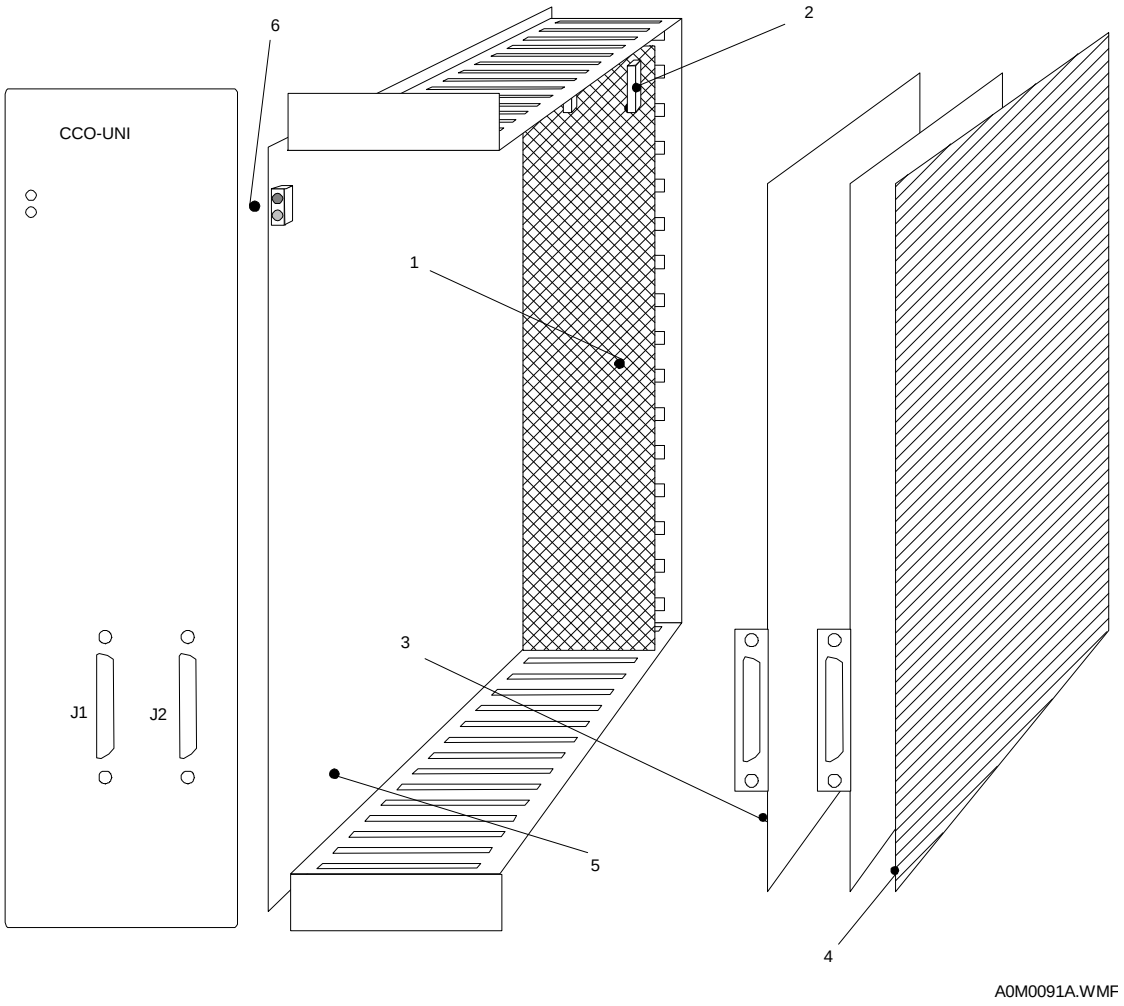


Fig. 26: Mechanical Structure of CCO-UNI

1. Power supply module PDF553
2. Connectors to subscriber line interface modules CCO555
3. Subscriber line interface modules (2 pcs) CCO555
4. EMC shielding plate
5. Control processor module PBU560
6. Alarm LEDs, upper red and lower yellow

The unit front panel houses two alarm LEDs and two subscriber lines interface connectors.

6.4.2.3 Block Diagram

See block diagram of CCO-UNI in Fig. 27 below.

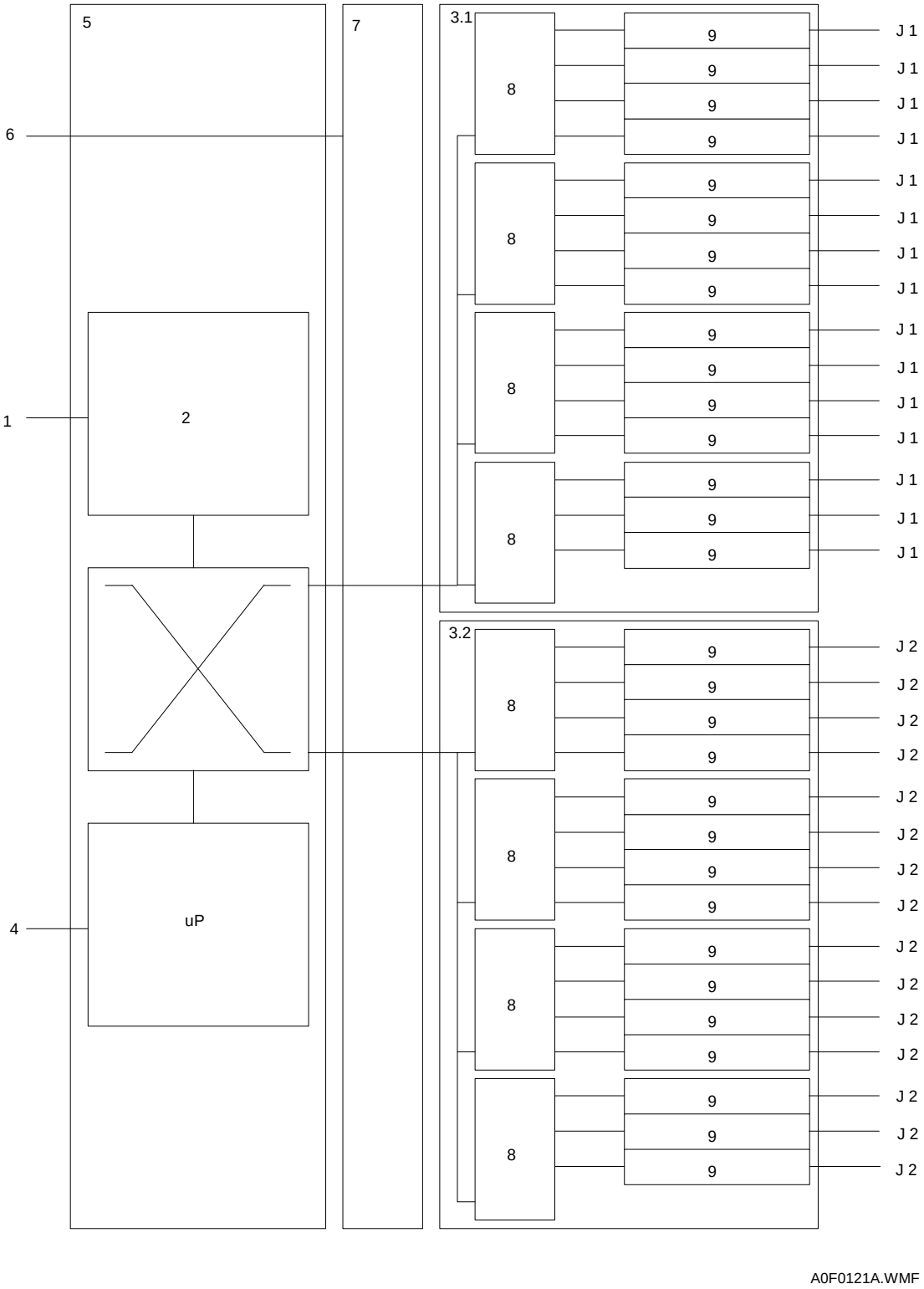


Fig. 27: Functional Structure of CCO-UNI

1. Cross connection bus (X-bus)
2. X-bus interface
3. 3.1 and 3.2 CCO555 office line interface modules
4. Control bus (C-bus)
5. Control processor module PBU560
6. Battery bus (B-bus)
7. Power supply module PDF553 delivering +5 V, +12 V, -10 V and –22 V
8. Four channel coder – decoder
9. Office line interface circuit

J 1 and J 2 front panel connectors

The main functional blocks of the unit include power supply, control processor module, two subscriber line interface modules and an X-bus interface.

Power supply delivers all operating voltages for unit from battery-bus. Control processor module handle signalling, monitors unit's state and reports faults to NMS. Unit's interface modules implement analog interfaces. Interface modules deliver control channels to control processor and bearer-channels have static cross-connection to X-bus.

6.4.3 Interface modules

Unit CCO-UNI uses two interface modules CCO555. Module CCO555 behind front plate connector J1 delivers channels 1 to 15 and module behind J2 channels 16 to 30. One CCO-UNI unit carries total 30 office line interfaces.

6.4.4 Faults

6.4.4.1 Fault table

The fault table is described here and the table should be updated here as required. The format of the table mirrors the format of the fault array structure in the software, with an additional field for the explanation of the fault.

The fields are interpreted as follows:

Name: Name of fault condition.
Sever: Major, Minor or Warning.
Status: PMA, DMA or MEI.
Srv: An S in this column means the alarm is a service alarm.
Led R: for Red (upper in front plate), Y for Yellow (lower in front plate).
Blk Block: number (defined below).
GPT: General problem type, see [6].
SPT: Specific problem type.
Description: A comment.

The block number defines the source of the fault according to the following table.

Block 0: Common Block
Blocks 1 – 30: The interfaces

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
Unpredicted fault condition	Major	PMA	-	R	0	1	1	This fault condition should never occur (or not yet supported).
Software error	Major	PMA	-	R	0	1	2	Software has noted an inconsistency in its own logic.
Software error in Signalling Controller	Major	PMA	-	R	0	1	3	The main processor has received an unknown message from the Signalling Controller.
Reset	Major	PMA	S	R	0	2	4	There has been a unit reset (detected always after the power-up of the unit).
Reset in Signalling Controller	Major	PMA	S	R	0	2	5	There has been a reset in the Signalling Controller (detected always after the power-up of the unit).
Setup error	Major	PMA	S	R	0	3	6	One of the setting structures has been corrupted in the non-volatile memory.
Power supply +5 V (subrack)	Major	PMA	-	R	0	4	7	The voltage is below the threshold limit (about 4.6 V depending on the calibration and the A/D resolution).
Power supply +5 V	Major	PMA	-	R	0	4	8	The voltage is below the threshold limit (about 4.6 V depending on the calibration and the A/D resolution).
Power supply +12 V	Major	PMA	-	R	0	4	9	The voltage is below the threshold limit (about 11.3 V depending on the calibration and the A/D resolution).
Power supply -10 V	Major	PMA	-	R	0	4	10	The voltage is above the threshold limit (about -9.0 V depending on the calibration and the A/D resolution).
Power supply -20 V	Major	PMA	-	R	0	4	11	The voltage is above the threshold limit
RAM fault	Major	PMA	S	R	0	5	12	A background process has detected a RAM location where the read value does not match with the written test pattern.
RAM fault in Signalling Controller	Major	PMA	S	R	0	5	13	A background process in the Signalling Controller has detected a RAM location where the read value does not match with the written test pattern.
PROM fault	Major	PMA	S	R	0	5	14	The calculated check sum does not match with the stored one.
Flash write error	Major	PMA	S	R	0	5	15	Error during writing to the flash memory (main bank).
Flash copy error	Major	PMA	S	R	0	5	16	Error during writing to the flash memory (shadow bank).
Flash erase error	Major	PMA	S	R	0	5	17	Error during erase of the flash memory (shadow bank).
Flash duplicate error	Major	PMA	S	R	0	5	18	Duplicated parameters (same ID) detected during start-up.

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
Flash shadow error	Major	PMA	S	R	0	5	19	The shadow bank of the flash is not erased during start-up.
Flash checksum error	Major	PMA	S	R	0	5	20	The calculated check sum does not match with the stored one.
Flash fault in Signalling Controller	Major	PMA	S	R	0	5	21	The Signalling Controller has detected an error in its own flash memory.
Missing module 1	Major	PMA	S	R	0	10	22	The interface module defined in the settings is missing.
Missing module 2	Major	PMA	S	R	0	10	23	The interface module defined in the settings is missing.
Conflict in module type 1	Major	PMA	S	R	0	10	24	There is a conflict between the installed module and the settings.
Conflict in module type 2	Major	PMA	S	R	0	10	25	There is a conflict between the installed module and the settings.
Loss of multiframe sync	Major	PMA	S	R	0	25	26	Loss of multiframe synchronization state detected by the Signalling Controller
ASIC fault in base unit	Major	PMA	S	R	0	32	27	The fault is activated if difference between write/read configuration data of ASIC has been detected.
Start permission denied	Major	PMA	S	R	0	36	28	Most likely the unit does not belong to the node configuration.
Bus sync fault	Major	PMA	S	R	0	38	29	No DXX bus synchronization from SXU detected.
IA activity missing	Major	PMA	S	R	0	40	30	The interface address is not activated on the cross-connection bus by the SXU.
Missing or incompatible application program	Major	PMA	S	R	0	55	31	There is no downloaded software in flash or the revision is wrong.
Checksum error in downloaded SW	Major	PMA	S	R	0	55	32	The downloaded software has been corrupted.
HW fault in base unit	Major	PMA	S	R	0	62	33	Base unit hardware does not work as expected.
Strapping conflict	Major	MEI	-	R	0	62	34	The strapping info of the base unit PCB is not what the software expects. Maybe the software is installed on a wrong unit.
HW fault in module 1	Major	PMA	S	R	0	62	35	Module hardware does not work as expected.
HW fault in module 2	Major	PMA	S	R	0	62	36	Module hardware does not work as expected.
No response from Signalling Controller	Major	PMA	S	R	0	62	37	A timeout occurred when waiting response from the Signalling Controller.
Error message from Signalling Controller	Major	PMA	S	R	0	62	38	The Signalling Controller returned an error to test message (other than RAM or flash error).
Setup conflict	Major	DMA	-	R	0	69	39	Information stored to setup is self-contradictory.
Interface loop to net	Warn	MEI	S	Y	1-30	27	40	An interface loop is created in the interface module. It loops transmitted data back to the interface receiver.

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
Equipment loop to net	Warn	MEI	S	Y	1-30	27	41	Similar to Interface loop except that the loop is made before the interface module on the PBU base card.
Line loop to user	Warn	MEI	S	Y	1-30	27	42	Rx-data is looped back to the interface transmitter.
AIS from Network	Warn	MEI	S	Y	1-30	42	43	AIS is detected from DXX Network.
Faults masked	Warn	MEI	-	Y	1-30	58	44	The fault is activated when interface Fault mask setting is on (all interface faults are cleared).
Fault in interface	Major	PMA	S	R	1-30	62	45	Line interface does not work as expected.
IF blocked off	Warn	MEI	S	-	1-30	63	46	The interface has been blocked from the use.
Filter coefficients missing	Warn	MEI	-	Y	1-30	69	47	The coefficients of the Signal Processing Codec Filter (SICOFI) are missing. Default coefficients are used.

6.4.5 Front Panel

See front panel of CCO-UNI unit in Fig. 28 below.

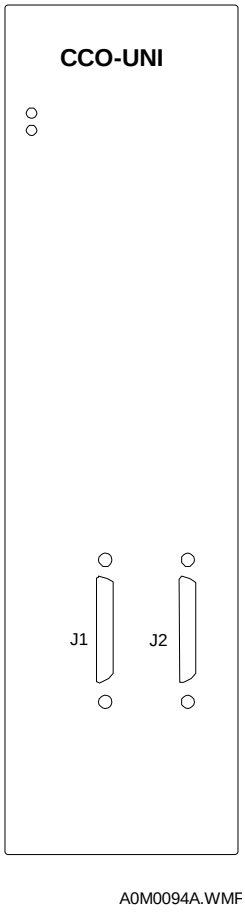


Fig. 28: Front Panel of CCO-UNI

Allocation of subscriber line interfaces is the following: Lines 1 to 15 connector J1 and lines 16 to 30 connector J2.

A 50-pin SCSI II style connector is used in front panel of CCO-UNI. See Fig. 29 below for numbering.

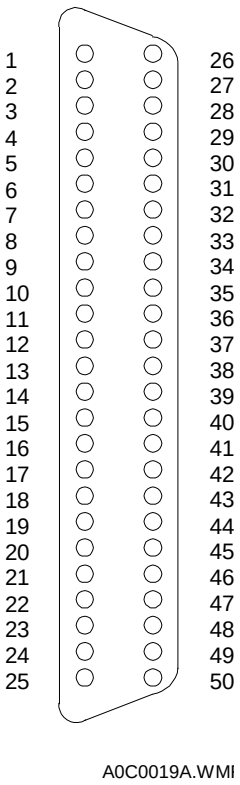


Fig. 29: Front Panel Connector of CCO-UNI, Front View

Numbering of Connector J1

Connector J1 pin number	Channel number at J1	Connector J1 pin number	Channel number at J1
1	GROUND	26	GROUND
2	1 TIP	27	9 TIP
3	1 RING	28	9 RING
4	GROUND	29	GROUND
5	2 TIP	30	10 TIP
6	2 RING	31	10 RING
7	GROUND	32	GROUND
8	3 TIP	33	11 TIP
9	3 RING	34	11 RING
10	GROUND	35	GROUND
11	4 TIP	36	12 TIP
12	4 RING	37	12 RING
13	GROUND	38	GROUND
14	5 TIP	39	13 TIP
15	5 RING	40	13 RING
16	GROUND	41	GROUND

Numbering of Connector J1

Connector J1 pin number	Channel number at J1	Connector J1 pin number	Channel number at J1
17	6 TIP	42	14 TIP
18	6 RING	43	14 RING
19	GROUND	44	GROUND
20	7 TIP	45	15 TIP
21	7 RING	46	15 RING
22	GROUND	47	GROUND
23	8 TIP	48	-
24	8 RING	49	-
25	GROUND	50	GROUND

Note 1: Each channel uses two connector pins because of two connected wires; Tip and Ring.

Numbering of Connector J2

Connector J2 pin number	Channel number at J2	Connector J2 pin number	Channel number at J2
1	GROUND	26	GROUND
2	16 TIP	27	24 TIP
3	16 RING	28	24 RING
4	GROUND	29	GROUND
5	17 TIP	30	25 TIP
6	17 RING	31	25 RING
7	GROUND	32	GROUND
8	18 TIP	33	26 TIP
9	18 RING	34	26 RING
10	GROUND	35	GROUND
11	19 TIP	36	27 TIP
12	19 RING	37	27 RING
13	GROUND	38	GROUND
14	20 TIP	39	28 TIP
15	20 RING	40	28 RING
16	GROUND	41	GROUND
17	21 TIP	42	29 TIP
18	21 RING	43	29 RING
19	GROUND	44	GROUND
20	22 TIP	45	30 TIP
21	22 RING	46	30 RING
22	GROUND	47	GROUND
23	23 TIP	48	-
24	23 RING	49	-
25	GROUND	50	GROUND

Note 1: Each channel uses two connector pins because of two connected wires; Tip and Ring.

6.4.6 Unit Cabling

CCO-UNI unit's channels can be connected to subscriber line cross-connection panel with cable 838117242B POTS-UNI 10 m. See figure Fig. 30. Two cables are needed for each CCO-UNI unit.

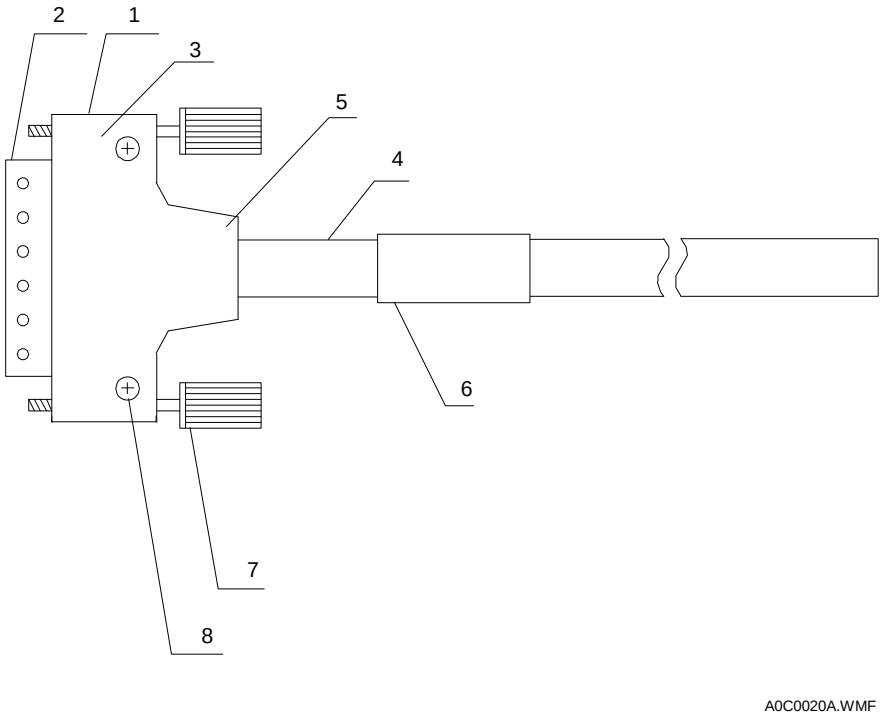


Fig. 30: Cable POTS-UNI 838117242B

1. AMP 749080-1 Shielded Backshell Kit with Jackscrews
2. AMP 749110-1 Cable Plug Connector
3. AMP 749108-4 Termination Cover, inside, 2 pcs
4. Madison 34ZDK00001 Cable, 17 pair, stranded 28 AWG, 100 W, 10 m
5. Strain Relief, inside
6. Marking: 838117242B POTS-UNI CABLE 10 m
7. Jackcrews, 2 pcs
8. Machine Screws, 2 pcs

6.4.6.1 Numbering of Cable Plug

See Fig. 31 below for unit cable plug's numbering:

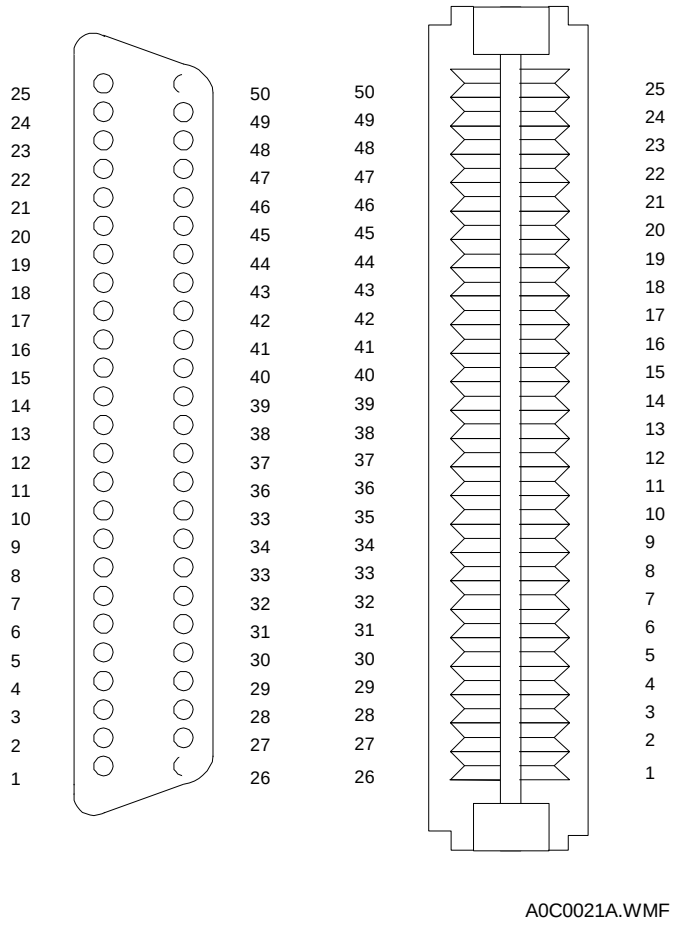


Fig. 31: POTS-UNI 838117242B Cable plug's numbering; Connector Pin Side and Termination Side

6.4.6.2 Numbering of Channels in Unit Cabling

Cable Connected to Connector J1

Subscriber line interface channels 1 to 16 are numbered in a cable connected to connector J1 as follows:

Interface Channel	Pair of Cable	Connector J1 Pins	Colour Coding of Wires
1	1	2,3	White/Black paired with Black/White
2	2	5,6	White/Brown paired with Brown/White
3	3	8,9	White/Red paired with Red/White
4	4	11,12	White/Orange paired with Orange/White
5	5	14,15	White/Yellow paired with Yellow/White
6	6	17,18	White/Green paired with Green/White
7	7	20,21	White/Blue paired with Blue/White
8	8	23,24	White/Violet paired with Violet/White
9	9	27,28	White/Grey paired with Grey/White
10	10	30,31	Black/Brown paired with Brown/Black
11	11	33,34	Black/Red paired with Red/Black
12	12	36,37	Black/Orange paired with Orange/Black
13	13	39,40	Black/Yellow paired with Yellow/Black
14	14	42,43	Black/Green paired with Green/Black
15	15	45,46	Black/Blue paired with Blue/Black
-	16	48,49	Black/Violet paired with Violet/Black
Ground	17	25,50	Black/Grey paired with Grey/Black

Cable Connected to Connector J2

Subscriber line interface channels 17 to 30 are numbered in a cable connected to connector J2 as follows:

Interface Channel	Pair of Cable	Connector J2 Pins	Colour Coding of Wires
16	1	2,3	White/Black paired with Black/White
17	2	5,6	White/Brown paired with Brown/White
18	3	8,9	White/Red paired with Red/White
19	4	11,12	White/Orange paired with Orange/White
20	5	14,15	White/Yellow paired with Yellow/White
21	6	17,18	White/Green paired with Green/White
22	7	20,21	White/Blue paired with Blue/White
23	8	23,24	White/Violet paired with Violet/White
24	9	27,28	White/Grey paired with Grey/White
25	10	30,31	Black/Brown paired with Brown/Black
26	11	33,34	Black/Red paired with Red/Black
27	12	36,37	Black/Orange paired with Orange/Black
28	13	39,40	Black/Yellow paired with Yellow/Black
29	14	42,43	Black/Green paired with Green/Black
30	15	45,46	Black/Blue paired with Blue/Black
-	16	48,49	Black/Violet paired with Violet/Black
Ground	17	25,50	Black/Grey paired with Grey/Black

6.4.7 Technical Specifications

6.4.7.1 Transmission Characteristics of CCO-UNI

Type of encoding 64 kbit/s PCM (ITU-T G.711 A-law)

Nominal impedance 600W, 200W+820W//115nF and 275W+850W//150 nF impedances are software selectable. List of impedances is possible to expand if needed.

Return loss

Per ITU-T Q.552 01/94 figure 1

Terminal balance return loss (TBRL)

Per ITU-T Q.552 01/94 figure 11, typical value over 30 dB at 1 kHz

Relative levels

72 different input and output level pair in regions

Input -6 dBr.....+3 dBr (attenuation from analog to DXX)

Output -9 dBr .....+1 dBr (gain from analog to DXX)

Longitudinal balance Minimum >40 dB, Typical >46 dB at 1kHz

Attenuation/frequency distortion in analog to DXX and DXX to analog. 0 dB level is set at frequency point 1020 Hz.

Frequency	minimum loss	maximum loss
0...200 Hz	0 dB	no limit
200...300 Hz	-0.30 dB	no limit
300...400 Hz	-0.30 dB	1.0 dB
400...600 Hz	-0.30 dB	0.75 dB
600...2400 Hz	-0.60 dB	0.35 dB
2400...3000 Hz	-0.60 dB	0.55 dB
3000...3400 Hz	-0.60 dB	1.5 dB
3400...3600 Hz	-0.60 dB	no limit
Frequency >3600 Hz	0 dB	no limit

Variation of gain with input level

Per ITU-T Q.552 01/94 figure 5

Signal-to-total distortion ratio

Encoding and decoding side per ITU-T Q.552 01/94 figure 14

Idle channel noise

Per ITU-T Q.552 01/94 sections Input connection and Output connections

6.4.7.2 Length of Office Line

CCO-UNI unit supports operation with **a short line length only**.
Limiting factor for the line length between PBX or LE and CCO-UNI unit is earth potential difference between devices. **Maximum difference between earth potentials is 15 Vpeak AC at 50 Hz or 60 Hz**. When CCO-UNI is installed in the same premises with the PBX or LE this does not usually form any limitation.

6.4.7.3 DC Characteristics

Reversal of line current is supported.

On-Hook condition: Less than 0.5 mA DC bleeding current.

Off-Hook condition: Constant voltage nominal 12 V between tip and ring terminals. Line current is determined according to PBX's or LE's feeding bridge. Off-Hook operating loop current range is from 8 mA to 100 mA (max). Nominal Off-Hook loop current is 40 mA.

6.4.7.4 Ringing

Ringing signal detector impedance at 25 Hz is 100 kW min.
Detecteing ringing signal frequency 20 Hz, 25 Hz or 50 Hz.
Detecting and not detecting voltages with 48 V superimposed battery at 25 Hz:
Detecting voltage is 28 Vrms minimum, not detecting voltage is 18 Vrms maximum.

6.4.7.5 Metering

Metering pulse frequency 12 kHz or 16 kHz nominal, software selectable from NMS
Metering pulse duration over 80 ms
Metering pulses repetition frequency between CCO-UNI, CCS-UNI is 2.4 Hz maximum
Metering pulse termination impedance 200 W nominal
Metering pulse detection level is software selectable from NMS as indicated in a table below:

Sensitivity setting	12.00 kHz not detecting	12.00 kHz detecting	16.00 kHz not detecting	16.00 kHz detecting
1	183 mV	302 mV	209 mV	364 mV
2	136 mV	207 mV	157 mV	247 mV
3	97 mV	151 mV	113 mV	181 mV
4	63 mV	98 mV	72 mV	118 mV
5	48 mV	77 mV	56 mV	91 mV
6	35 mV	61 mV	39 mV	71 mV
7	24 mV	46 mV	26 mV	54 mV
8	17 mV	34 mV	21 mV	40 mV
9	12 mV	24 mV	15 mV	29 mV
10	9 mV	19 mV	12 mV	24 mV
11	8 mV	16 mV	10 mV	21 mV
12	6 mV	12 mV	8 mV	17 mV

Voltage readings in the table above represent typical values on one of two centre operating frequencies (12.00 kHz or 16.00 kHz). Sensitivity is highest at these frequencies. The sensitivity is given as rms values at one of channel's input terminals (TIP, RING) of CCO-UNI unit. If input metering pulse's voltage level is between values detecting and not detecting, it may be detected or rejected.

6.4.7.6 Caller Identification

CCO-UNI is capable to transmit caller identification during On-Hook.

6.4.7.7 Power Supply Requirements

Input voltage –48 VDC, range –40.5 V to –60.0 V pRETS 300 132-2 May 1996.

Maximum input power 20 W

Subrack's Power Supply Unit

A DC-feeding power supply unit (PFU) is required in a DXX subrack carrying CCO-UNI units.

However, it is possible to use an AC power supply PAU-5T or PAU-10T with CCO-UNI. Power supply units PAU or PAU-15T are not possible to use. When an AC power supply unit is used, the subrack of the node must be permanently grounded according to safety regulations.

6.4.7.8 Electromagnetic Compatibility

Test has been performed according to ETSI 300 386-1: December 1994, table 4: Public telecommunications equipment, locations other than telecommunication centres. Normal priority of service.

Immunity:

Test	Coupling	Standard	Test level / Compliance criterion	Result	Remarks
ESD (ElectroStatic Discharge)	Enclosure	EN 61000-4-2	3 (6 kV & 8 kV) / NP 4 (8 kV & 15 kV)/ LFS	NP	
EFT (Electrical Fast Transient)	Signal	EN 61000-4-4	2 (500 V)/ NP 3 (1 kV)/ LFS	NP	
Surge	Outdoor signal	K.21/table 1, No 1	1 kV / 1,5 kV / LFS 4 kV/LFS	OK	a
Conducted RF	AC & DC power & signal	EN 61000-4-6	2 (3 V)/ NP 3 (10 V)/RP	NP	

a 4 kV level only to be applied when primary protection is fitted.

NP: Normal Performance

RP: Reduced Performance

LFS: Loss of Function (Self recovery)

Statement of conformity: CCO-UNI unit with cable 838117242B POTS-UNI 10 m installed into a DXX node fulfil the essential requirements of the European telecommunication standard ETS 300 386-1.

6.4.7.9 Environmental Specifications

Unit is intended to be used in telecommunication equipment premises.

Environmental operating conditions: ETS 300 019-1-3 Class 3.1; 1992

(Combination of IEC 721-3-3 classes 3K3/3B1/3C2/3S2/3M1)

Condition

normal operating conditions +5º+40 oC, < 85 % RH, non-condensing

exceptional operating conditions -5º +45 oC < 90 % RH, non-condensing

6.4.7.10 System Alternatives

Refer to Chapter 6.5.7.9

6.4.7.11 Thee bit-CAS Signalling

Refer to Chapter 6.5.7.10

6.5 CCS-UNI Interface Unit

6.5.1 General Information

With plain old telephone system (POTS) interface units, an operator can build a voice connection from a private branch exchange (PBX) or local exchange (LE) through the DXX™ system into analog telephone terminal equipment.

The 30-channel CCS-UNI unit is used as an interface between analog telephone terminals and DXX network. If the analog connection is desired also for PBX, the CCO-UNI unit supports up to 30 analog extension lines from the PBX towards DXX network.

The connection through the DXX network is permanent: the DXX system does not function as a telephone switch. POTS interface units are fully integrated with the powerful DXX Network Management System (NMS).

For alternative ways to build a system using CCS-UNI please see Chapter 6.5.7.9, System Alternatives.

For Channel Associated Signalling between CCS-UNI and CCO-UNI please see Chapter 6.5.7.10, Three Bit CAS-Signalling.

6.5.2 Operation

6.5.2.1 Supported Features

The following analog subscriber line interface's features are supported with CCS-UNI unit:

1. Detection of on-hook and off-hook condition
2. Generation of line length adaptive loop current
3. Detection of pulse dialling
4. Transmitting of polarity reversal
5. Loop current enabling and disabling
6. Transmitting of 25 Hz balanced ringing voltage
7. Transmitting of 12 or 16 kHz metering pulses, programmable frequency
8. Programmable level of metering pulse transmitting
9. Transmitting and receiving of voice frequencies with a 2 wire / 4 wire hybrid
10. Programmable receiving and transmitting levels of voice frequencies
11. Programmable line termination impedance
12. Calling line identification (CLI)
13. Over voltage protection

6.5.2.2 Mechanical Design

The mechanical design of CCS-UNI units is based on standard DXX system mechanics. The units can occupy any card slot in the subrack; however, general recommendations for subrack equipping should be followed. CCS-UNI unit is 10T (50.8 mm) wide.

The CCS-UNI unit is build up by PBU560 control processor module, PDF553 power supply and two CCS554 subscriber line interface modules. Line interface modules are connected to control processor through power supply card PDF553, which delivers all operating voltages to unit. Unit is connected into the MarisDXX subrack's X-bus through connectors at the rear edge of the PBU560. See Fig. 32.

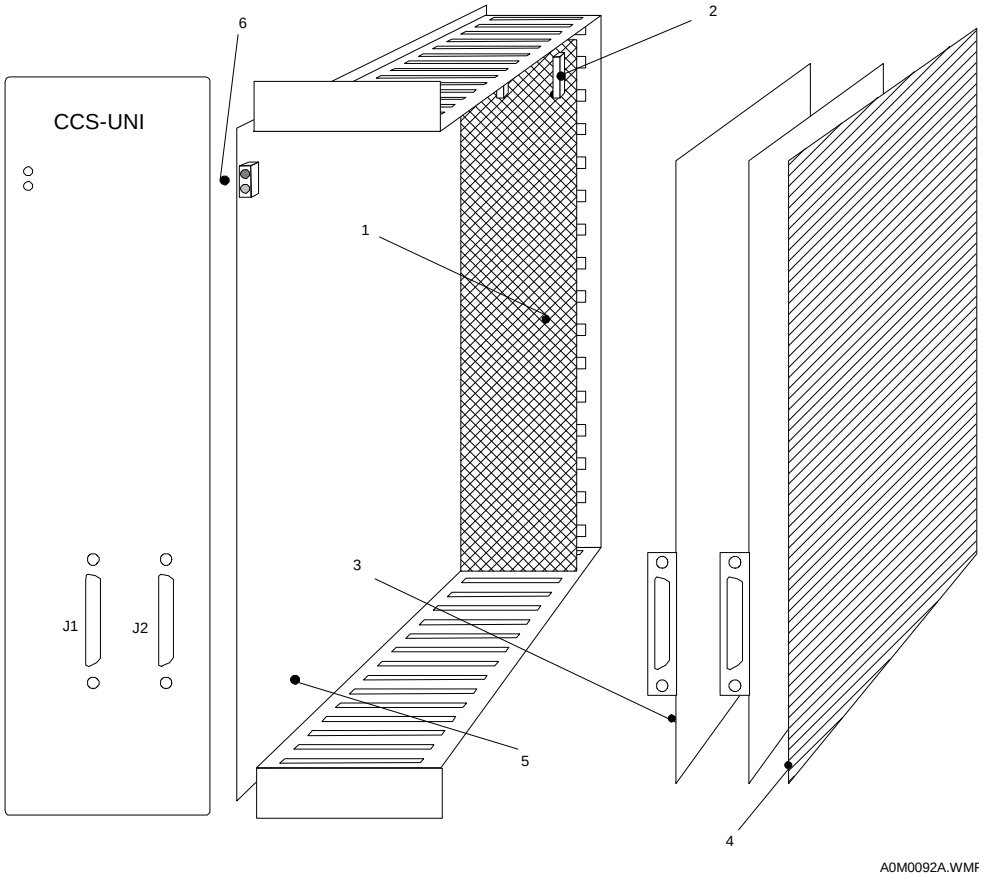


Fig. 32: Mechanical Structure of CCS-UNI

1. Power supply module PDF553
2. Connectors to subscriber line interface modules CCS554
3. Subscriber line interface modules (2 pcs) CCS554
4. EMC shielding plate
5. Control processor module PBU560
6. Alarm LEDs, upper red and lower yellow

The unit front panel houses two alarm LEDs and two subscriber lines interface connectors.

6.5.2.3 Block Diagram

See block diagram of CCS-UNI in Fig. 33.

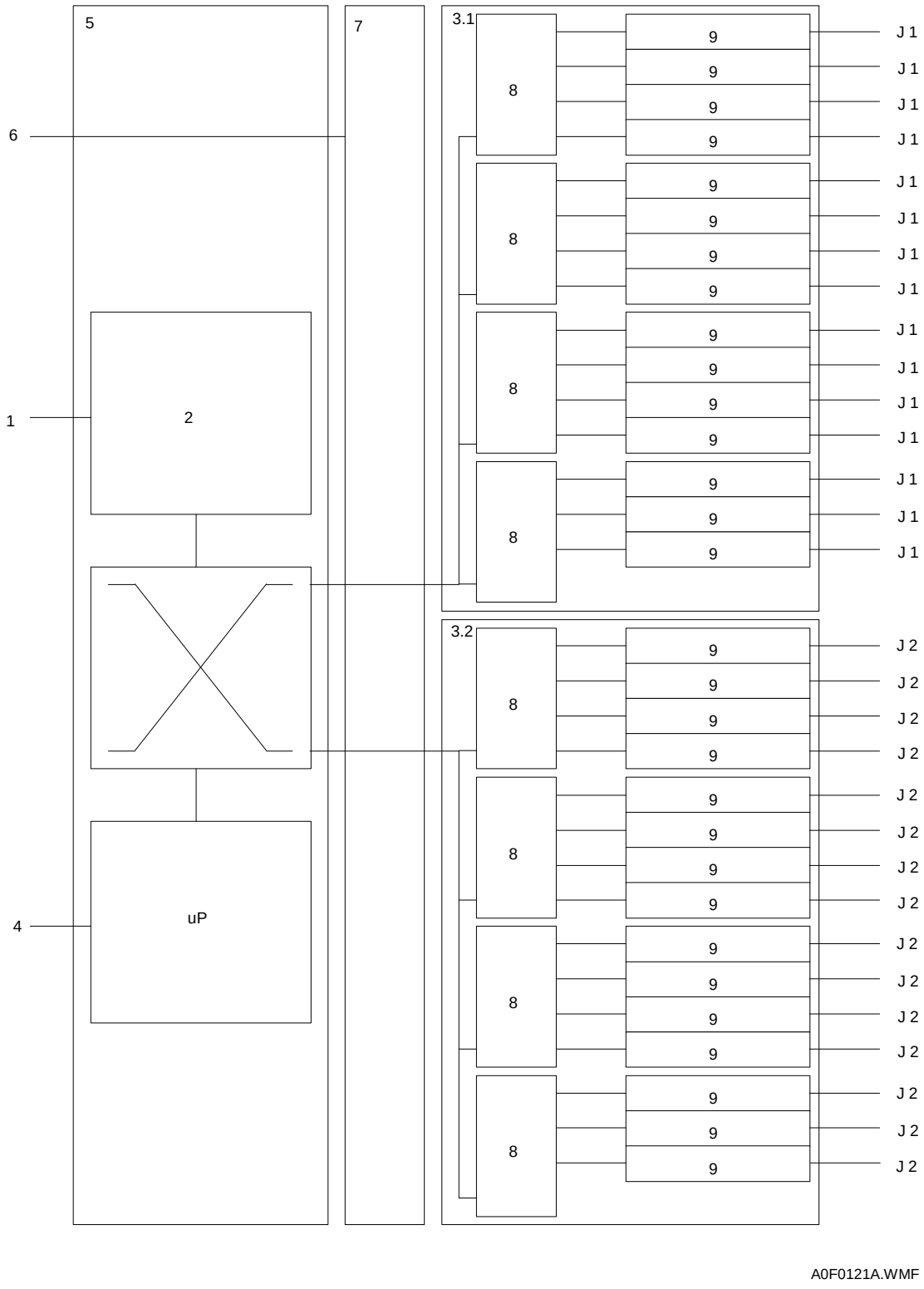


Fig. 33: Functional Structure of CCS-UNI

1. Cross connection bus (X-bus)
2. X-bus interface
3. 3.1 and 3.2CCS554 subscriber line interface modules
4. Control bus (C-bus)
5. Control processor module PBU560
6. Battery bus (B-bus)
7. Power supply module PDF553 delivering +5 V, +12 V, -10 V and –22 V
8. Four channel coder – decoder
9. Subscriber line interface circuit

J 1 and J 2 front panel connectors

The main functional blocks of the unit include power supply, control processor module, two subscriber line interface modules and an X-bus interface.

Power supply delivers all operating voltages for unit from battery-bus. Control processor module handle signalling, monitors unit's state and reports faults to NMS. Unit's interface modules implement analog interfaces. Interface modules deliver control channels to control processor and bearer-channels have static cross-connection to X-bus.

6.5.3 Interface Modules

Unit CCS-UNI uses two similar 16 channel interface modules CCS554. Module CCS554 behind front plate connector J1 delivers channels 1 to 16 and module behind J2 channels 17 to 30. One CCS-UNI unit carries total 30 subscriber line interfaces.

6.5.4 Faults

6.5.4.1 Fault table

The fault table is described here and the table should be updated here as required. The format of the table mirrors the format of the fault array structure in the software, with an additional field for the explanation of the fault.

The fields are interpreted as follows:

Name: Name of fault condition.
Sever: Major, Minor or Warning.
Status: PMA, DMA or MEI.
Srv: An S in this column means the alarm is a service alarm.
Led: R for Red (upper in front plate), Y for Yellow (lower in front plate).
Blk: Block number (defined below).
GPT: General problem type, see [6].
SPT: Specific problem type.
Description: A comment.

The block number defines the source of the fault according to the following table.

Block 0: Common Block
Blocks 1 – 30: The interfaces

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
Unpredicted fault condition	Major	PMA	-	R	0	1	1	This fault condition should never occur (or not yet supported).
Software error	Major	PMA	-	R	0	1	2	Software has noted an inconsistency in its own logic.
Software error in Signalling Controller	Major	PMA	-	R	0	1	3	The main processor has received an unknown message from the Signalling Controller.
Reset	Major	PMA	S	R	0	2	4	There has been a unit reset (detected always after the power-up of the unit).
Reset in Signalling Controller	Major	PMA	S	R	0	2	5	There has been a reset in the Signalling Controller (detected always after the power-up of the unit).
Setup error	Major	PMA	S	R	0	3	6	One of the setting structures has been corrupted in the non-volatile memory.
Power supply +5 V (subrack)	Major	PMA	-	R	0	4	7	The voltage is below the threshold limit (about 4.6 V depending on the calibration and the A/D resolution).
Power supply +5 V	Major	PMA	-	R	0	4	8	The voltage is below the threshold limit (about 4.6 V depending on the calibration and the A/D resolution).
Power supply +12 V	Major	PMA	-	R	0	4	9	The voltage is below the threshold limit (about 11.3 V depending on the calibration and the A/D resolution).
Power supply -10 V	Major	PMA	-	R	0	4	10	The voltage is above the threshold limit (about -9.0 V depending on the calibration and the A/D resolution).
Power supply -20 V	Major	PMA	-	R	0	4	11	The voltage is above the threshold limit
RAM fault	Major	PMA	S	R	0	5	12	A background process has detected a RAM location where the read value does not match with the written test pattern.
RAM fault in Signalling Controller	Major	PMA	S	R	0	5	13	A background process in the Signalling Controller has detected a RAM location where the read value does not match with the written test pattern.
PROM fault	Major	PMA	S	R	0	5	14	The calculated check sum does not match with the stored one.
Flash write error	Major	PMA	S	R	0	5	15	Error during writing to the flash memory (main bank).

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
Flash copy error	Major	PMA	S	R	0	5	16	Error during writing to the flash memory (shadow bank).
Flash erase error	Major	PMA	S	R	0	5	17	Error during erase of the flash memory (shadow bank).
Flash duplicate error	Major	PMA	S	R	0	5	18	Duplicated parameters (same ID) detected during start-up.
Flash shadow error	Major	PMA	S	R	0	5	19	The shadow bank of the flash is not erased during start-up.
Flash checksum error	Major	PMA	S	R	0	5	20	The calculated check sum does not match with the stored one.
Flash fault in Signalling Controller	Major	PMA	S	R	0	5	21	The Signalling Controller has detected an error in its own flash memory.
Missing module 1	Major	PMA	S	R	0	10	22	The interface module defined in the settings is missing.
Missing module 2	Major	PMA	S	R	0	10	23	The interface module defined in the settings is missing.
Conflict in module type 1	Major	PMA	S	R	0	10	24	There is a conflict between the installed module and the settings.
Conflict in module type 2	Major	PMA	S	R	0	10	25	There is a conflict between the installed module and the settings.
Loss of multiframe sync	Major	PMA	S	R	0	25	26	Loss of multiframe synchronization state detected by the Signalling Controller
ASIC fault in base unit	Major	PMA	S	R	0	32	27	The fault is activated if difference between write/read configuration data of ASIC has been detected.
Start permission denied	Major	PMA	S	R	0	36	28	Most likely the unit does not belong to the node configuration.
Bus sync fault	Major	PMA	S	R	0	38	29	No DXX bus synchronization from SXU detected.
IA activity missing	Major	PMA	S	R	0	40	30	The interface address is not activated on the cross-connection bus by the SXU.
Missing or incompatible application program	Major	PMA	S	R	0	55	31	There is no downloaded software in flash or the revision is wrong.
Checksum error in downloaded SW	Major	PMA	S	R	0	55	32	The downloaded software has been corrupted.
HW fault in base unit	Major	PMA	S	R	0	62	33	Base unit hardware does not work as expected.
Strapping conflict	Major	MEI	-	R	0	62	34	The strapping info of the base unit PCB is not what the software expects. Maybe the software is installed on a wrong unit.
HW fault in module 1	Major	PMA	S	R	0	62	35	Module hardware does not work as expected.

Name	Sever	Status	Srv	Led	Blk	GPT	SPT	Description
HW fault in module 2	Major	PMA	S	R	0	62	36	Module hardware does not work as expected.
No response from Signalling Controller	Major	PMA	S	R	0	62	37	A timeout occurred when waiting response from the Signalling Controller.
Error message from Signalling Controller	Major	PMA	S	R	0	62	38	The Signalling Controller returned an error to test message (other than RAM or flash error).
Setup conflict	Major	DMA	-	R	0	69	39	Information stored to setup is self-contradictory.
Interface loop to net	Warn	MEI	S	Y	1-30	27	40	An interface loop is created in the interface module. It loops transmitted data back to the interface receiver.
Equipment loop to net	Warn	MEI	S	Y	1-30	27	41	Similar to Interface loop except that the loop is made before the interface module on the PBU base card.
Line loop to user	Warn	MEI	S	Y	1-30	27	42	Rx-data is looped back to the interface transmitter.
AIS from Network	Warn	MEI	S	Y	1-30	42	43	AIS is detected from DXX Network.
Faults masked	Warn	MEI	-	Y	1-30	58	44	The fault is activated when interface Fault mask setting is on (all interface faults are cleared).
Fault in interface	Major	PMA	S	R	1-30	62	45	Line interface does not work as expected.
IF blocked off	Warn	MEI	S	-	1-30	63	46	The interface has been blocked from the use.
Filter coefficients missing	Warn	MEI	-	Y	1-30	69	47	The coefficients of the Signal Processing Codec Filter (SICOFI) are missing. Default coefficients are used.

6.5.5 Front Panel

See front panel of CCS-UNI unit in Fig. 35.

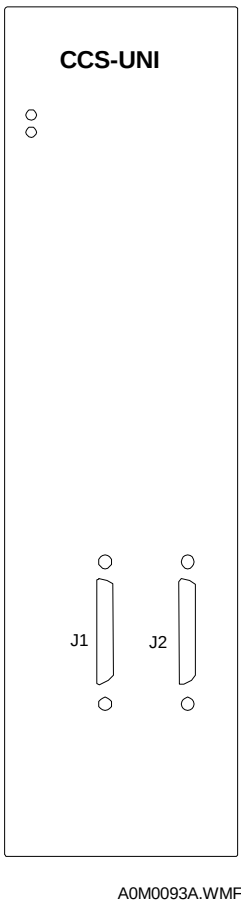


Fig. 34: Front Panel of CCS-UNI

Allocation of subscriber line interfaces is the following: Lines 1 to 16 connector J1 and lines 17 to 30 connector J2.

Numbering of Connector J1

Connector J1 pin number	Signal name	Connector J1 pin number	Signal name
1	GROUND	26	GROUND
2	1 TIP	27	9 TIP
3	1 RING	28	9 RING
4	GROUND	29	GROUND
5	2 TIP	30	10 TIP
6	2 RING	31	10 RING
7	GROUND	32	GROUND

Numbering of Connector J1

Connector J1 pin number	Signal name	Connector J1 pin number	Signal name
8	3 TIP	33	11 TIP
9	3 RING	34	11 RING
10	GROUND	35	GROUND
11	4 TIP	36	12 TIP
12	4 RING	37	12 RING
13	GROUND	38	GROUND
14	5 TIP	39	13 TIP
15	5 RING	40	13 RING
16	GROUND	41	GROUND
17	6 TIP	42	14 TIP
18	6 RING	43	14 RING
19	GROUND	44	GROUND
20	7 TIP	45	15 TIP
21	7 RING	46	15 RING
22	GROUND	47	GROUND
23	8 TIP	48	16 TIP
24	8 RING	49	16 RING
25	GROUND	50	GROUND

Note 1: Each channel uses two connector pins because of two connected wires; Tip and Ring.

Numbering of Connector J2

Connector J2 pin number	Signal name	Connector J2 pin number	Signal name
1	GROUND	26	GROUND
2	17 TIP	27	25 TIP
3	17 RING	28	25 RING
4	GROUND	29	GROUND
5	18 TIP	30	26 TIP
6	18 RING	31	26 RING
7	GROUND	32	GROUND
8	19 TIP	33	27 TIP
9	19 RING	34	27 RING
10	GROUND	35	GROUND
11	20 TIP	36	28 TIP
12	20 RING	37	28 RING
13	GROUND	38	GROUND
14	21 TIP	39	29 TIP
15	21 RING	40	29 RING
16	GROUND	41	GROUND
17	22 TIP	42	30 TIP

Numbering of Connector J2

Connector J2 pin number	Signal name	Connector J2 pin number	Signal name
18	22 RING	43	30 RING
19	GROUND	44	GROUND
20	23 TIP	45	-
21	23 RING	46	-
22	GROUND	47	GROUND
23	24 TIP	48	-
24	24 RING	49	-
25	GROUND	50	GROUND

Note 1: Each channel uses two connector pins because of two connected wires; Tip and Ring.

A 50-pin SCSI II style connector is used in front panel of CCS-UNI. See Fig. 35 below for numbering.

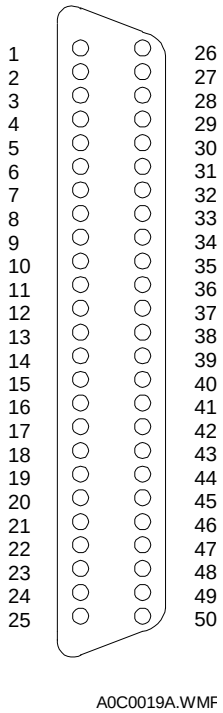


Fig. 35: Front Panel Connector of CCS-UNI, Front View

6.5.6 Unit Cabling

CCS-UNI unit's channels can be connected to subscriber line cross-connection panel with cable 838117242B POTS-UNI 10 m. See Fig. 36. Two cables are needed for each CCS-UNI unit.

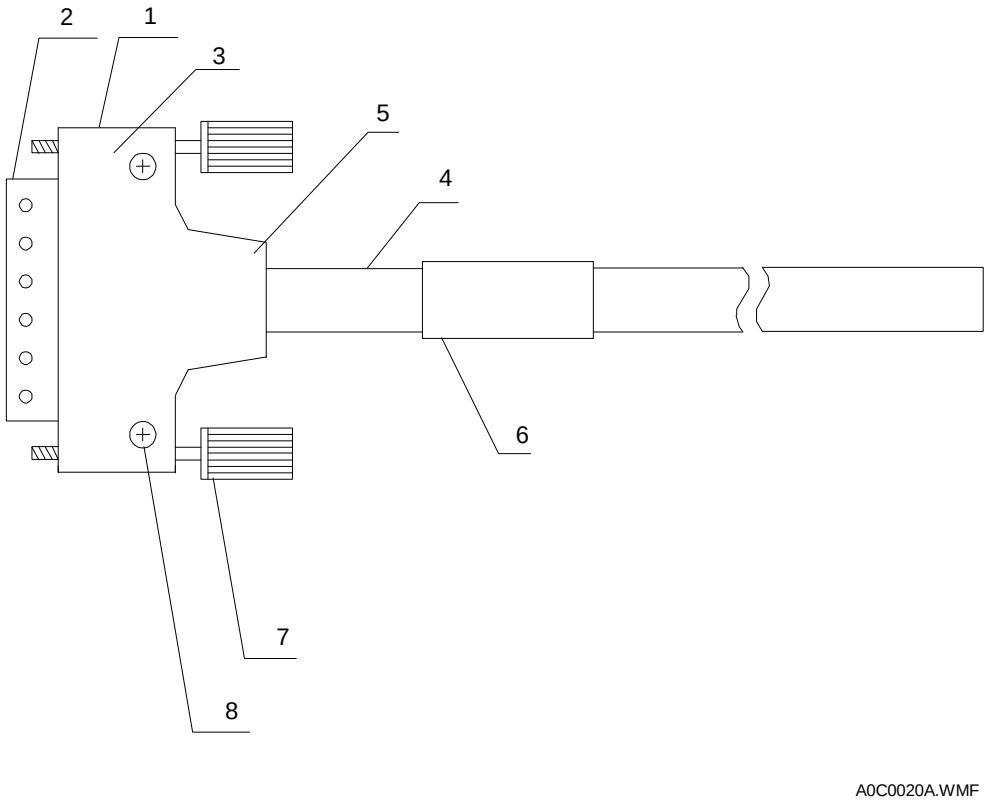


Fig. 36: Cable POTS-UNI 838117242B

1. AMP 749080-1 Shielded Backshell Kit with Jackscrews
2. AMP 749110-1 Cable Plug Connector
3. AMP 749108-4 Termination Cover, inside, 2 pcs
4. Madison 34ZDK00001 Cable, 17 pair, stranded 28 AWG, 100 W, 10 m
5. Strain Relief, inside
6. Marking: 838117242B POTS-UNI CABLE 10 m
7. Jackcrews, 2 pcs
8. Machine Screws, 2 pcs

6.5.6.1 Numbering of Cable Plug

See Fig. 37 below for unit cable plug's numbering:

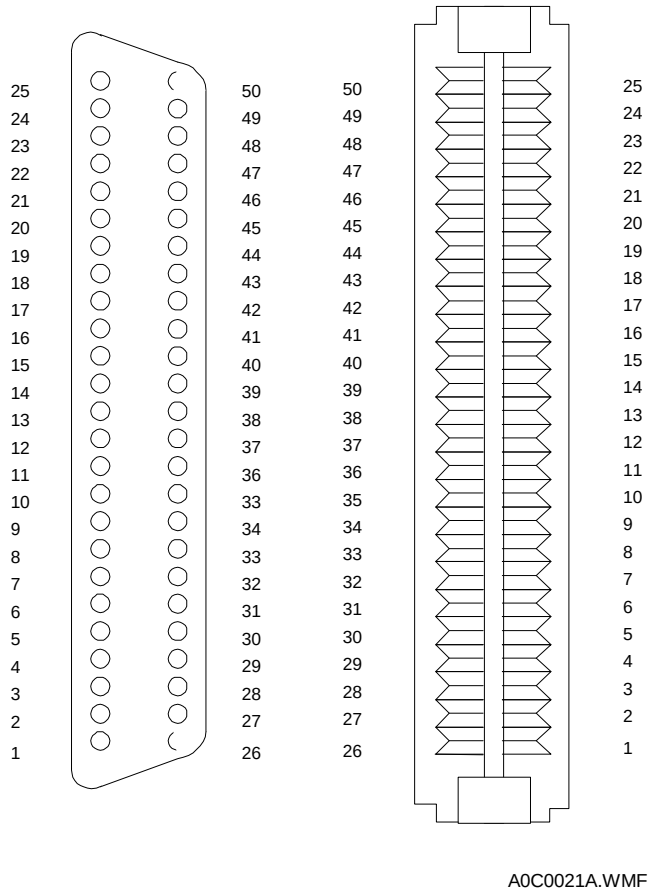


Fig. 37: POTS-UNI 838117242B Cable plug's numbering; Connector Pin Side and Termination Side

6.5.6.2 Numbering of Channels in Unit Cabling

Cable Connected to Connector J1

Subscriber line interface channels 1 to 16 are numbered in a cable connected to connector J1 as follows:

Interface Channel	Pair of Cable	Connector J1 Pins	Colour Coding of Wires
1	1	2,3	White/Black paired with Black/White
2	2	5,6	White/Brown paired with Brown/White
3	3	8,9	White/Red paired with Red/White
4	4	11,12	White/Orange paired with Orange/White
5	5	14,15	White/Yellow paired with Yellow/White
6	6	17,18	White/Green paired with Green/White
7	7	20,21	White/Blue paired with Blue/White
8	8	23,24	White/Violet paired with Violet/White
9	9	27,28	White/Grey paired with Grey/White
10	10	30,31	Black/Brown paired with Brown/Black
11	11	33,34	Black/Red paired with Red/Black
12	12	36,37	Black/Orange paired with Orange/Black
13	13	39,40	Black/Yellow paired with Yellow/Black
14	14	42,43	Black/Green paired with Green/Black
15	15	45,46	Black/Blue paired with Blue/Black
16	16	48,49	Black/Violet paired with Violet/Black
Ground	17	25,50	Black/Grey paired with Grey/Black

Cable Connected to Connector J2

Subscriber line interface channels 17 to 30 are numbered in a cable connected to connector J2 as follows:

Interface Channel	Pair of Cable	Connector J2 Pins	Colour Coding of Wires
17	1	2,3	White/Black paired with Black/White
18	2	5,6	White/Brown paired with Brown/White
19	3	8,9	White/Red paired with Red/White
20	4	11,12	White/Orange paired with Orange/White
21	5	14,15	White/Yellow paired with Yellow/White
22	6	17,18	White/Green paired with Green/White
23	7	20,21	White/Blue paired with Blue/White
24	8	23,24	White/Violet paired with Violet/White
25	9	27,28	White/Grey paired with Grey/White
26	10	30,31	Black/Brown paired with Brown/Black
27	11	33,34	Black/Red paired with Red/Black
28	12	36,37	Black/Orange paired with Orange/Black
29	13	39,40	Black/Yellow paired with Yellow/Black
30	14	42,43	Black/Green paired with Green/Black
-	15	45,46	Black/Blue paired with Blue/Black
-	16	48,49	Black/Violet paired with Violet/Black
Ground	17	25,50	Black/Grey paired with Grey/Black

6.5.7 Technical Specifications

6.5.7.1 Transmission Characteristics of CCS-UNI

Type of encoding 64 kbit/s PCM (ITU-T G.711 A-law. Also, m-law is possible, but not implemented)

Nominal impedance 600W, 200W+820W//115nF, 275W+850W//150 nF impedances are software selectable. List of impedances is possible to expand if needed.

Return loss

Per ITU-T Q.552 01/94 figure 1, typical value over 24 dB at 1 kHz

Terminal balance return loss (TBRL)

Per ITU-T Q.552 01/94 figure 11, typical value over 26 dB at 1 kHz

Relative levels

64 different input and output level pair in regions

Input -6 dBr.....+6 dBr (attenuation from analog to DXX)

Output –7,5 dBr .....+1 dBr (gain from analog to DXX)

Longitudinal balance Minimum > 35 dB, Typical > 46 dB at 1 kHz

Attenuation/frequency distortion in analog to DXX and DXX to analog. 0 dB level is set at frequency point 1020 Hz.

Frequency	minimum loss	maximum loss
0...200 Hz	0 dB	no limit
200...300 Hz	-0.30 dB	no limit
300...400 Hz	-0.30 dB	1.0 dB
400...600 Hz	-0.30 dB	0.75 dB
600...2400 Hz	-0.30 dB	0.35 dB
2400...3000 Hz	-0.30 dB	0.55 dB
3000...3400 Hz	-0.30 dB	1.5 dB
3400...3600 Hz	-0.30 dB	no limit
Frequency >3600 Hz	0 dB	no limit

Variation of gain with input level

Per ITU-T Q.552 01/94 figure 5

Signal-to-total distortion ratio

Encoding and decoding side per ITU-T Q.552 01/94 figure 14

Idle channel noise

Per ITU-T Q.552 01/94 sections Input connection and Output connections

6.5.7.2 DC Characteristics

On-Hook voltage 48V +20% -15%

Loop resistance at Off-Hook state less than 1500 W

Line feeding current 25 mA nominal into 0 W, 20 mA nominal into 1000 W

Reversal of line current is supported

6.5.7.3 Ringing

Voltage generation mode balanced

Frequency 25 Hz nominal (22.25 to 26.25 Hz)

Voltage level 60 Vrms at 10 kW

Ring trip function is implemented without any imposed DC offset voltage component within the ringing voltage.

6.5.7.4 Metering

Metering pulse frequency 12 kHz or 16 kHz, software selectable

Inaccuracy of frequency +- 1000 ppm

Metering pulse duration 150 ms (140 ms to 160 ms)

Metering pulses repetition frequency between CCO-UNI, CCS-UNI is 2.4 Hz maximum

Metering pulse's nominal level into 200 W termination is software selectable as indicated in a table below:

Level setting	Transmitting voltage rms level when frequency setting is 12 kHz	Transmitting voltage rms level when frequency setting is 16 kHz
1	0 V	0 V
2	0.10 V	0.22 V
3	0.20 V	0.45 V
4	0.29 V	0.65 V
5	0.41 V	0.95 V
6	0.50 V	1.1 V
7	0.60 V	1.3 V
8	0.68 V	1.5 V
9	0.86 V	1.8 V
10	0.92 V	2.0 V
11	0.98 V	2.1 V
12	1.0 V	2.2 V
13	1.0 V	2.3 V
14	1.1 V	2.3 V
15	1.1 V	2.4 V
16	1.1 V	2.4 V

6.5.7.5 Caller Identification

CCS-UNI is capable to transmit caller identification during On-Hook.

6.5.7.6 Power Supply Requirements

Input voltage –48 VDC, range –40.5 V to –60.0 V prETS 300 132-2 May 1996.

Typical power consumption 15 W when all 30 lines On-Hook and maximum 50 W when all 30 lines are Off-Hook. When traffic is 100 mErlang per line, the average power is 20 W and 99.999 % of the time power is less than 35 W. Maximum peak input power is 75 W.

Subrack's Power Supply Unit

A DC-feeding power supply unit (PFU) is required in a DXX subrack carrying CCS-UNI units.

However, it is possible to use an AC power supply PAU-5T or PAU-10T with CCS-UNI. Power supply units PAU or PAU-15T are not possible to use. When an AC power supply unit is used, the subrack of the node must be permanently grounded according to safety regulations.

6.5.7.7 Electromagnetic Compatibility

Test has been performed according to ETSI 300 386-1: December 1994, table 4: Public telecommunications equipment, locations other than telecommunication centres. Normal priority of service.

Statement of conformity: CCS-UNI unit with cable 838117242B POTS-UNI 10 m installed into a DXX node fulfil the essential requirements of the European telecommunication standard ETS 300 386-1.

6.5.7.8 Environmental Specifications

Unit is intended to be used in telecommunication equipment premises

Environmental operating conditions: ETS 300 019-1-3 Class 3.1; 1992

(Combination of IEC 721-3-3 classes 3K3/3B1/3C2/3S2/3M1)

Condition:

normal operating conditions +5º+40 oC, < 85 % RH, non-condensing

exceptional operating conditions -5º +45 oC < 90 % RH, non-condensing

6.5.7.9 System Alternatives

There are three alternative ways to build the system towards the PBX or LE, namely by using:

1. An analog connection to PBX or LE with CCO-UNI unit.
2. A digital V2 interface with Channel Associated Signalling (CAS).
3. A digital V5.1 interface with Common Channel Signalling.

Please see Fig. 40, Fig. 41 and Fig. 42 below.

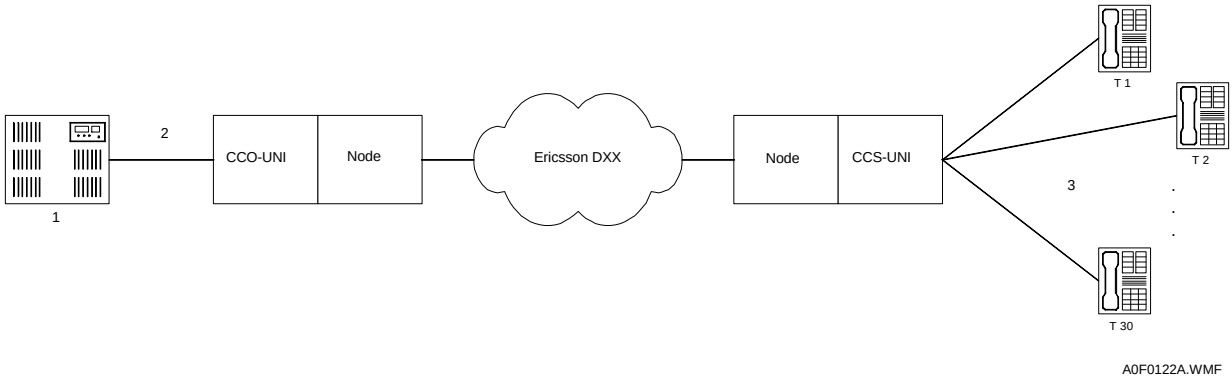


Fig. 38: A system using analog two-wire office line interface unit

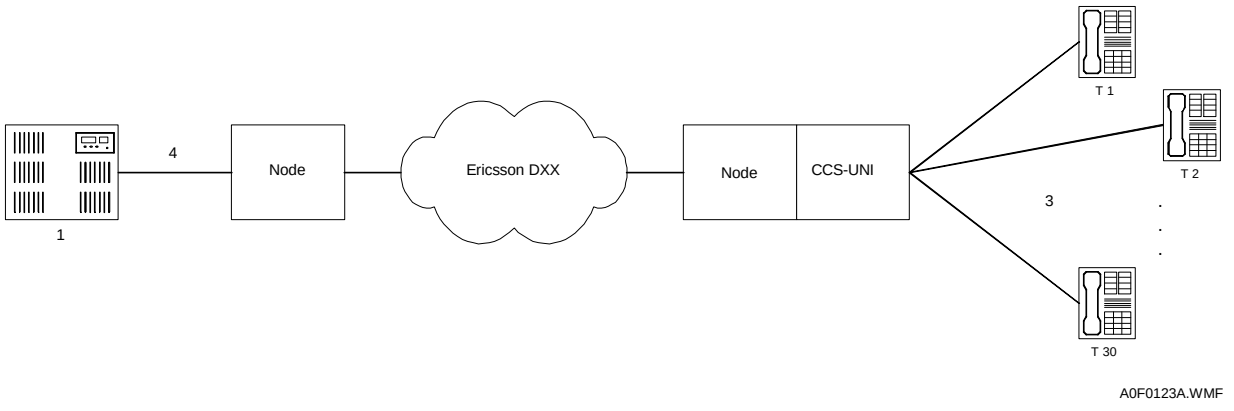


Fig. 39: (CCO-UNI) connection to PBX or LE

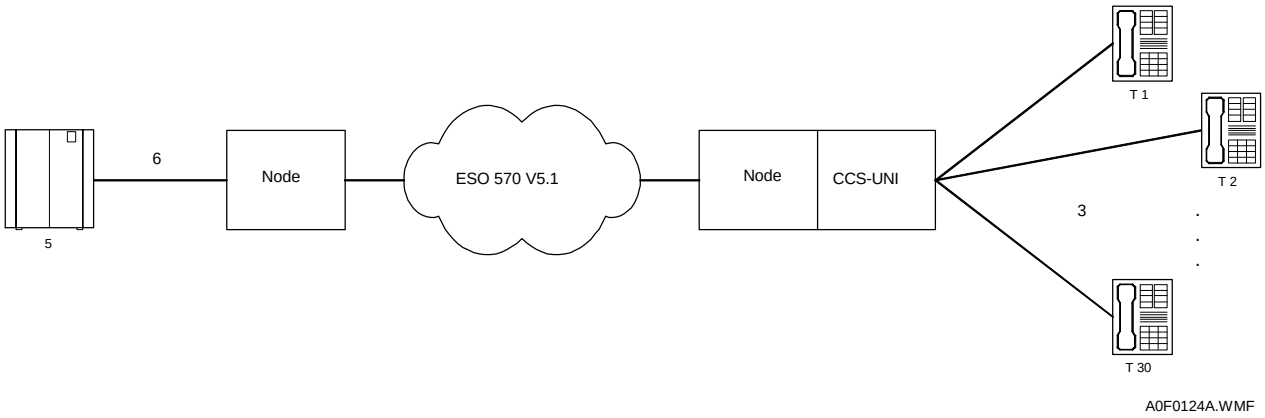


Fig. 40: A system using V5.1 interface to PBX or LE and V5.1 signalling server ESO 570

1. PBX or LE
2. Analog two-wire office line interfaces
3. Analog two-wire subscriber lines
4. V2 (CAS) G.703 digital interface
5. LE
6. V5.1 G.703 digital interface

In every case, a 30-channel subscriber line interface **CCS-UNI** unit is used as an interface between analog telephone terminals and the DXX system.

Note: If V2 channel associated signalling (CAS) support is used with the CCS-UNI, it may require software customisation by Ericsson. Please consult Ericsson sales office for details.

6.5.7.10 Three Bit-CAS Signalling

Channel Associated Signalling (CAS) transmits four signalling bits simultaneously in both directions between calling parties. Three signalling bits, namely a, b and c, are used in this application for every telephone call. Three signalling bits are needed to support CCS-UNI's and CCO-UNI's wide functionality.

Fourth signalling bit (d) is not used in signalling. It is set by unit's unit software, typically to value '1'.

The following features are supported between CCS-UNI and CCO-UNI with a three bit signalling:

— on-hook / off-hook
— ground key
— metering pulse
— polarity reversal
— ringing
— blocking

First two features are detected by CCS-UNI and transmitted towards CCO-UNI. The remaining features (from metering pulse to blocking) are detected by CCO-UNI and they are transmitted towards CCS-UNI.

Between CCS-UNI and a V5.1 server there is an additional feature:

— line test

Signalling functions of CCS-UNI and CCO-UNI are realised by contents of program memories of PBU's microprocessor and microcontroller. The contents of program memories can be altered by configuring an existing unit software version with NMS or by releasing and down loading a new version of unit software.

Note that there can be a different kind of CAS signalling when CCS-UNI is connected directly to a V2 local exchange. In addition, a two bit signalling may be present, especially if information compression is desired for ADPCM-transmission.

Signalling Bits of CCS-UNI

Definition of Directions
Signalling directions of CCS-UNI are defined in Fig. 41 below:

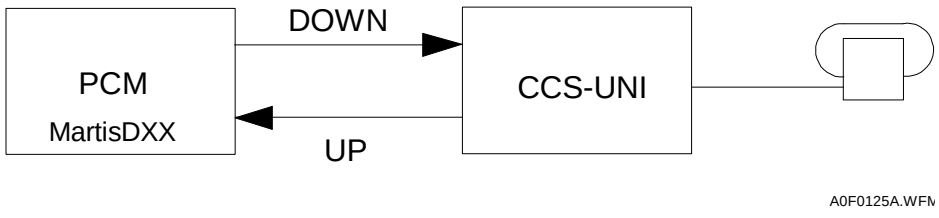


Fig. 41: Signalling directions of CCS-UNI

Usage of Signalling Bits

CCS-UNI's Direction DOWN

a	b	c	Meaning
'0'	'0'	'0'	This code is reserved for future expansion
'0'	'0'	'1'	Normal polarity
'0'	'1'	'0'	Reversed polarity
'0'	'1'	'1'	Normal polarity with metering pulse on
'1'	'0'	'0'	Reversed polarity with metering pulse on
'1'	'0'	'1'	Ringing
'1'	'1'	'0'	Line testing request
'1'	'1'	'1'	Blocked, no line current feed

CCS-UNI's Direction UP

a	b	c	Meaning
'0'	'0'	'0'	This code is reserved for future expansion
'0'	'0'	'1'	On-hook
'0'	'1'	'0'	Off-hook, ground key off
'0'	'1'	'1'	Off-hook, ground key on
'1'	'0'	'0'	Line test in operation
'1'	'0'	'1'	Line test OK
'1'	'1'	'0'	Line test failed
'1'	'1'	'1'	Alarm indication signal

Signalling Bits of CCO-UNI

Definition of Directions

Signalling directions of CCO-UNI are defined in Fig. 42 below:

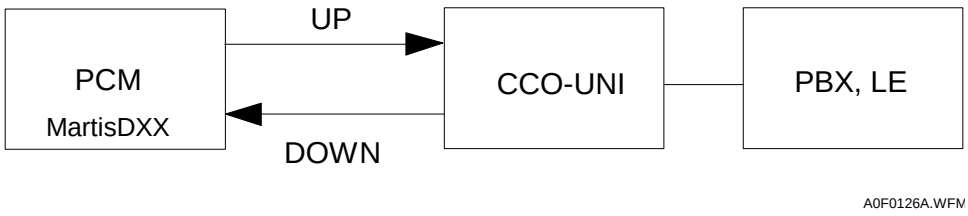


Fig. 42: Signalling directions of CCO-UNI

Usage of Signalling Bits

CCO-UNI's Direction UP

a	b	c	Meaning
'0'	'0'	'0'	This code is reserved for future expansion
'0'	'0'	'1'	On-hook
'0'	'1'	'0'	Off-hook, ground key off
'0'	'1'	'1'	Off-hook, ground key on
'1'	'0'	'0'	Line test in operation (not in use)
'1'	'0'	'1'	Line test OK (not in use)
'1'	'1'	'0'	Line test failed (not in use)
'1'	'1'	'1'	Alarm indication signal

CCO-UNI's Direction DOWN

a	b	c	Meaning
'0'	'0'	'0'	This code is reserved for future expansion
'0'	'0'	'1'	Normal polarity
'0'	'1'	'0'	Reversed polarity
'0'	'1'	'1'	Normal polarity with metering pulse on
'1'	'0'	'0'	Reversed polarity with metering pulse on
'1'	'0'	'1'	Ringing
'1'	'1'	'0'	Line testing request (not in use)
'1'	'1'	'1'	Blocked, no line current feed

6.6 EAE ADPCM Server Unit

6.6.1 General

EAE ADPCM Server Unit offers a compression feature in the DXX Cross-Connect System. One unit serves 30 individual channels. PCM data is compressed to ADPCM, transported through the DXX network and expanded back to PCM.

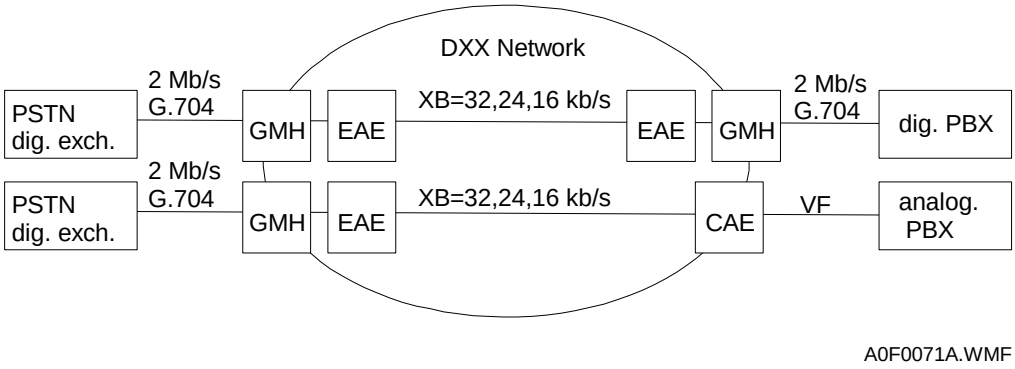


Fig. 43: EAE ADPCM Server Unit Applications

6.6.2 Operation of EAE ADPCM Server Unit

6.6.2.1 Mechanical Design

The body of the EAE consists of a base unit, a power supply and a program memory EAZ418. The available interface module is ADPCM-30.

The unit dimensions are 25 x 160 x 233 mm. The front panel houses two alarm LEDs, a red one and a yellow one. The back panel holds two euro connectors. The upper one accesses the control bus and the lower one the 64 Mbit/s data cross-connection bus of the subrack (X-bus). The back panel connectors also provide battery voltage for the power supply module.

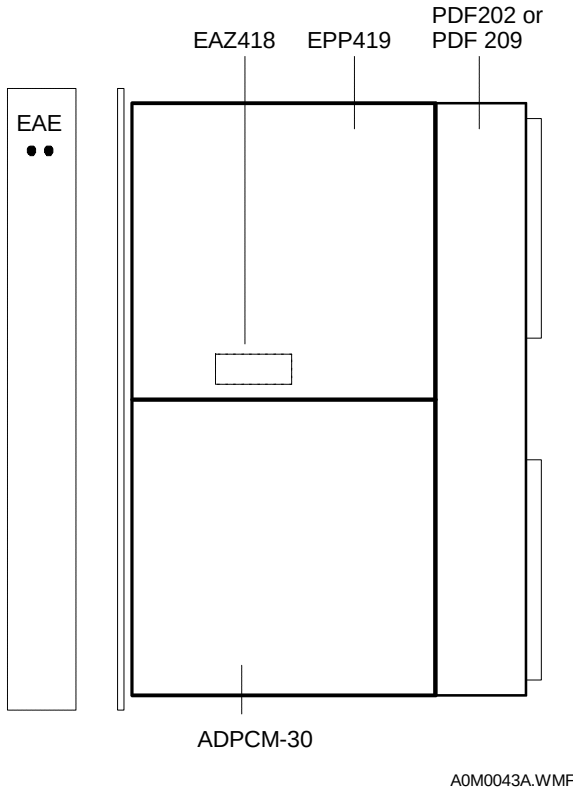


Fig. 44: EAE Equipped with Interface Module

Functional Structure

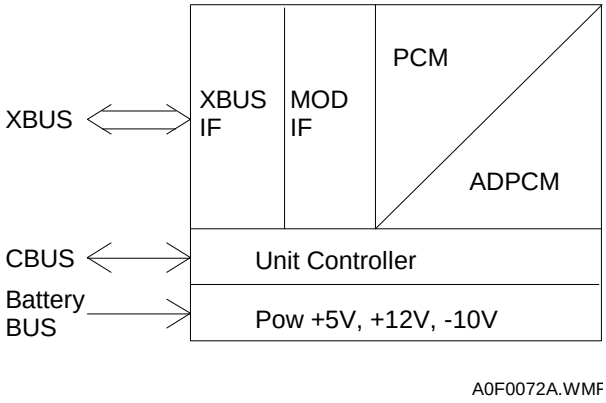


Fig. 45: Functional Structure of EAE

The main functional blocks of the EAE unit are the power supply, unit controller including the processor and its peripheral circuits, and an X-bus interface common for each channel.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor generates HDLC messages.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit; correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

The PCM data is taken from the X-bus and led to the module where it is compressed to ADPCM format. The ADPCM rate is selected by the NMS.

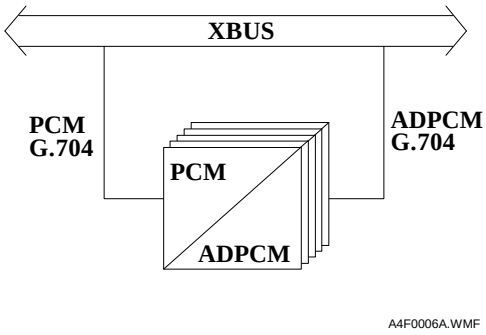


Fig. 46: Basic Function of EAE

Block Diagram

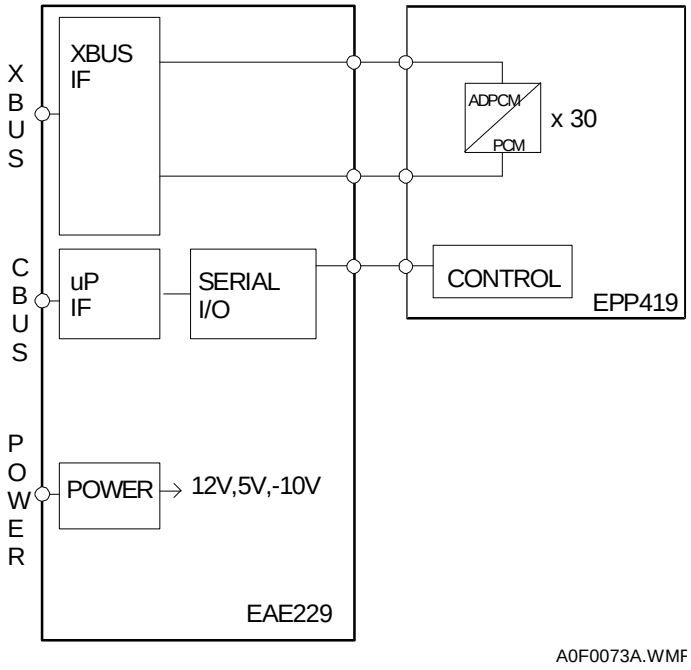


Fig. 47: EAE Block Diagram

6.6.2.2 Power Supply

A unit receives its operating voltage from the power supply module PDF 202 or PDF 209. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector.

The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit, and a low operating voltage results in a unit reset.

All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

6.6.2.3 Unit Controller

The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM memory identified as EAZ 418. Part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in case of a power interruption the unit is automatically reset to the conditions prevailing the interruption without specific parameterization. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC-links and the frame control bus.

6.6.2.4 Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored, and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting, it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

6.6.2.5 A/D Converter

The unit includes a multichannel analog-to-digital converter (A/D) which monitors the operating voltages.

6.6.2.6 X-bus Interface

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with the data bus DR2. The cross-connect unit decides with the aid of the bus test which bus to use, and this information is supplied to other units through the control bus. From the cross-connect unit the EAE unit receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are also monitored by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing, the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

The EAE unit has two G.704 ports to X-bus, one is for PCM data and the other for ADPCM data. Server channels 1...15 are mapped in time slots 1...15 and channels 16...30 in time slots 17...31. The ADPCM byte in X-bus is filled starting with the MSB bit.

6.6.2.7 ADPCM-30 Interface Module

There is one server chip for each channel in the module; the chip takes data from its own time slot from appropriate 2 Mbit/s bus, from PCM or ADPCM port, and makes the PCM/ADPCM conversion in the defined direction. The conversion direction from PCM to ADPCM, or vice versa, is selected by the NMS.

The microprocessor communicates with the module via a serial communication channel. It can read the module identification and set the configuration of the module.

The VF coding or ADPCM rate can be set individually for each channel the alternatives being:

— 64kbit/s PCM
— 32kbit/s ADPCM
— 24kbit/s ADPCM
— 16kbit/s ADPCM

CAS signalling is not supported.

Configuration cannot be changed when the channel is locked.

6.6.3 Faults and Actions in EAE ADPCM Server Unit

6.6.3.1 EAE ADPCM Faults and Actions

The following acronyms will be used in the table below:

PMA = Prompt Maintenance Alarm
S = Service Affecting Fault
MEI = Maintenance Event Information
R = Red alarm LED
Y = Yellow alarm LED

Common Faults

Fault Condition	Status	Front LEDs
Power supply : +5 V, +12 V, -10 V +5 V back plane voltage)	 PMA PMA	 R R
Memory faults RAM, EPROM fault FLASH fault	 PMA, S PMA, S	 R R
Check sum error in FLASH memory	PMA, S	R
Check sum error in downloaded SW	PMA, S	R
Operation status faults: Unit reset Unit unregistered Setup parameter error Conflict in module type Port conflict	 PMA, S PMA, S PMA, S PMA, S PMA, S	 R R R R R
Fault masking	MEI	Y
Module operation (IF combo write/read fault)	PMA, S	R

6.6.4 Technical Specifications for EAE ADPCM Server Unit

Number of channels per unit	30
Type of encoding	64 kbit/s PCM CCITT G.711 A-law (see Relevant Recommendations) 32 kbit/s ADPCM CCITT G.721 24 kbit/s ADPCM ANSI T1.303 16 kbit/s ADPCM by Dallas Semiconductor
Absolute channel delay	
- PCM to ADPCM	< 375 µs
- ADPCM to PCM	< 375 µs
Total distortion (CCITT G.712/G.713 method 1)	
- 64 kbit/s PCM	G.712/G.713
- 32 kbit/s ADPCM	G.712/G.713
- 24 kbit/s ADPCM	G.712/G.713 - 5 dB
- 16 kbit/s ADPCM	G.712/G.713 - 13 dB

6.7 ECS V.110 to X.50 Conversion Server Unit

6.7.1 General

The ECS V.110 to X.50 Conversion Server Unit has two variants, the ECS-5T and ECS-10T. The ECS-5T converts 30 channels of V.110 (or V.110M) data into 4 channels of X.50 (Division 2, Division 3 or bis) data and vice versa on a per-channel basis.

The ECS-10T converts 60 channels of V.110 (or V.110M) data into 8 channels of X.50 (Division 2, Division 3 or bis) data and vice versa on a per-channel basis.

6.7.2 Operation of ECS V.110 to X.50 Conversion Server Unit

6.7.2.1 ECS Structure

ECS Mechanical Design

ECS-5T Structure

ECS-5T consists of the following base unit and modules:

— UBU 254 universal base unit
— UBZ 439 unit software module
— PDF 488 (-48V) power supply module or
— PDF 489 (+24V) power supply module
— ECS 440 V.110 to X.50 conversion module
— RMU 467 Bus board for EPS-5T

The power supply module is mounted on the base unit.

The ECS-5T is 5T wide and may be mounted in any IF card slot.

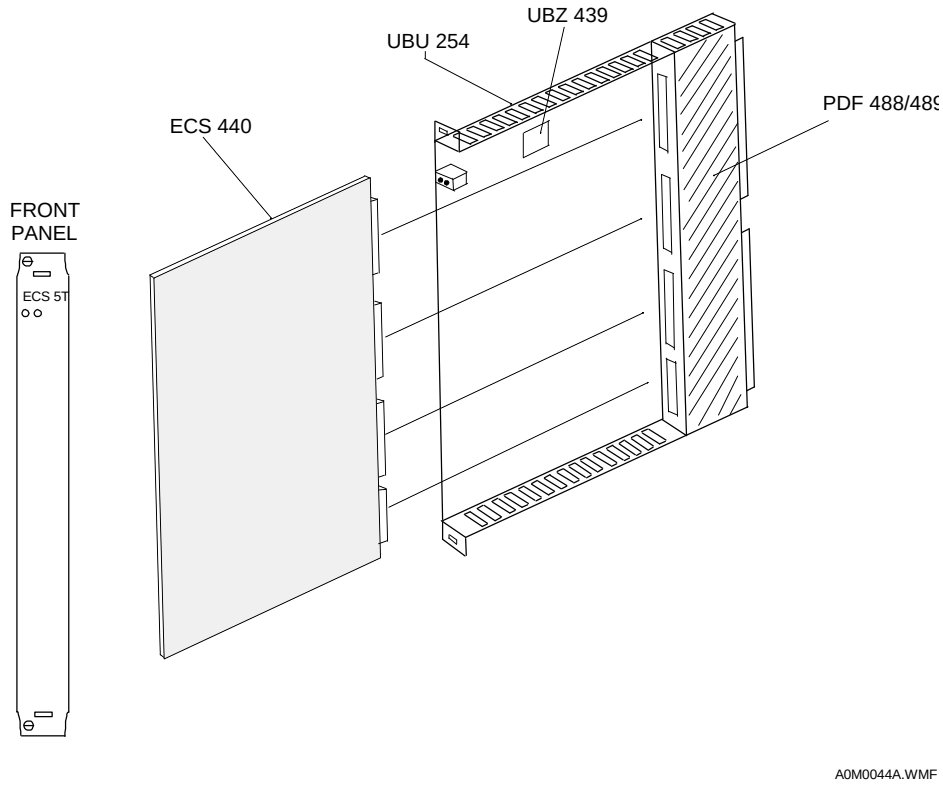


Fig. 48: ECS-5T structure

ECS-10T Structure

ECS-10T consists of the following base unit and modules:

— UBU 256 universal base unit
— UBZ 439 unit software module
— PDF 499 (-48V) power supply module or
— PDF 489 (+24V) power supply module
— Two ECS 440 V.110 to X.50 conversion modules
— RMU 468 Bus board for EPS-10T

The base unit is similar to the UBU 254 but comes equipped with double wide mechanics (10T).

The ECS-10T may be mounted in any IF card slots for 10-T units.

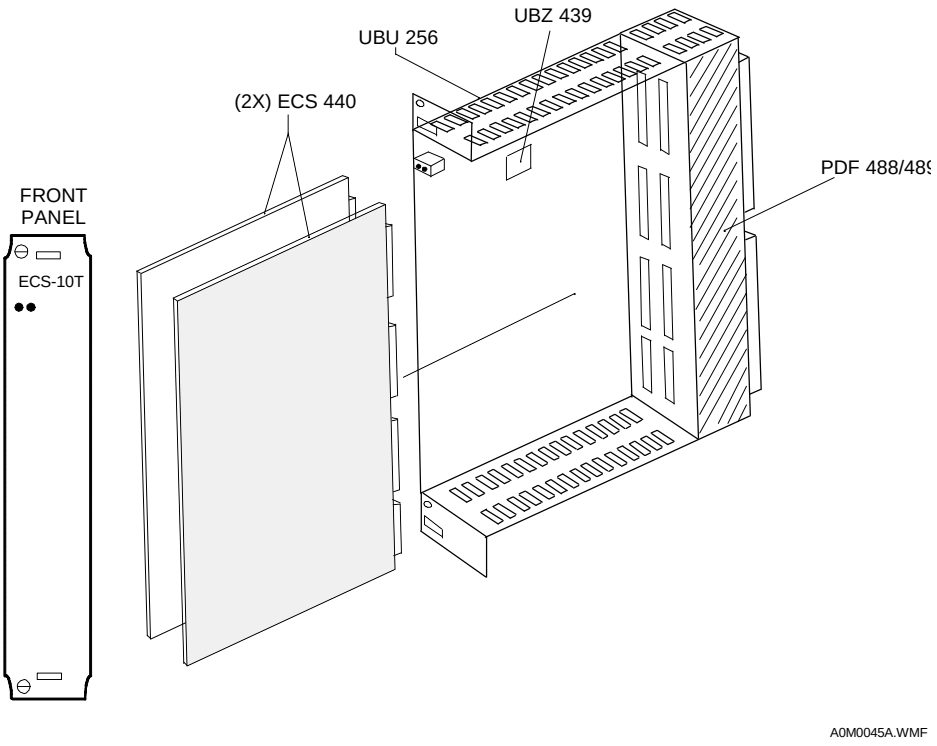


Fig. 49: ECS-10T structure

ECS 5T Block Diagram

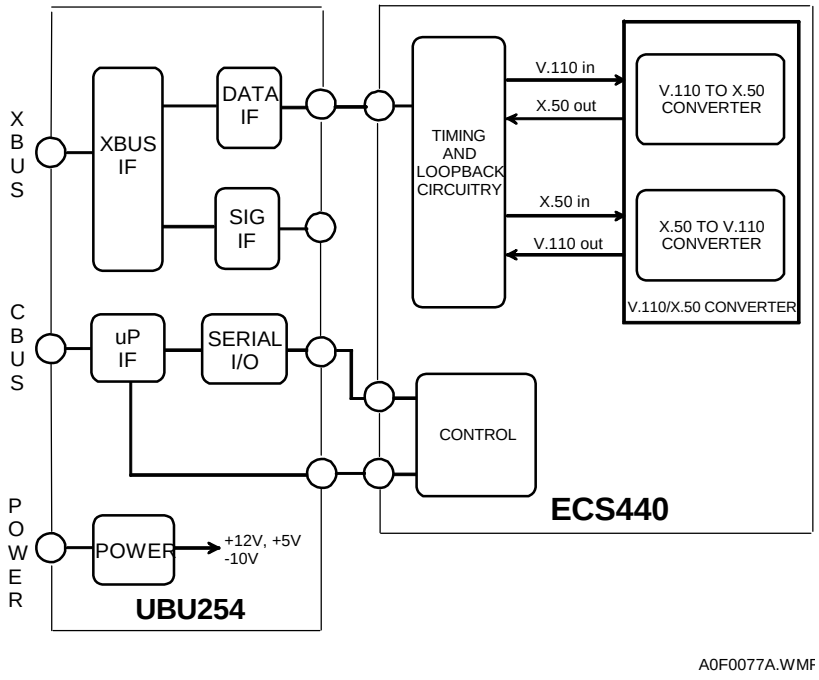


Fig. 50: ECS Server Block Diagram

6.7.2.2 Configuration Parameters

X.50 Framing Format

The user can select, on a per-X50-module basis, the X.50 framing format used. The ECS supports both ITU-T X.50 Division 2 and ITU-T X.50 Division 3. For a customer data rate of 48kbit/s, the customer can select either ITU-T X.50 Division 2, ITU-T X.50 Division 3, or ITU-T X.50 bis.

Customer Data Rates Supported

Data Rate	X.50 Division 2	X.50 Division 3	X.50 bis	V.110	V.110M
600 bit/s	Yes	No	No	Yes	Yes
1200 bit/s	Yes	Yes	No	Yes	Yes
2400 bit/s	Yes	Yes	No	Yes	Yes
4800 bit/s	Yes	Yes	No	Yes	Yes
9600 bit/s	Yes	Yes	No	Yes	Yes
14400 bit/s	Yes	Yes	No	Yes	Yes
19200 bit/s	Yes	Yes	No	Yes	Yes
48000 bit/s	Yes	Yes	Yes	Yes	Yes

Octet Assignments

The user will be able to select octet assignments in accordance with ITU-T Recommendation X.54 for the standard X.50 data rates.

X.50 Octet Assignments Supported

Data Rate (kbit/s)	Valid Octets per Channel	Total Possible Channels
0.6[a]	1 through 80	80 - Each 600 bit/s subrate uses 1 octet out of 80. Appears once every 80 octets.
1.2[b c]	1 & 41, or 2 & 42, or 3 & 43, or... 40 & 80	40 - Each 1.2 kbit/s subrate uses 2 octets out of 80. Appears twice every 80 octets.
2.4[d]	1 through 20	20 - Each 2.4 kbit/s subrate uses 1 octet out of 20. Appears once every 20 octets.
4.8[d]	1 & 11, or 2 & 12, or 3 & 13, or... 10 & 20	10 - Each 4.8 kbit/s subrate uses 2 octets out of 20. Appears twice every 20 octets.
9.6[d]	1 6 11 16, or 2 7 12 17, or 3 8 13 18, or 4 9 14 19, or 5 10 15 20	5 - Each 9.6 kbit/s subrate uses 4 octets out of 20. Appears four times every 20 octets.
14.4[b d]	1 2 6 11 12 16, or 3 4 8 13 14 18	2 - Each 14.4 kbit/s subrate uses 6 octets out of 20. Appears six times every 20 octets.
19.2[b d]	1 2 6 7 11 12 16 17, or 3 4 8 9 13 14 18 19, or 1 3 6 8 11 13 16 18, or 2 4 7 9 12 14 17 19, or 3 5 8 10 13 15 18 20	2 - Each 19.2 kbit/s subrate uses 8 octets out of 20. Appears eight times every 20 octets.
48.0	ALL	1 - Uses all octets in the X.50 bearer.

a ITU-T Recommendation X.50 Div. 2 support only.

b Not a standard X.50 subrate.

c Normally used only if X.50 bearer is configured as Div. 2. If Used with Div. 3, the 1.2 kbit/s channel shall be allocated octets as if it were a 2.4 kbit/s channel.

d Table reflects ITU-T Recommendation X.50 Div. 3 (20 octets). If an X.50 bearer has been configured as Div. 2, the listed subrate channel octets shall be continued throughout the 80 octet frame. For example, a 9.6 kbit/s channel shall reside in the following octets: 1 6 11 16 21 26 31 36... 71 76.

X.50 AIS Detection

The user can select either 15 or 32 consecutive octets of all ones as the threshold for declaring AIS on each of the four X.50 channels.

V.110 Line Conditioning

The user can select the data to be forwarded to V.110 channels for X.50 loss of frame and AIS.

Conditioning for X.50 Loss of Frame Alignment:

Detection of X.50 loss of frame alignment shall occur when four consecutive sections of framing bits are received with one or more bit errors in each section. A section shall consist of 10 consecutive framing bits, not including the housekeeping bits (A or A, B, C, D, E, F, G and H).

The recovery of X.50 loss of frame is achieved in two phases:

Step 1. Search Phase - The X.50 channel is searched for the forcing configuration bits (5 or 7 bits) in the framing pattern. When this is achieved the second phase is entered.

Step 2. Confirmation Phase - The 16 framing bits (except A, B, C, D, E, F, G and H) immediately following those of the search phase are examined together with those of the search phase. If all bits form part of the X.50 framing pattern, alignment is assumed to be recovered. If the bits do not form part of the framing pattern, the search phase is reentered.

The user can select one of the following three actions to occur while the loss of frame is active:

— AIS (all 1’s, no framing) shall be sent on all V.110 channels associated with the X.50 channel.
— IDLE (all 1’s, valid framing) shall be sent on all V.110 channels associated with the X.50 channel.
— IDLE (all 1’s, valid framing) shall be sent on all V.110 channels associated with the X.50 channel. If the loss of frame is active for 64 octets, Network Out of Service (NOS - SB=1 ata = 0) shall be sent on all V.110 channels associated with the X.50 channel.

Conditioning for X.50 AIS Detection:

AIS is assumed to be present when 15 or 32 (as selected by user) consecutive octets, each containing all ones, have been received. AIS shall inhibit X.50 loss of frame and excessive error ratio alarms.

The AIS is assumed to be cleared when three consecutive octets containing at least one ‘0’ have been received, or if X.50 frame alignment has been achieved.

The user can select one of the following three actions to occur while the X.50 channel is receiving AIS:

— AIS (all 1’s, no framing) shall be sent on all V.110 channels associated with the X.50 channel.
— IDLE (all 1’s, valid framing) shall be sent on all V.110 channels associated with the X.50 channel.
— IDLE (all 1’s, valid framing) shall be sent on all V.110 channels associated with the X.50 channel. If AIS is received for 64 octets, Network Out of Service (NOS - SB=1 data = 0) shall be sent on all V.110 channels associated with the X.50 channel.

X.50 Excessive Error Ratio (primary)

The user can select a threshold for the rate of framing bit errors on an X.50 channel required to declare an alarm. The available choices are 10^{-4}, 10^{-5}, and 10^{-6}, with 10^{-6} as the default. If this threshold is exceeded, a prompt maintenance alarm (PMA) will be declared.

X.50 Excessive Error Ratio (secondary)

The user can select a threshold for the rate of framing bit errors on an X.50 channel required to condition data. The available choices are 10^{-2}, 10^{-3}, 10^{-4}, 10^{-5} and 10^{-6}, with 10^{-2} as the default. The user can select one of the following three actions to occur while this threshold is exceeded:

— No action is taken.
— AIS (all 1's, no framing) shall be sent on all V.110 channels associated with the X.50 channel.
— IDLE (all 1's, valid framing) shall be sent on all V.110 channels associated with the X.50 channel.

X.50 S-bit Sense

The user must select the sense of the S-bit in the incoming X.50 data channel. This is used to determine whether the S-bit should be inverted before it is transmitted as the V.110 SB bit. The options are:

— S-bit not inverted (S = 0 $\rightarrow$ ON) (default)
— S-bit inverted (S = 0 $\rightarrow$ OFF)

X.50 Line Conditioning

The user can select the data to be forwarded on an X.50 channel for V.110 loss of frame and V.110 AIS.

Conditioning for V.110 Loss of Frame Alignment

V.110 loss of frame synchronization shall be defined as the detection of at least three consecutive V.110 frames, each with at least one framing bit error.

The user can select one of the following actions to occur while the loss of frame is active:

— Network Out Of Service (NOS - S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.
— IDLE (S=OFF, DATA=1) shall be sent on the X.50 octet(s) associated with the V.110 channel. If the loss of frame is active for 64 octets, NOS (S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.

Conditioning for V.110 AIS Detection

V.110 AIS shall be detected when less than 3 zeroes are received in 256 bits on the V.110 data stream.
V.110 AIS shall be cleared when at least 3 zeroes are received in 256 bits on the V.110 data stream.

The user can select one of the following actions to occur while the V.110 channel is receiving AIS:

— Network Out Of Service (NOS - S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.
— IDLE (S=OFF, DATA=1) shall be sent on the X.50 octet(s) associated with the V.110 channel. If AIS is received for 64 octets, NOS (S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.

6.7.2.3 Loopbacks

Only one loopback (patterned local loopback or line loopback) per X50 interface module may be active at any time.

X.50 External Line Loopback

An X.50 External Line Loopback is designed into the module for each of the four X.50 channels. The X.50 data toward the ECS is intercepted and looped back toward the source of the X.50. AIS will be transmitted on all V.110 channels connected to the X.50 channel under test.

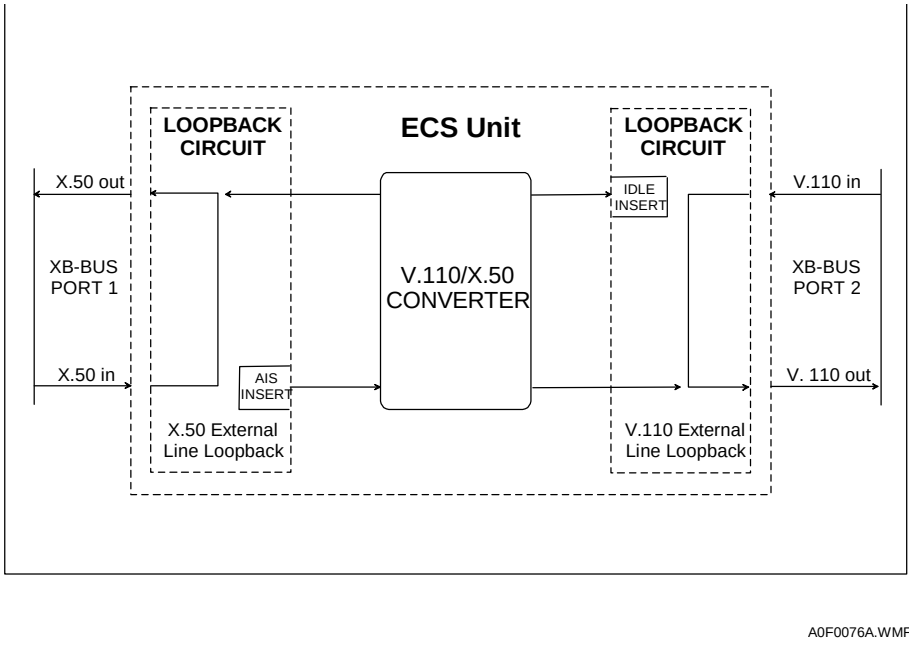


Fig. 51: ECS External Line Loopbacks

V.110 External Line Loopback

A V.110 External Line Loopback is designed into the module for each of the 30 V.110 channels. The V.110 data toward the ECS is intercepted and looped back toward the source of the V.110. IDLE will be transmitted on the X.50 octet(s) connected to the V.110 channel under test.

X.50 Internal Line Loopback

An X.50 Internal Line Loopback is designed into the module for each of the 4 X.50 channels. The X.50 data out of the V.110/X.50 converter block is looped back toward the V.110/X.50 converter block. All ones shall be transmitted towards the source of the X.50 channel under test.

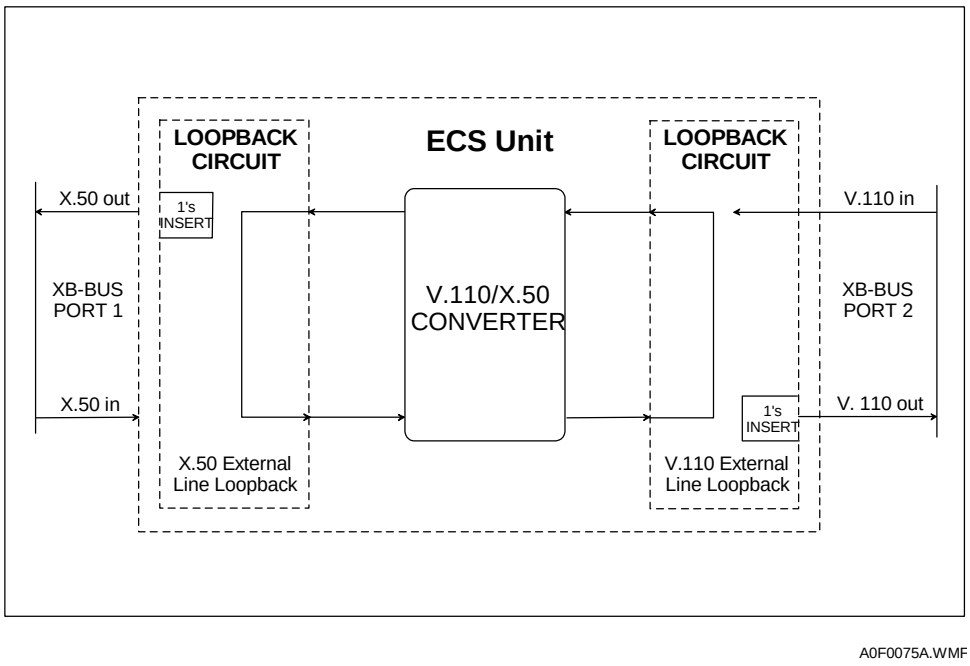


Fig. 52: ECS Internal Line Loopbacks

V.110 Internal Line Loopback

A V.110 Internal Line Loopback is designed into the module for each of the 30 V.110 channels. The V.110 data out of the V.110/X.50 converter block is looped back toward the V.110/X.50 converter block. All ones shall be transmitted towards the source of the V.110 channel under test.

Patterned Local Loopback

The patterned local loopback is used to verify the integrity of the X50 interface module hardware and software. The patterned local loopback tests the V.110 and X.50 input buffers, V.110 look-up-table RAM, V.110 output mapper functions, loopback control functions, and the V.110 framer functions. The DSP writes a test pattern into the X.50 input buffer. The V.110 mapper and look-up table convert this test data into V.110 data. The V.110 data is looped back to the V.110 framer using the V.110 Internal Line Loopback. The V.110 framer writes the test data into the V.110 input buffer and the DSP reads the V.110 input buffer and verifies the data. Because the patterned local loopback uses unassigned time slots, it does not affect data transmission or reception on any channels.

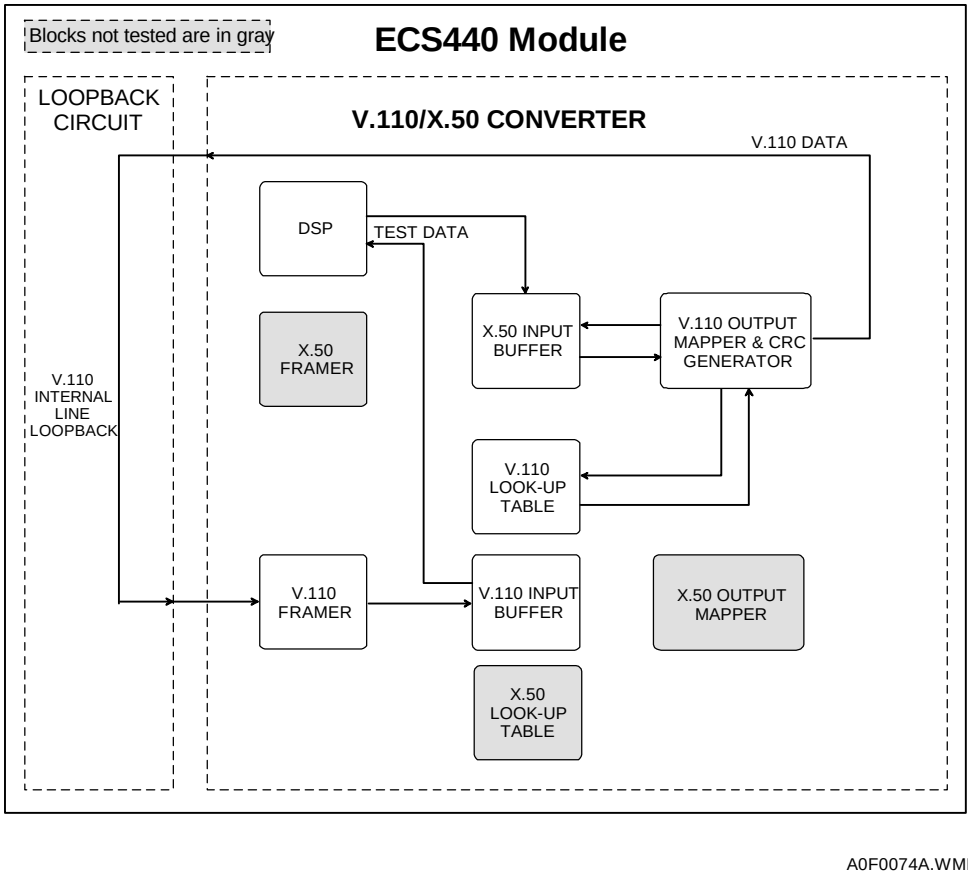


Fig. 53: ECS Patterned Local Loopback

6.7.2.4 Unit Control

The ECS unit is controlled by a 16-bit 80C188 microprocessor, which runs at 10 MHz. The unit processor links the subrack to the NMS via the VTP bus. The application program is stored in an interchangeable EPROM or FLASH memory. FLASH can be used to download updates to the application program. The unit's configuration parameters and unit number are stored in nonvolatile FLASH memory. This allows the unit to restore to its original state should a power loss occur. A watchdog circuit monitors the operation of the processor and generates a unit reset when the circuit is triggered.

6.7.2.5 Power Supply

ECS-5T/10T receives its power from the unit power supply module, PDF 488/499 or PDF489. The switching power supply provides three regulated output voltages: +5Vdc, +12Vdc and -10Vdc. Battery voltage is fed from the DXX-bus to be used as the supply voltage for the PDF488/499 power supplies. The module also receives +5Vdc bus voltage, which for start-up conditions is supplied to the interface circuits connected to the bus. The unit's generated +5Vdc is monitored by a reset circuit. A low operating voltage results in a unit reset. All operating voltages including the +5Vdc bus voltage are monitored by measuring them with an internal A/D converter. An alarm is generated if a voltage exceeds its limits.

6.7.2.6 Timing and Loopback Circuitry

The function of the timing block is to provide each interface with clocking and synchronization signals so each interface can transmit data to and receive data from the data interface. The timing and loopback circuitry block also is responsible for providing the loopbacks for all interfaces. The loopbacks are activated by the writing of a specific control register by the microprocessor.

X-bus Interface

The X-BUS interface performs the adaptation between the data formatting circuitry and the data bus and address bus of the DXX subrack. The ECS unit has two ports to the XBUS: X.50 and V.110. The V.110 byte is filled starting from the MSB.

C-bus Interface

The ECS unit communicates with other units of the subrack and with the NMS via the control bus interface. Each unit position in the subrack has an individual address, which is read from the backplane connector. This address is part of the unit identification address used by the DXX. Unit settings can be changed via the control bus with the aid of NMS or a service computer connected to the SCU. The units are also monitored and fault data is collected via the control bus.

V.110/X.50 Converter

The ECS unit multiplexes V.110 channels into X.50 channels and demultiplexes X.50 channels into V.110 channels.

X.50 to V.110 Converter

The X.50 to V.110 conversion block handles four X.50 channels per X50 module. Each module can be configured to search for either the Division 2 or Division 3 framing pattern.

The X.50 to V.110 converter block clocks in the incoming X.50 data and frames on the Division 2 or Division 3 framing pattern. It will search all bit positions for the X.50 framing pattern (this allows the module to frame on X.50 channels received from nonframe-aligned interfaces. It detects framing errors and stores error counts for the Control block to read. It demultiplexes the X.50 stream into individual customer channels in V.110 format. It calculates a CRC on V.110M channels and transmits either V.110(M) data or conditioning to the Timing and Loopback Circuitry block.

V.110 to X.50 Converter

The V.110 to X.50 conversion block handles 30 V.110 channels per X50 module. Each module can be configured to search for either V.110 or V.110M.

The V.110 to X.50 converter block clocks in the incoming V.110 data and frames on the framing pattern. It detects framing errors and stores error counts for the Control block to read. If the channel is configured as V.110M, it detects CRC errors and reports them to the Control block. It multiplexes the V.110(M) channel(s) into any of the four available Division 2 or Division 3 X.50 channels. It transmits either X.50 data or conditioning to the Timing and Loopback Circuitry block.

6.7.3 ECS Fault Monitoring

6.7.3.1 Faults in Block 0

The ECS holds either four or eight identical blocks for X.50 channels numbered 1 through 4 or 1 through 8. The ECS holds either 30 or 60 identical blocks for V.110 channels numbered 9 through 39 or 9 through 69. The common parts are named block 0.

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Alarm
R = Red alarm LED
Y = Yellow alarm LED

Power supply faults monitored in the ECS (Block 0)

Fault Condition	Status	LED
PDF +5V	PMA	R
+12V	PMA	R
-10V	PMA	R
+5V backplane voltage	PMA	R

Faults in Common Parts (Block 0)

Fault Condition	Status	LED
Checksum error		
Checksum error in FLASH memory	PMA + S	R
Checksum error in downloaded SW	PMA + S	R
Operating status faults		
Software unpredicted	PMA + S	R
Unit in reset	PMA	R
Wrong or missing interface module 1	PMA + S	R
Wrong or missing interface module 2	PMA + S	R
ASIC fault in base unit	PMA + S	R
FPGA Error in Interface module 1	PMA + S	R
FPGA Error in Interface module 2	PMA + S	R
Set-up structure error	PMA + S	R
Start permission denied	PMA + S	R
Unit Hardware Error	PMA + S	R
X-bus fault		
Missing IA activity CIF 1 Port 1	PMA + S	R
Missing IA activity CIF 1 Port 2	PMA + S	R
Missing IA activity CIF 2 Port 1	PMA + S	R

Fault Condition	Status	LED
Missing IA activity CIF 2 Port 2	PMA + S	R
Incompatible EPROM/FLASH Program	PMA	R
Bus Sync Fault	PMA + S	R
Module Error fault		
Hardware Errors, Interface Module 1	PMA + S	R
Hardware Errors, Interface Module 2	PMA + S	R
DSP Communication Errors, Interface Module 1	PMA + S	R
DSP Communication Errors, Interface Module 2	PMA + S	R

Memory Faults (Block 0)

Fault Condition	Status	LED
Memory faults		
RAM fault, UBU	PMA + S	R
RAM fault, interface module 1	PMA + S	R
RAM fault, interface module 2	PMA + S	R
EPROM fault	PMA + S	R
FLASH Write Error	PMA	R
FLASH Copy Error	PMA	R
FLASH Erase Error	PMA	R
FLASH Duplicate Error	PMA	R
FLASH Shadow Error	PMA	R

6.7.3.2 ECS IF General Faults

Block 1…8, 8 X.50 Channels

Fault Condition	Status	LED
BER 10	PMA	R
BER 10	PMA	R
BER 10	PMA	R
Frame Far-End Alarm	MEI	Y
AIS	MEI + S	Y
Frame Alignment Lost	PMA + S	R
Channel in Loopback	MEI + S	Y
Unavailable state in terms of CCITT G.821	PMA + S	R
Performance Event	PMA + S	R
Faults Masked	MEI	Y

Block 9…68, 60 V.110(M) Channels

Fault Condition	Status	LED
Frame Far-End Alarm	MEI	Y
AIS	MEI + S	R
Frame Alignment Lost	PMA + S	R
Channel in Loopback	MEI + S	Y
Unavailable state in terms of G.821	PMA + S	R
Performance Event	PMA + S	R
Faults Masked	MEI	Y

6.7.4 Front Panel of ECS Conversion Server Unit

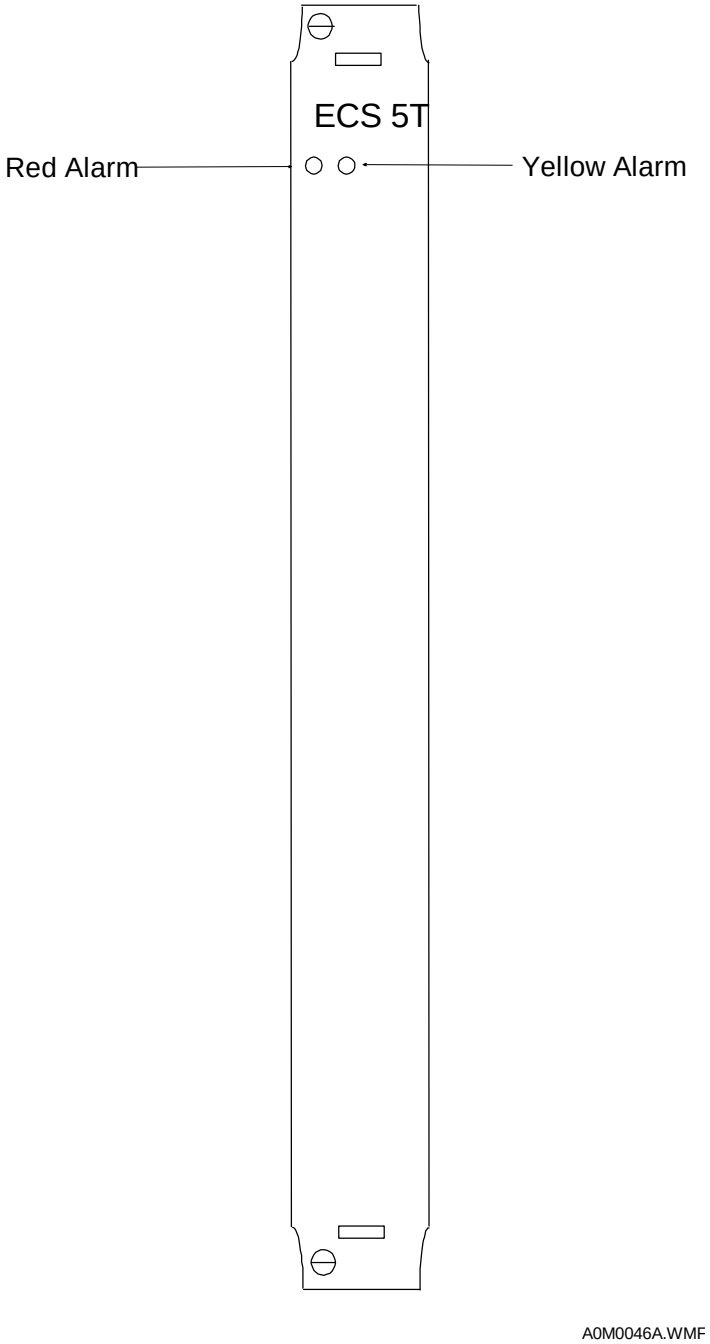


Fig. 54: ECS front panel

6.7.5 Technical Specifications for ECS Conversion Server Unit

Number of X.50 channels per unit: 8 for 10T, 4 for 5T

Number of V.110 channels per unit: 60 for 10T, 30 for 5T

6.7.5.1 X.50 Interface Requirements

The X.50 channel may connected to any Nx64kbit/s data interface. Byte alignment is not required except for 48kbit/s X.50 bis channels.

6.7.5.2 Power Requirements

DC Supply

PDF488 (-48V version)	input voltage:-30 to -60 Vdc
PDF499 (-48V version)	input voltage:-30 to -60 Vdc
PDF489 (+24V version)	input voltage:+19 to +32 Vdc

Power consumption

From DC input voltage (max):

— ECS-5T: 6.5 W
— ECS-10T: 11 W

6.7.5.3 Mechanical Dimensions

Width

one slot unit: 25 mm

two slot unit: 50 mm

Depth

160 mm

Height

244 mm

6.8 EPS Voice Fax Compression Server Unit

6.8.1 General

The EPS Voice Fax Compression server unit has two variants, EPS-5T and EPS-10T.

The EPS-5T converts 4 channels of 64 kbit/s A-law or Mu-law coded PCM voice to either 8 kbit/s Codebook Excited Linear Prediction (CELP) or 16 kbit/s Adaptive Transform Coding (ATC) and vice versa on a per-channel basis.

The EPS-10T converts 8 channels of 64 kbit/s A-law or Mu-law coded PCM voice to either 8 kbit/s CELP or 16 kbit/s ATC and vice versa on a per-channel basis.

6.8.2 Operation of EPS Voice Fax Compression Server Unit

6.8.2.1 EPS Structure

EPS Mechanical Design

EPS-5T Structure

EPS-5T consists of the following base unit and modules:

— UBU 254 universal base unit
— UBZ 441 unit software module
— PDF 488 (-48V) or PDF489 (+24V) power supply module
— EPS 442 voice fax compression module
— RMU 467 bus board for EPS-5T

The power supply module is mounted on the base unit. The EPS-5T is 5T wide and can be used in any IF card slot.

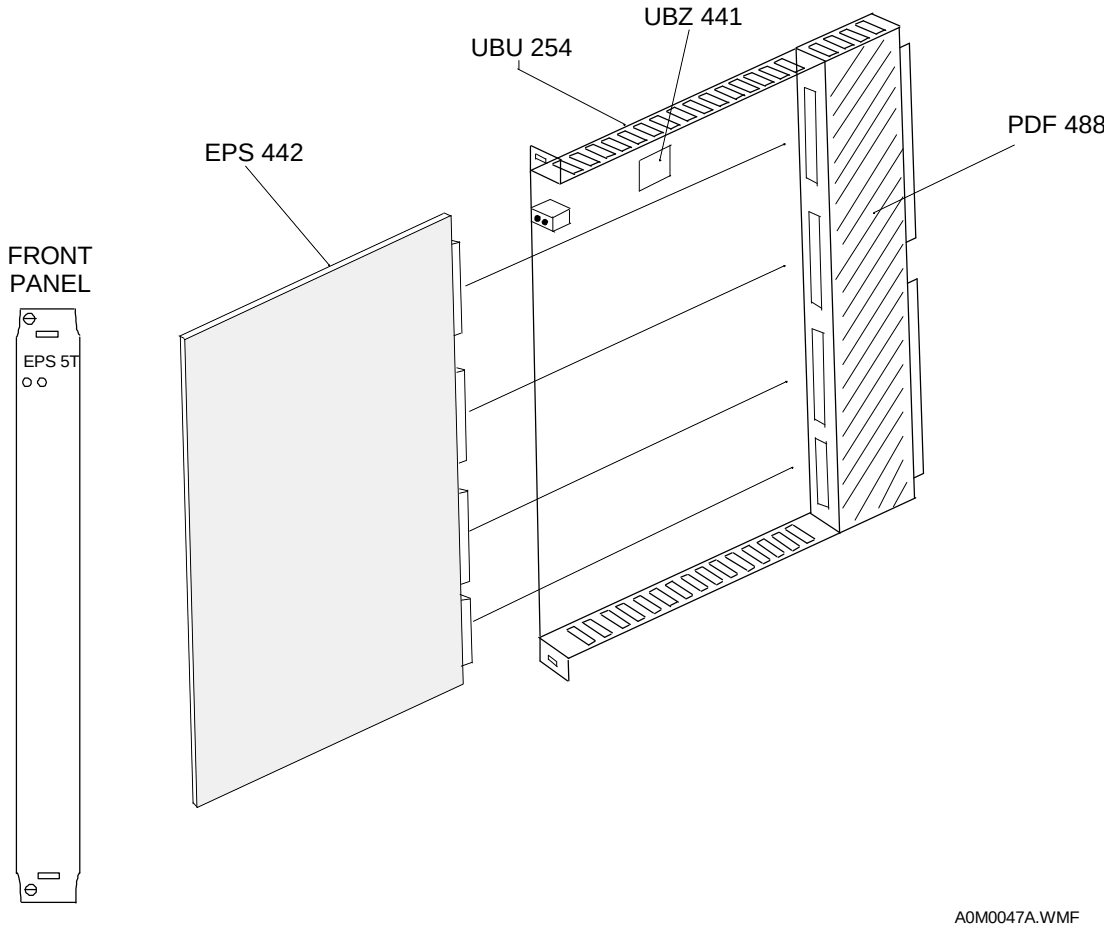


Fig. 55: EPS-5T Structure

EPS-10T Structure

EPS-10T consists of the following base unit and modules:

— UBU 256 cross-connect base unit
— UBZ 441 unit software module
— PDF 499 (-48V) or PDF 489 (+24V) power supply module
— EPS 442 voice fax compression modules, 2 pcs
— RMU 468 bus board for EPS-10T

The base unit is similar to the UBU 254 with the exception that it is equipped with double-wide mechanics (10T). The EPS-10T may be mounted in any IF slot for 10-T units.

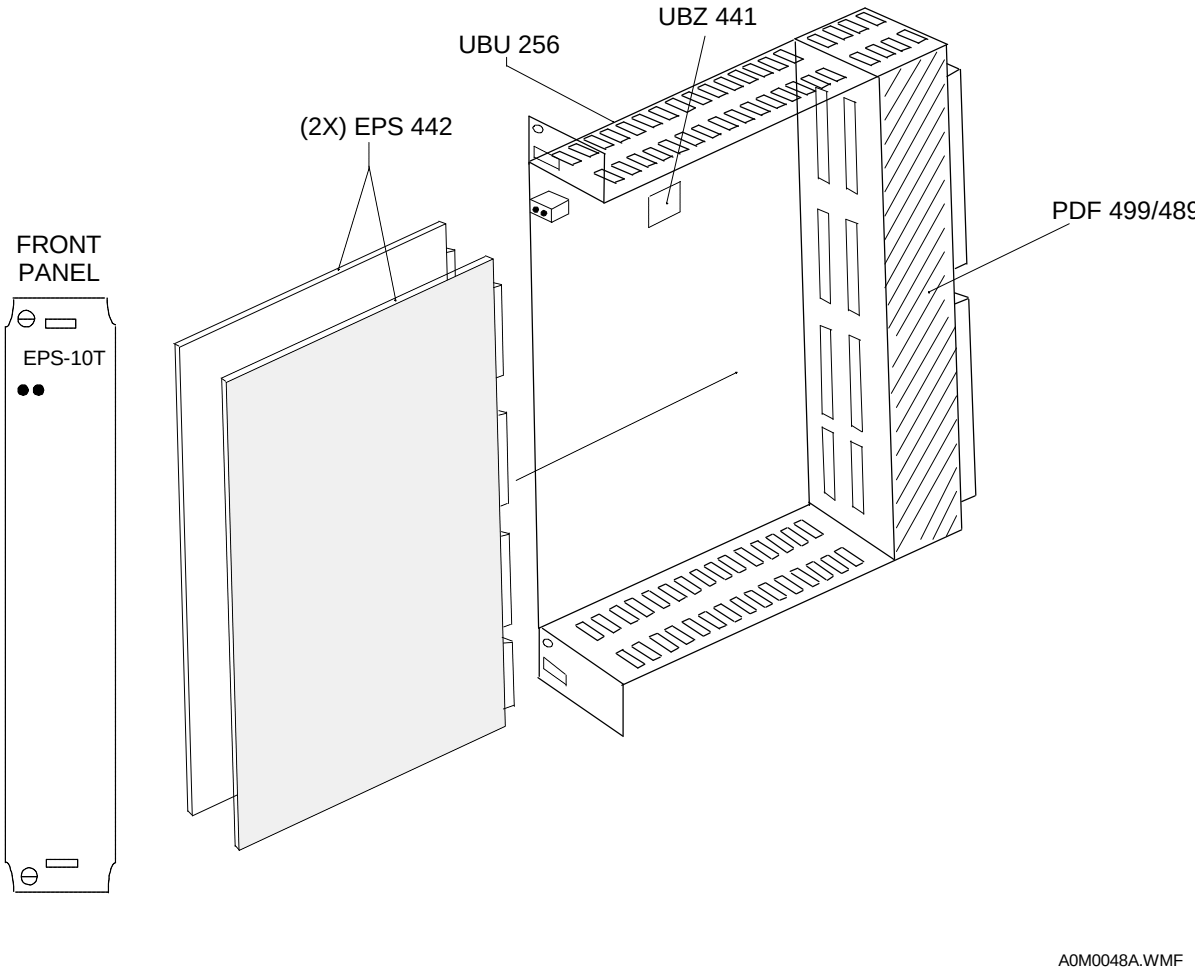


Fig. 56: EPS-10T Structure

EPS Server Block Diagram

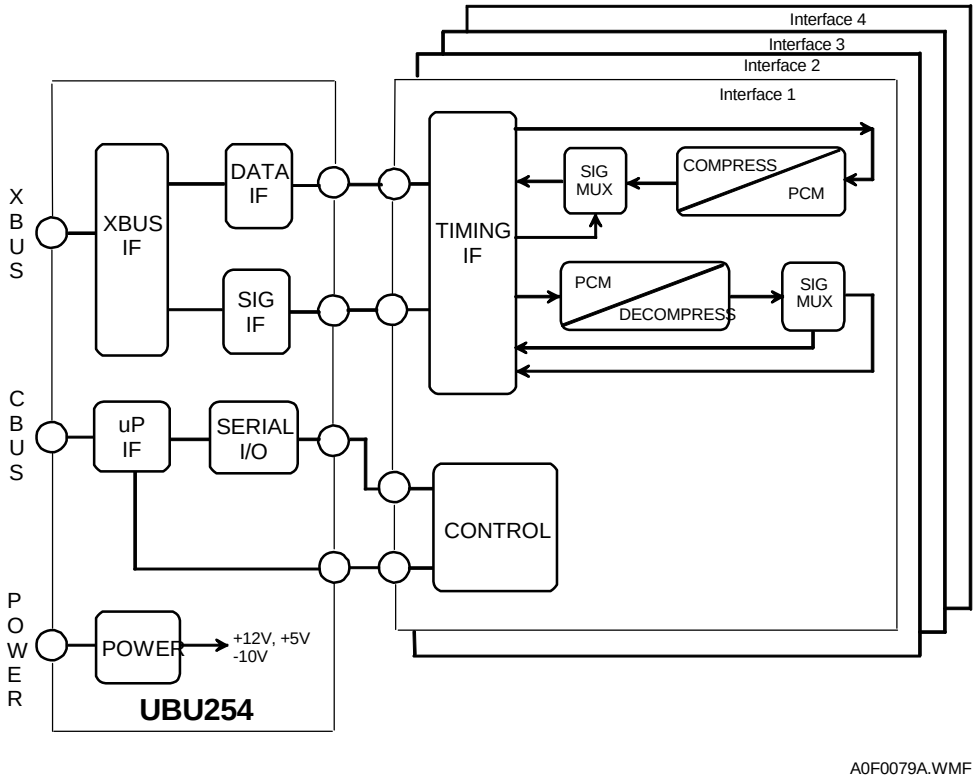


Fig. 57: EPS Server Block Diagram

Configuration Parameters

Compression Rate
The EPS can support either 8 Kb/s (CELP) or 16 Kb/s (ATC) compression rates. Each interface can be independently configured for one of the two compression rates.

PCM Coding
The EPS can support both A-Law even bit inversion and Mu-Law coding.

Signalling

DTMF Relay

The EPS will preserve the integrity of the DTMF tones both at auto-dialer and slower signalling rates. The DTMF tones can be supported up to a maximum rate of 10 pulses per second with a duty cycle of 50 ms on and 50 ms off. The DTMF tones are first detected, then regenerated. The tone frequencies are regenerated at nominal tone frequencies and the levels are regenerated at the detected level.

ABCD Signalling

The user can have ABCD signalling bits pass through the EPS. The signalling bits are multiplexed into the proprietary compressed stream along with the compressed voice or data bits.

AC15 Signalling Relay

The user has the option of activating AC15 signalling. AC15 integrity is preserved by encoding the AC15 inband signals at the near-end, relaying them to the far-end and then regenerating them at the far-end.

The AC15 signalling relay will detect the following call progress tones: dial tone (350Hz and 440Hz), ring back (400Hz, 450Hz), and circuit busy (400 Hz). The AC15 signalling relay will also detect the following signalling tones: idle (continuous 2280 Hz) and digit pulse (gated 2280 Hz).

The detector requires input levels above -29 dBm0. The call progress tones are regenerated at fixed levels of -13 dBm0, and the idle signal is regenerated at a fixed level of -20 dBm0. Digit pulses are regenerated at the detection level.

The idle signal (2280Hz) is detected by band-pass filters with a detection range of ± 50 Hz from the nominal line signal frequency. The idle signal is relayed after 300 mSec of detection. The call progress relay is active only if line signalling is active, and the pulse relay is active if the idle signal is active in the opposite direction. The signal detector has a ± 5% frequency tolerance and will relay dial pulses at rates up to 10 pps.

PAC15 Option

There are two options for the AC15 relay. The PAC15 or pulse dialing option is selected when AC15 switches are converting DTMF to pulse dialing and thus producing consecutive DTMF and AC15 pulse digits. In this case the guard timing of the AC15 register (pulse dialing) and DTMF cannot be guaranteed to relay correctly if applied consecutively. Therefore when selecting the PAC15 option, the DTMF relay is blocked during AC15 line signalling.

DAC15 Option

In some instances the AC15 switches do not convert DTMF digits to AC15 dial pulsing. In such case the DAC15 option gives DTMF-dialed digits precedence during AC15 signalling call setup.

Fax Relay

The EPS automatically transitions from voice compression into fax relay before demodulating and digitally retransmitting data and fax signals if required. The algorithm preserves the automatic rollback of facsimile transmission rates. No configuration parameter changes are required. The following table lists the fax rates supported for the two different compression rates.

Fax Transmission Rates

Parameter	16 kbit/s	8 kbit/s
V.21 300 bps	Yes	Yes
V.27 ter 2400 bps	Yes	Yes
V.27 ter 4800 bps	Yes	Yes
V.29 ter 7200 bps	Yes	Yes
V.29 9600 bps	Yes	No

NSF Option

Some fax machines support non-standard facility (NSF) features such as encryption, security mailbox or proprietary modulation schemes. In case the user knows that both end-to-end machines are using NSF features, this option must be enabled. The feature will also work with standard fax machines because the answering machine must respond with an NSF identifier. If the orginating NSF machine does not receive this identifier, it assumes the answering end is a standard machine and switches to standard operation.

Data Transparency

The EPS can preserve the integrity of data signals at 16 kbit/s compression rate which conforms to the standards listed in the table below. The algorithm preserves the automatic rollback of modem transmission rates. No configuration parameter changes are required.

Data Transmission Rates

Parameter	16 kbit/s	8 kbit/s
Bell 103 300 bps	Yes	No
V.22 1200 bps	Yes	No
V.22 bis 2400 bps	Yes	No

Echo Cancellation

The echo canceller provides 32 ms of end-path cancellation. During fax transmission the algorithm automatically adjusts the echo canceller state and returns it to normal at the end of the transmission.

The echo cancellation can be disabled if necessary. It is recommended that when running external diagnostics using analog tones the echo canceller is disabled. In normal operation the echo canceller should be set to enabled.

6.8.2.2 Unit Controller

The EPS unit is controlled by a 16-bit 80C188 microprocessor running at 20 Mhz. The unit processor links the subrack to the NMS via a VTP bus. The application program is stored in an interchangeable EPROM or FLASH memory; the FLASH can be used to download updates to the application program. The unit's number and configuration parameters are stored in a non-volatile FLASH memory. This allows the unit to restore to its original state should a power loss occur. A watchdog circuit monitors the operation of the processor and generates a unit reset when the circuit is triggered.

6.8.2.3 Power Supply

EPS-5T/10T receives its power from the unit power supply module PDF 488/499 or PDF489. The switching power supply provides three regulated output voltages: +5VDC, +12VDC and -10VDC. Battery voltage is fed from the DXX bus to be used as supply voltage for the PDF488/499 power supplies. The module also receives +5VDC bus voltage supplied for start-up conditions to the interface circuits connected to the bus. The +5VDC generated by the unit is monitored with a reset circuit. A low operating voltage results in a unit reset. All operating voltages including +5VDC bus voltage are monitored by measuring them with an internal A/D converter. An alarm is generated if a voltage exceeds its limits.

6.8.2.4 Timing and Control

The function of the timing interface block is to provide each interface with clocking and synchronization signals so each interface can transmit and receive data and signalling to/from the data and signalling interface. The timing and control block is also responsible for providing bidirectional PCM loop back for all four interfaces. The loop back is activated by the microprocessor writing a specific control register.

6.8.2.5 X-Bus Interface

The X-bus interface performs the adaptation between the data formatting circuitry and the data bus and address bus of the DXX subrack.

The EPS unit has three ports to the X-bus: PCM, compressed, and signalling. The compressed byte is filled by starting from the MSB.

Signal Mapping

The signalling bits for each interface are normally mapped to the interface from the XD-bus by the SXU. The signalling bits are then multiplexed into the compressed stream along with the data. The process of multiplexing the signalling bits onto the compressed stream is handled by the algorithm.

Signal Mapping

Encoding	XB Rate	TS Bit Usage	Signalling Bits Supported
ATC	16 kbit/s	B7…B8	a, b, c, d
CELP	8 kbit/s	B8	a, b, c, d

6.8.2.6 C-Bus Interface

The EPS unit communicates with other units of the subrack and with the NMS via the control bus interface. Each unit position in the subrack has an individual address which is read from the back plane connector. This address is part of the unit identification address used by the DXX. Unit settings can be changed through the control bus with the aid of a service computer connected to the SCU. The units are also monitored and fault data is collected through the control bus.

6.8.2.7 Echo Cancellation

Echoes occur in the network when converting analog 4-wire circuits to 2-wire circuits in which hybrids are involved. Poor hybrid balance is not the single factor that makes the echoes more noticeable and annoying to the human ear. Misaligned levels in the 4-wire circuits can reduce the amount of hybrid balance. However, the amount of transmission delay causes the echoes to be more noticeable. For this very reason an echo canceller is used to remove potential echoing.

The echo canceller samples the outgoing PCM (PCM OUT) and models the hybrid and end-path tail circuit. The canceller then produces an equal but opposite signal and subtracts that from the incoming path. The echo canceller can produce up to 32 mSec of end-path cancellation. The canceller protects the far-end listener from echoes generated at the near-end.

6.8.2.8 Compression/Decompression Blocks

Normal speech samples enter via a PCM IN port from the near-end. It passes through the 8K CELP, or 16K ATC. Out-of-band signalling such as ABCD signalling bits are multiplexed and synchronized along with the encoded speech into a compressed stream labelled Compress Out.

From the opposite direction or from the far-end the compressed data enters a port labelled Compress In. Speech is decoded and out-of-band signals are stripped off by a demultiplexing circuit and sent to the signalling bus. PCM data leaves toward the near-end via a port labelled PCM OUT.

A detector is used to analyse the presence of fax or in-band signals. When one of these is detected, the encoder transitions to allow the fax relay to demodulate the transmitting fax machine data. This digital data is then multiplexed into the compressed stream.

In the opposite direction the fax digital data is converted by the fax converter block and passed into the receiving fax machine.

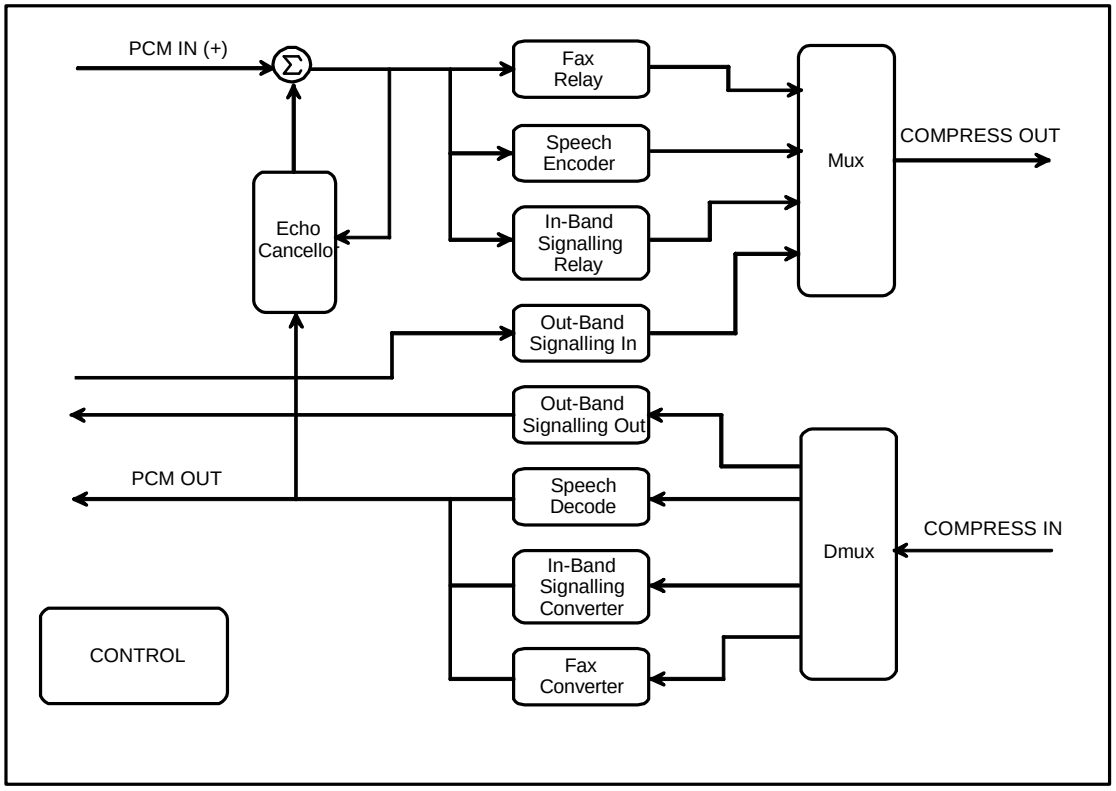


Fig. 58: Compression/Decompression Block Diagram

6.8.2.9 Loop Backs

The NMS is able to control two loops per interface in the EPS unit. Loops and measurement points are used to isolate faulty equipment and to detect faulty directions. The unit includes a loop back time-out control on a per channel basis which will turn off a loop when the user-defined time has come to an end. Bit pattern tests (BERT) cannot be used to isolate problems through the compression algorithm. The compression algorithm does not reproduce the bit pattern in the same manner as it does an analog tone or speech.

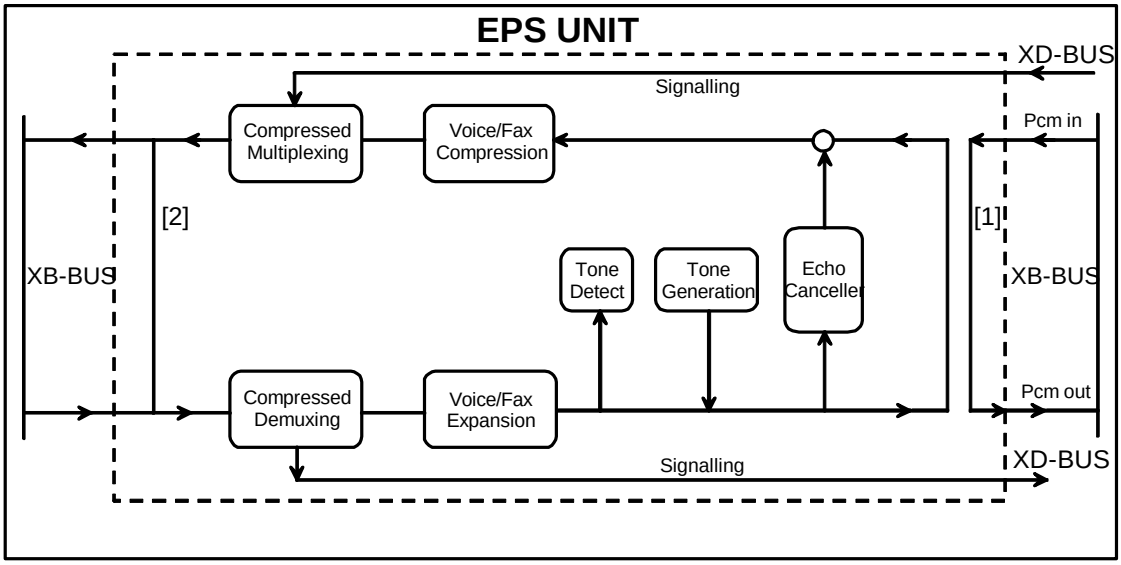


Fig. 59: EPS Loop Backs and Diagnostics

PCM Loop Back

A PCM loop back [1] is designed into the module for each interface. This loop back is a bidirectional loop back with loops toward the PCM source and a loop back toward the core. The PCM data toward the EPS is intercepted and looped back toward the source of the PCM. The other end takes the data from the voice decompression block and loops it back to the voice compression block.

Compressed Loop Back

A compressed side loop back [2] is designed into the module for each interface. This loop back takes the compressed data out of the packets and loops them to the demultiplexing data in the block. This loop allows the user to have tones pass through the entire unit to verify the status of the unit.

6.8.2.10 Tone Generation

A tone generator is designed into the module for each interface to give the user the ability to generate tones internally for troubleshooting. The user has control through the NMS to generate two unique tones at three unique levels. In order to generate a tone, tone generation must be ON (see Fig. 59). The table below lists the user options.

Tone Generation

Tone Frequency	Tone Level	Generation State
Digital mW 1000 Hz	0, -10, -23 dBm	On/Off
1020 Hz Sine wave	0, -10, -23 dBm	On/Off

6.8.2.11 Tone Detection

The user has the ability of measuring internally the level and frequency. A detection circuit is designed into the module for each interface. The user can use this only if the tone generation parameter is enabled. It is possible to isolate a particular problem to the path (transmit/receive) by using external test equipment with the internal generator. By selecting the external equipment to generate a tone different from the internal tones available, the internal level/frequency detector can measure the external tone, and the tone generated internally can be measured by the external equipment.

When the internal generator is activated, software automatically disables the echo canceller and returns it to normal state when the internal generator is deactivated. During diagnostics the state of the echo canceller does not change in the configuration menus of the NMS.

Whenever the user is isolating problems with external equipment while at the same time activating internal interface loops, it is recommended that the echo canceller is disabled by the user during the diagnostics.

6.8.3 Faults and Actions in EPS Voice Fax Compression Server Unit

6.8.3.1 Fault Conditions

The EPS holds either four or eight identical blocks numbered 1 through 4 or 1 through 8. The common parts are named block 0.

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Affecting Fault
R = Red alarm LED
Y = Yellow alarm LED

EPS Faults Conditions (Block 0)

Fault Condition	**Status**	**LED**
Power supply		
+5V, +12V, -10V, +5V	PMA	R
+5V back plane voltage	PMA	R
Fault Condition	Status	LED
Checksum error		
- in FLASH memory	PMA+S	R
- in downloaded SW	PMA+S	R
Incompatible SW revisions	PMA+S	R
Operating status faults		
UBU reset	PMA	R
Unit not registered	PMA+S	R
Missing module	PMA+S	R
Conflict in module type	PMA+S	R
ASIC fault in base unit	PMA+S	R
ASIC fault in module	PMA	R
Software unpredicted	PMA+S	R
Setup structure corrupted	PMA	R
Start permission error	PMA	R
X-bus fault		
Missing IA activity	PMA+S	R
SW in FLASH incompatible with EPROM	PMA+S	R
UBU to server module comm error	PMA+S	R
Memory faults		
RAM, EPROM fault	PMA+S	R
FLASH fault	PMA+S	R

EPS IF Fault Conditions (Block 1…8)

Fault Condition	Status	LED
DSP readback failure	PMA+S	Red
Fault mask	MEI	Y
Loop back on	MEI	Y

6.8.4 EPS Front Panel

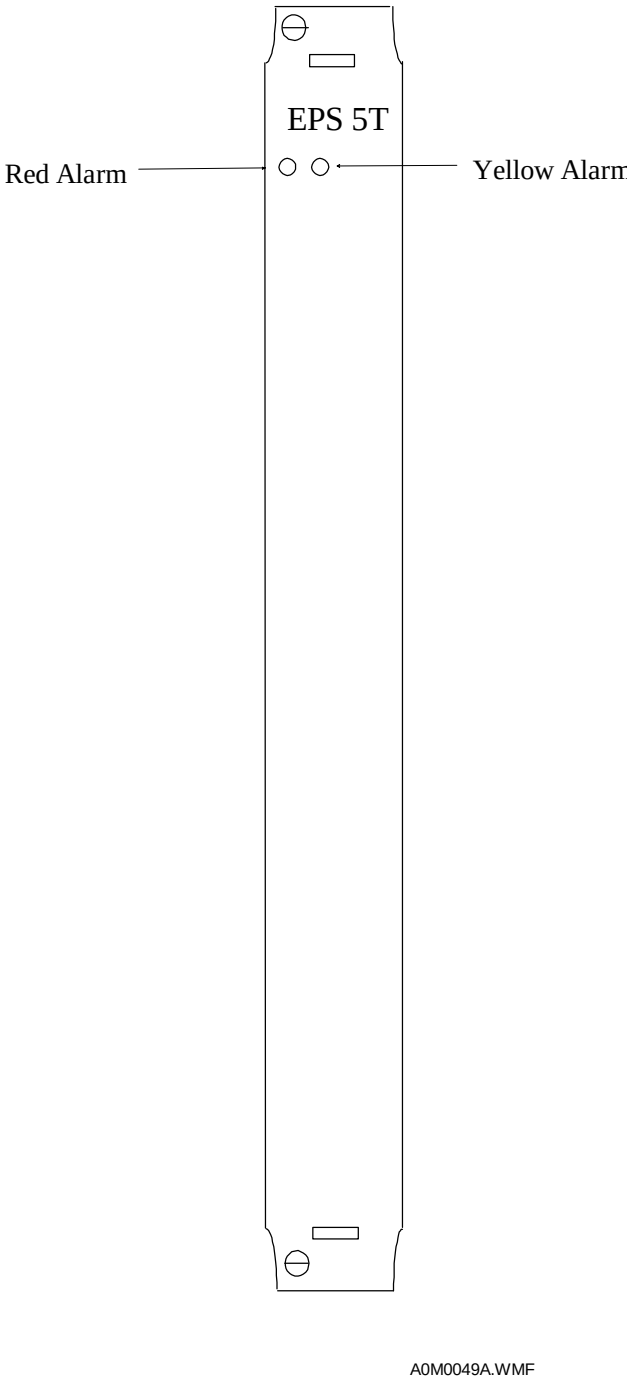


Fig. 60: EPS Front Panel

6.8.5 Technical Specifications for EPS VOice Fax Compression Server Unit

Number of channels per unit		
in EPS-10T	8	
in EPS-5T	4	
Voice coder specifications		
Type of encoding	16 kbit/s ATC	
	8 kbit/s CELP	
Signal/noise ratio	> 30 dB	
(1004 Hz @ 0 dBm0 Single tandem, single tone)		
End-to-end delay (excluding transmission links)		
16 kbit/s	less than 80 ms	
8 kbit/s	less than 150 ms	
Magnitude transfer response		
(1004 Hz @ 0 dBm0)	600 - 3500 Hz	± 0.5 dB
	300 - 3500 Hz	± 1.5 dB
	100 - 3900 Hz	± 15 dB
Echo canceller		
End path cancellation	32 mSec	
DTMF detection		
frequency deviation	± 1.4 % max. of nominal	
level range	0 to - 25 dBm	
pulse duration	40 mSec minimum	
interdigit duration	40 mSec minimum	
pulse interval	93 mSec minimum	
(Pulse on + Pulse off)		
DTMF regeneration		
frequency deviation	± 0.5 % of nominal	
level range	± 3 dB (of detected valid level)	
Tone generation		
frequency accuracy		
1020/1000 Hz	± 0.5%	
level accuracy 1020/1000Hz	± 0.5 dB	
Tone detection		
frequency accuracy	± 0.5%	
frequency resolution	1 Hz	
level range	0 to - 45 dBm	
level accuracy	± 0.5 dB	
level resolution	0.1 dB	

6.8.5.1 Power requirements

DC Supply

- PDF488 (-48V version)	input voltage -30 to -60 VDC
- PDF499 (-48V version)	input voltage -30 to -60 VDC
- PDF489 (+24V version)	input voltage +19 to +32VDC

Power consumption

From DC input voltage	
EPS-5T	9 W
EPS-10T	17 W

6.8.5.2 Mechanical Dimensions

Width	
- one-slot unit	25 mm
- two-slot unit	50 mm
Depth	160 mm
Height	244 mm

6.9 ESO V5.1 Server Unit

6.9.1 General

DXX ESO is a server unit with no physical line interfaces. The ESO provides V5.1 signaling protocol capability to the DXX product family. As such, it supports all of the features, functions and interfaces needed to both support V5.1 networking services and to interface to the DXX product family.

Physically the ESO consists of DXX base module UBU254 that interfaces DXX cross-connection and control bus and of ESO570 V5.1 processor module Together they form a single DXX unit ESO.

6.9.1.1 Normative General Standards

ETS 300 324-1, “Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange, V5.1 Interface for the support of Access Network” February 1994.

6.9.2 Operation of ESO V5.1 Server Unit

6.9.2.1 Mechanical Design

The mechanical design of the ESO unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; however, the general recommendations for subrack equipping should be followed.

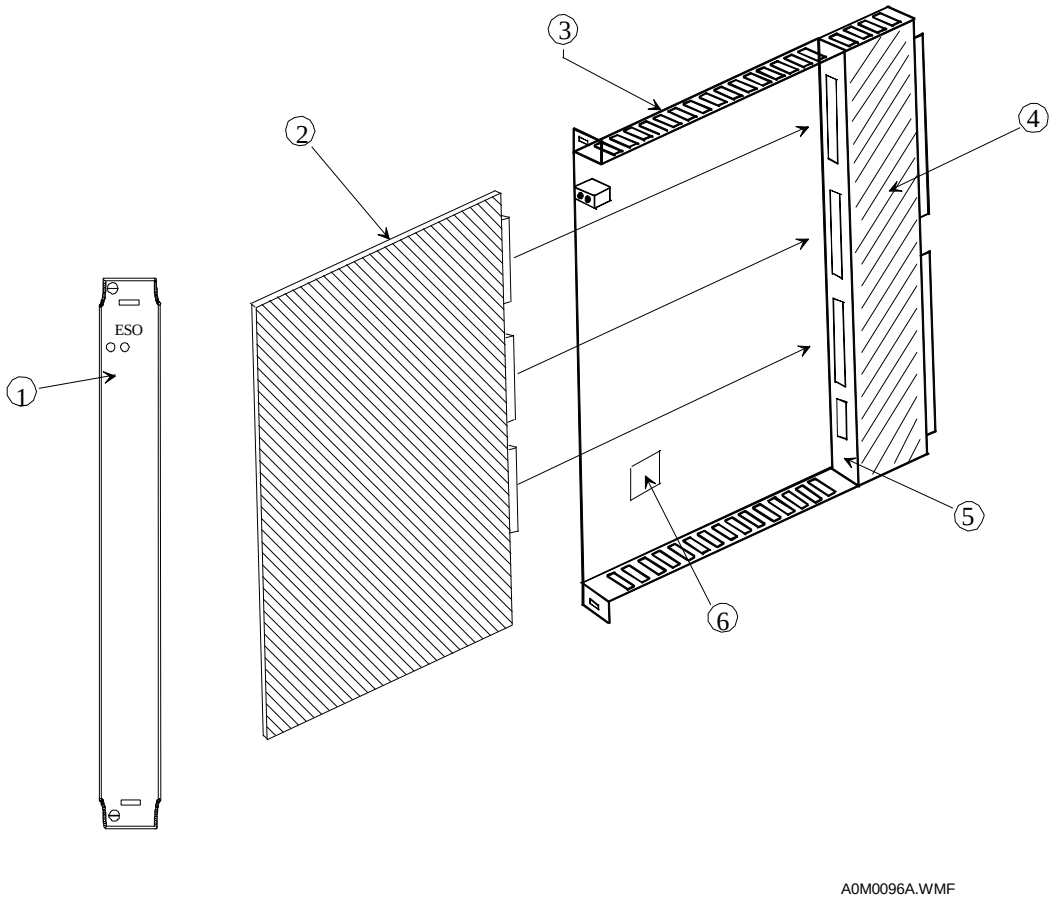


Fig. 61: ESO Mechanical Structure

1	Front Panel
2	V5 signaling Processor ESO570
3	Universal Base Unit UBU254
4	Power Supply Unit PDF488
5	Backbone bus unit RMU465
6	Flash EEPROM UBZ536

The UBZ 536 is a user replaceable Flash EEPROM located on the UBU254.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

Application

The ESO allows the DXX to be used as an access network connected to a local exchange that conforms to the V5.1 standard: ETS 300 324-1. The ESO is a server module, and provides no physical interfaces. The ESO can support one or two V5.1 interfaces to the LE. Each V5.1 interface can support a maximum of 14 BRI-ISDN user ports using the ISD-LT line interface unit, or 30 PSTN user ports using the CCS-UNI line interface unit. For PSTN, the ESO supports the exceptions and modifications to the V5.1 standard for several countries. The ESO also provides three C-Channels per V5.1 interface. Provisioning of the C-Channels is performed with the NMS. Combinations of ISDN and POTS user interfaces are supported.

Block Diagrams

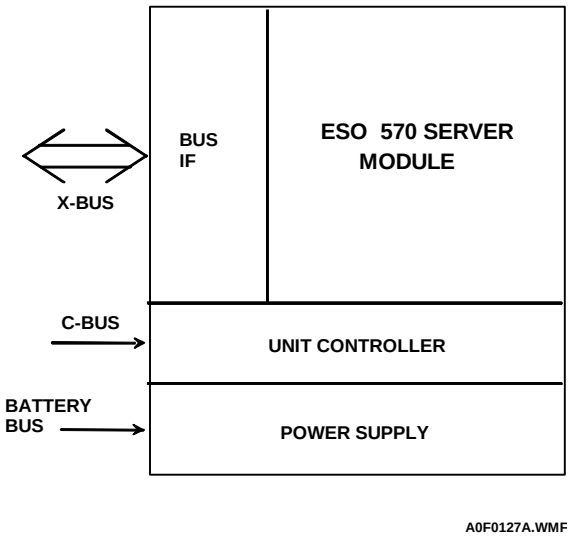


Fig. 62: Functional Structure of ESO

The ESO unit includes the power supply, the processor and its peripheral circuits, various interfaces for the interface module and an X-bus interface.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored by the UBU CPU and a functional disturbance activates a fault message.

NOTE! ***The power supply will function only with a -48V battery input. 24V Battery operation is not supported.***

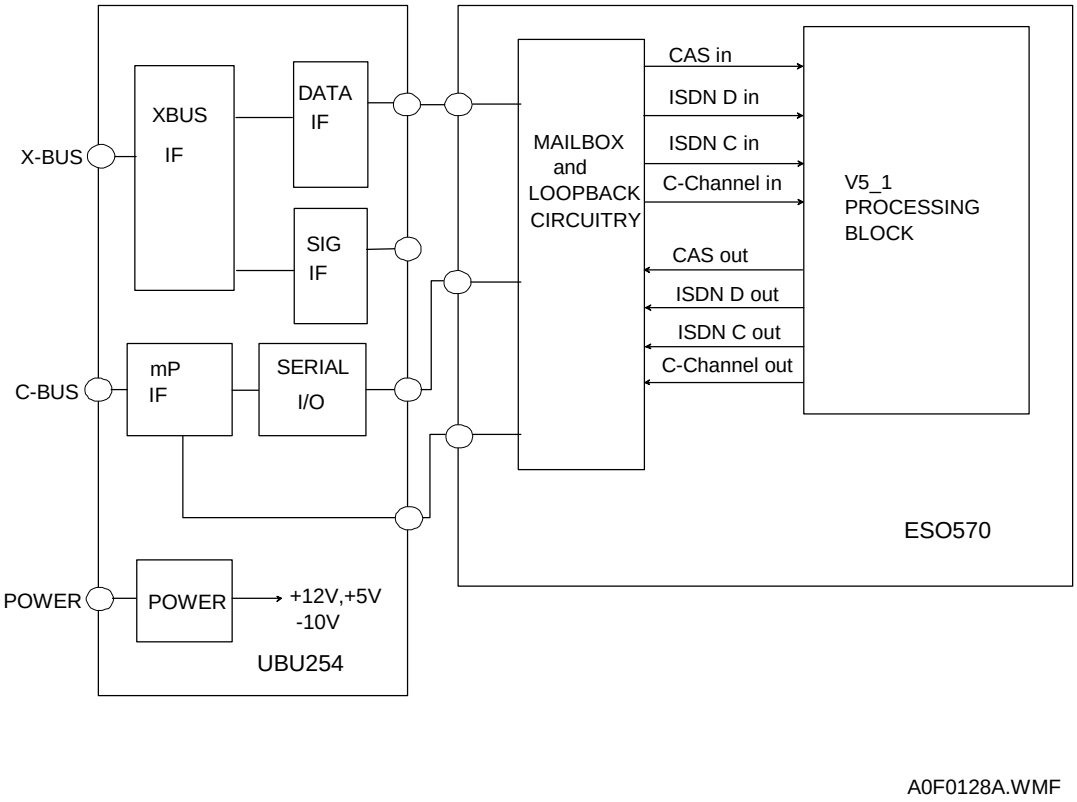


Fig. 63: Functional Block Diagram of ESO

The ESO consists of the following base unit and modules:

— Universal Base Unit (UBU254)
— Backbone bus unit (RMU465)
— Power Supply Unit (PDF488)
— V5 signaling Processor (ESO570)

6.9.2.2 Functional Blocks

The main functional blocks of the ESO include Universal Base Unit (UBU 254), V5 signaling Processor (ESO570), Unit power supply (PDP488), backbone bus (RMU465). The ESO occupies 1 slot (5T) in DXX node.

Universal Base Unit (UBU 254)

The UBU includes power supply, processor with its peripheral circuits, various interfaces for interface modules, and an X-bus interface. The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to the control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack.

Communication between the Ericsson DXX Manager and the ESO shall be via the UBU/ESO control interface. This control interface shall allow the Ericsson DXX Manager to completely control the ESO's configuration management, fault management, performance management, accounting management, general MIB access and software download functions.

Processor and memory: The unit is controlled with an 80C188 microprocessor. The common part of the UBZ536 program is stored on the board in an interchangeable FLASH EEPROM-memory. The application part of UBZ536 can also be stored in EEPROM, but may be stored in non-volatile FLASH memory. Thus, it is possible to update the application part without removing the unit from its operating environment. The non-volatile memory is also used to store the unit's operating parameters and the unit number so that in the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM memory of the processor operates as a working storage.

V5 Signaling Server Module (ESO570)

The ESO is designed to function in the DXX. Major components of ESO 570 are, QUICC CPU, memory, FPGA, boot program, and application program. The following is a brief functional description of major components.

QUICC CPU: The ESO570 contains one high speed MC68MH360 QUICC CPU to satisfy all processing requirements. The processor bus connects with SRAM, boot FLASH PROM, a Dual Port RAM, an FPGA and two banks of application FLASH memory.

Memory: Four types of memory are implemented in the ESO570: SRAM, Boot FLASH, application FLASH and Dual Port RAM. SRAM is used for parameter and data storage. The two banks application FLASH memory contain the operation code and can be downloaded from the DXX NMS. The boot FLASH PROM contains the initial boot code for the processor and is used at power up. The Dual port RAM is used for communication between the UBU254 and the ESO570 CPU.

FPGA: The FPGA on ESO570 board is an SRAM based device. The FPGA image is programmed on UNIT reset and power-up by a serial bus from the UBU254. The FPGA acts as a transceiver for the ISDN C8 links and CAS signaling. The FPGA translates signalling data to/from the CIF data streams and the CPU accesses that data in Dual port RAM contained within the FPGA.

Boot Program: The boot program is the stored program responsible for executing the power up sequence of the ESO570. The program performs board diagnostics and starts the application program, if a valid load is found. If a valid application program is not found, the boot program enters into a mode that is capable of downloading an application program. The boot program resides in a 256 Kbyte FLASH part, and cannot be modified.

Application Program: The application program is stored in application FLASH memory, and is responsible for implementing the V5.1 standard. The application program is started by the Boot Program. After initialising itself, the program processes CAS signalling from PSTN user ports, converting the bit oriented CAS into the message based signalling scheme defined in [1]. The application also processes ISDN D-channel signalling by performing the frame relay function defined in [1]. After conversion the user side signalling is sent to a local exchange via 64 Kbps bi-directional C-Channels. Finally, the application program is used to configure each V5.1 interface, and can be modified via a software download from the DXX network management system.

Power Supply

The unit receives its operating voltage from the PDF488power supply module. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in the place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, and +12V to the UBU and ESO570, modules. The module also receives a +5V bus voltage from the shelf backplane, which during start-up conditions is supplied to the interface circuits connected to the backplane buses. The +5V operating voltage from the PDF is monitored with a reset-circuit and a low operating voltage results in unit reset.

6.9.2.3 Interface Modules

There are no line interfaces on the ESO itself. All subscriber side ISDN D-channel, and PSTN CAS signalling traffic processed by the ESO is cross-connected from an appropriate interface module (e.g. ISD-LT, CCS-UNI) to the ESO. The processed signalling is carried to a local exchange via C-Channels. Each V5.1 interface can support up to 3 C-Channels. The C-Channels must be cross-connected from the ESO, to a 2MB line interface module (e.g. GMH). Additionally, the bearer traffic from the subscriber side interface module must be cross connected to the line interface module.

6.9.3 Fault conditions in ESO V5.1 Server Unit

6.9.3.1 General

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
S = Service Affecting Fault
MEI = Maintenance Event Information
R = Red alarm LED
Y = Yellow alarm LED

The following table contains all the faults that can be monitored in the ESO, as well as the reaction of the unit to each fault. In the Indication column, R or Y indicates that the red or yellow LED is turned on, respectively. The block number defines the source of the fault indication as follows:

Block 0	ESO unit level block that reports UBU and ESO570 faults such as ROM, RAM, and FLASH memory failures, as well as other general unit faults.
Blocks1 and 2	2.048 Mbps V5.1 interface-related faults, which includes V5.1 protocol errors and channel loop-back and AIS indications. V5.1 interface 1 faults are reported in block 1 and interface 2 faults are reported in block 2.

6.9.3.2 Block 0 :

Fault Condition	**Severity**	**Indication**	**GPT**	**SPT**
Software Unpredicted	MON+MAJ	PMA+S+R	1	1
Unit in Reset	MON+MAJ	PMA+R	2	2
Power Supply Faults:				
Backplane +5V	MON+MAJ	PMA+R	4	3
PDF +5V	MON+MAJ	PMA+R	4	4
+12V	MON+MAJ	PMA+R	4	5
-10V	MON+MAJ	PMA+R	4	6
RAM Faults:				
UBU	MON+MAJ	PMA+S+R	5	7
Interface module 1	MON+MAJ	PMA+S+R	5	8
EPROM Fault	MON+MAJ	PMA+S+R	5	9
BOOT PROM Fault	MON+MAJ	PMA+S+R	5	10
FLASH Write Error				
UBU	MON+MAJ	PMA+R	5	11
Interface module 1	MON+MAJ	PMA+R	5	12
FLASH Copy Error	MON+MAJ	PMA+R	5	13
FLASH Erase Error				
UBU	MON+MAJ	PMA+R	5	14
Interface Module 1		PMA+R	5	15
FLASH Duplicate Error	MON+MAJ	PMA+R	5	16
FLASH Shadow Error	MON+MAJ	PMA+R	5	17
FLASH Checksum Error	MON+MAJ			

Fault Condition	Severity	Indication	GPT	SPT
UBU	MON+MAJ	PMA+S+R	5	18
Interface Module 1		PMA+S+R	5	19
Setup Structure Error	MON+MAJ	PMA+S+R	5	20
Wrong or Missing Interface module	MON+MAJ	PMA+S+R	10	21
ASIC Error	MON+MAJ	PMA+S+R	32	22
Unit Hardware Error	MON+MAJ	PMA+S+R	32	23
Interface Module FPGA Error	MON+MAJ	PMA+S+R	32	24
Start Permission Denied	MON+MAJ	PMA+S+R	36	25
Bus Sync Fault	MON+MAJ	PMA+S+R	38	26
IA Activity Missing:				
CIF 1 Port 1	MON+MAJ	PMA+S+R	40	27
CIF 1 Port 2	MON+MAJ	PMA+S+R	40	28
Incompatible EPROM/ FLASH Program	MON+MAJ	PMA+R	55	29
Downloaded Program Checksum Error	MON+MAJ	PMA+S+R	55	30
Interface Module Hardware Error	MON+MAJ	PMA+S+R	62	31
MC68MH360 communication errors	MON+MAJ	PMA+S+R	62	32
Interface Module Configuration configuration not restored	MON+MAJ	PMA+S+R	77	80
Interface Module Reset	MON+MAJ	PMA+S+R	2	81

6.9.3.3 Blocks 1 and 2 (2.048Mbps V5.1 links - C-channels as provisioned) :

Fault Condition	Severity	Indication	GPT	SPT
AIS (Cessation of flags on provisioned C-channel)	MON+MIN	MEI+S+Y	23	33
Channel in Loopback	MON+WARNING	MEI+S+Y	27	34
Faults Masked	MON+WARNING	MEI+Y	58	35

V5.1 Protocol Stack Core Management Entity Errors

Fault Condition	Severity	Indication	GPT	SPT
Activation Failed	MON+WARNING	MEI+R	79	36
Interface ID Not Identical	MON+WARNING	MEI+R	79	37
Variant ID Not Identical	MON+WARNING	MEI+R	79	38
Variant Does Not Exist	MON+WARNING	MEI+R	79	39
Internal Failure	MON+WARNING	MEI+R	79	40
Attempt to Switch to Same Variant	MON+WARNING	MEI+R	79	43

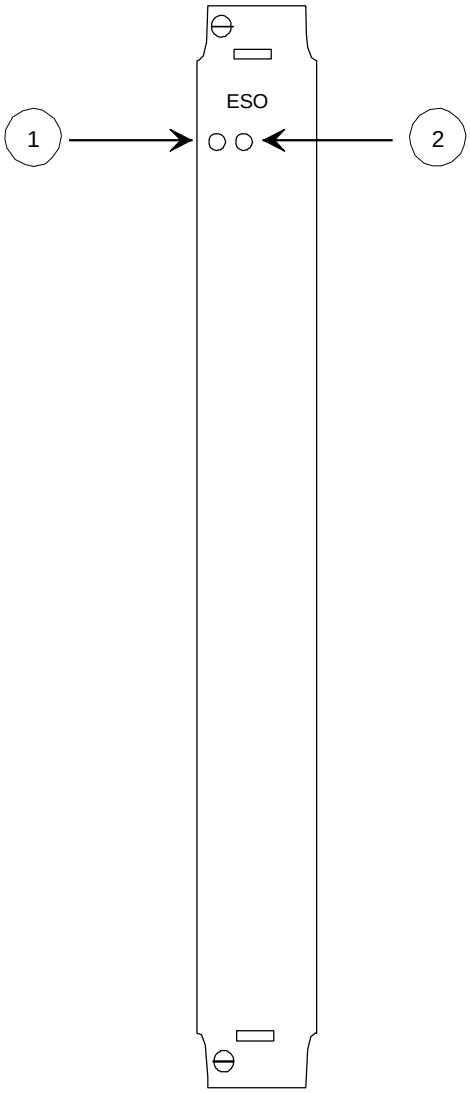
V5.1 Protocol Stack Protocol Errors

Fault Condition	Severity	Indication	GPT	SPT
Protocol Discriminator Error	MON+WARNING	MEI+R	77	44
L3addr Error	MON+WARNING	MEI+R	77	45
Message Type Unrecognised	MON+WARNING	MEI+R	77	46
Out of Sequence Information Element	MON+WARNING	MEI+R	77	47
Repeated Optional Information Element	MON+WARNING	MEI+R	77	48
Mandatory Information Element missing	MON+WARNING	MEI+R	77	49
Unrecognised Information Element	MON+WARNING	MEI+R	77	50
Mandatory Information Element Error	MON+WARNING	MEI+R	77	51
Optional Information Element Error	MON+WARNING	MEI+R	77	52
Message Not Compatible with Path State	MON+WARNING	MEI+R	77	53
Repeated Mandatory Information Element	MON+WARNING	MEI+R	77	54
Invalid Sequence Number Received	MON+WARNING	MEI+R	77	55
Next Sequence Number Unavailable	MON+WARNING	MEI+R	77	56
Tt Timer Expired	MON+WARNING	MEI+R	77	57
T3 Timer Expired 3rd Time	MON+WARNING	MEI+R	77	59
Message Received is Too Short	MON+WARNING	MEI+R	77	60
Message Received is Too Long	MON+WARNING	MEI+R	77	61
Too Many Information Elements	MON+WARNING	MEI+R	77	65

V5.1 Protocol Stack Protocol Errors

Fault Condition	Severity	Indication	GPT	SPT
Control Function Error	MON+WARNING	MEI+R	77	66
Message Received During Out of Service State	MON+WARNING	MEI+R	77	70
Timer T01 Expired 2nd Time	MON+WARNING	MEI+R	77	71
Timer T02 Expired 2nd Time	MON+WARNING	MEI+R	77	72

6.9.4 Front Panel



A0M0095A.WMF

Fig. 64: ESO front panel

Fig. 64 represents the front view of ESO front panel. It has to be removed if replacing user configurable FLASH EEPROM on UBU.

6.9.5 Technical Specifications

Number of V5.1 Links Supported	2
Maximum Number of ISDN D-Channels per link	14
Number of C-Channels per link	1-3
Input Voltage (ESO will work only on a -48v battery supply)	-30V to -60V DC
Power Consumption	4.78W
Physical Dimensions	
Width	25 mm
Height	244 mm
Depth	160 mm

6.9.5.1 Environmental Specifications

Temperature and Humidity

The ESO shall be capable of continuous operation at ambient temperatures of +5 degree C to 40 degree C and relative humidity <85%, non-condensing and exceptional operating conditions of ambient temperature -5 degree C to +45 degree C and relative humidity < 90%. Refer to ETS 300 019-1-7: 1992 classification of environmental conditions.

Electromagnetic

ESO meets standard of Public Telecommunication Equipment, ETS 300386-1:1994, Table 4.

6.10 FRU Frame Relay Server Unit

6.10.1 General

The FRU product is an application for local Frame Relay switching and concentration serving LAN interconnect through the DXX system. With this product DXX provides a managed Frame Relay transport and access service for branch office types of customers who need to access Frame Relay backbone services with a low capacity (0 kbits/s- 2 Mbit/s).

6.10.1.1 FRU General Description

DXX Frame Relay Unit (FRU) is a server unit with no physical line interfaces. The FRU provides an embedded Frame Relay (FR) networking capability to the DXX product family. As such, it supports all of the features, functions and interfaces needed to both support FR networking services and to interface to the DXX product family.

Logically the FRU consists of DXX base module UBU that interfaces DXX cross-connection and control bus and of FR engine that does FR core functions. Together they form a single DXX unit FRU.

6.10.1.2 General Solution

An FRU is connected to another FRU via Frame Relay Virtual Trunk of which 5 percent of the bandwidth is reserved for the control traffic. The trunk bandwidth may be oversubscribed in order to take advantage of the statistical nature of packet-switching. This oversubscribed bandwidth is called Virtual Bandwidth.

FRUs use OSPF routing protocol to find the best path to send traffic over. FRUs send out Link State Updates every 30 minutes, collect Link State Updates and place them in a Link State Database. Each node runs the Dijkstra algorithm on the Link State Database which results in a tree of shortest paths throughout the Frame Relay network (built up by FRUs).

Frame Relay Virtual Circuits (VCs) have three capacity parameters:

— CIR (Committed Information Rate). This is the rate the network agrees to transfer data under normal conditions.
— Bc (Committed Burst Size). This is the maximum number of bits, during the time interval T, the network agrees to accept under normal conditions. This ensures the user can exceed their CIR for short periods of time as long as the average transfer rate does not exceed CIR.
— Be (Excess Burst Size). This is the maximum number of uncommitted bits, during the time interval T, that the network agrees to accept above the committed burst size Bc under normal conditions.

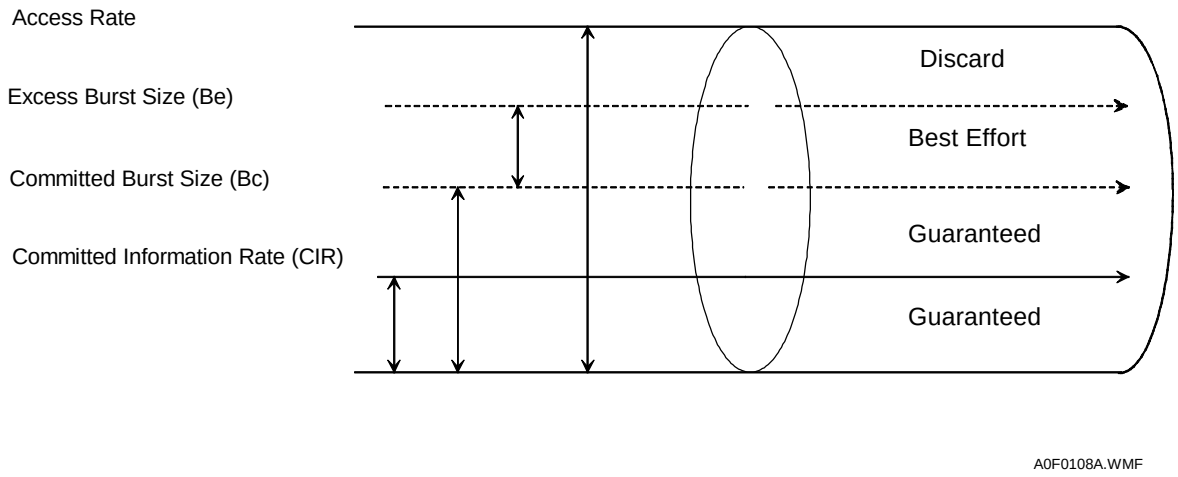


Fig. 65: The Frame Relay Data Rate Definitions and Rate Enforcement

There is a distinct relationship between these parameters where Be < (T * lport capacity) - Bc, where T = Bc/CIR. The CIR can take on a value greater than or equal to 8 in increments of 8 up to the logical port capacity. Bc, like the CIR, must be greater than or equal to 8 and have a value at any multiple of 8 up to the size of the logical port. Values of Bc and CIR that are not multiples of 8 will get rounded down to the closest multiple of 8. The minimum value for Be is 0 and can take on any value up to the size of the user port less the value of Bc. Be is entered as a multiple of 8 with all values not being an multiple of 8 being rounded down to the nearest multiple of 8.

The colors green, amber and red are used to describe and categorize packet frames for rate monitoring and enforcement.

Green frames are never discarded by the network, except under extreme circumstances. Green frames identify packets where the number of bits received during the current time interval (Tc), including the current frame, is less than Bc.

Amber frames are forwarded with the Discard Eligible (DE) bit set and are eligible for discard if they pass through a congested node. Amber frames identify packets where the number of bits received during the current time interval (Tc), including the current frame, is greater than Bc, but less than Bc + Be.

Red frames are forwarded with the Discard Eligible (DE) bit set when the Graceful Discard feature is enabled. When the Graceful Discard feature is disabled, red frames are discarded. Red frames identify packets where the number of bits received during the current time interval (Tc), including the current frame, is greater than Bc + Be.

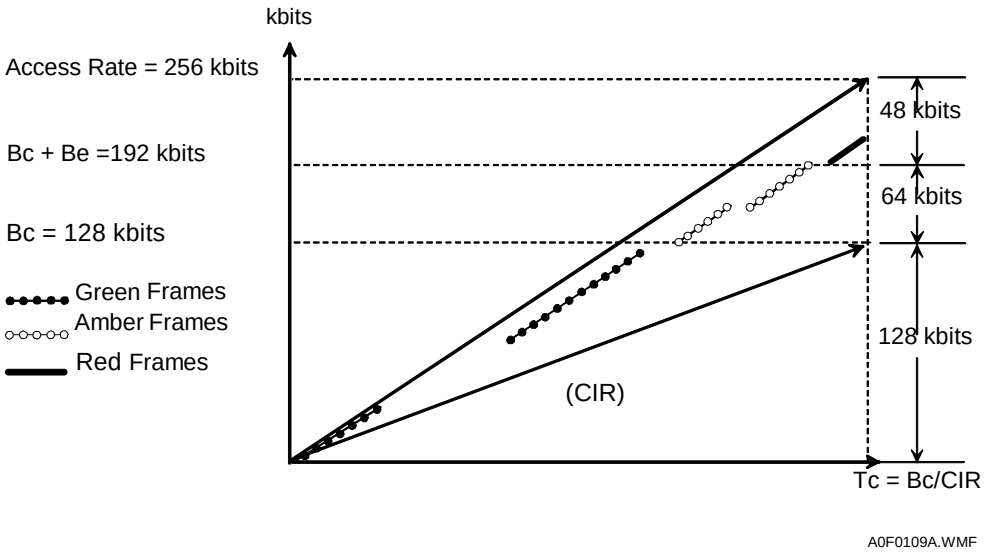


Fig. 66: The Frame Relay Data Rate Monitoring and Rate Enforcement

DXX NMS is used to configure the FRU, to set up Frame Relay Virtual Circuits (VCs) for user traffic. VC routes are defined by FRUs in the frame relay network DXX NMS also monitors FRU faults and reports on 24 h performance statistic of VCs.

FRU Unit

FRU unit consists of four physical ports (pports). Each of the pports can contain up to 32 logical ports (lports). A pport maps to a 2M xbusport, whereas lport is a dynamic resource which can be created and deleted.

Capacity of a lport is N*64 kbits/s where N has a maximum value of 32. There are four different types of lports in FRU.

UNI-DCE (Frame Relay Switch) configures the lport to appear as frame relay User Network Interface DCE. This type of lport performs the frame relay DCE functions for Link Management purposes and expects a frame relay DTE device to be attached. Frame relay DTE devices refer to those user devices which perform LMI/DTE and F or B protocol such as Routers, Bridges, Cluster Controllers, and Front End Processors, or Packetized Voice and Video.

UNI-DTE (Frame Relay Feeder) configures the lport to appear as frame relay User Network Interface-DTE. This type of lport performs the frame relay DTE functions specified for Link Management.

UNI-NNI (Frame Relay) configures the lport to appear as frame relay Network-to-Network Interface, according the Frame Relay Forum NNI Specification. NNI enables two disparate networks to connect together by using a standard protocol. The NNI lport performs both the DTE and DCE LMI function.

Frame Relay Virtual Trunk configures the lport to appear as trunk connection to another FRU. The trunk connection is used to carry traffic destined for other FRUs in the network using a trunk protocol. Frame Relay Virtual Trunks can be over-configured. This enables the operator to define more available virtual bandwidth over the trunk. This means that the sum of CIRs of those VCs going through the trunk can exceed the physical data rate of the lport.

Each of the lports may be configured independently from the others. There is no limitation on the number of each type of lport that can be configured in an FRU.

All the lport types provide flexible PDH capacity between 64 kbits/s and 2 Mbit/s for frame relay traffic. Lports adapt the frames to the xbusport. There are four 2M xbusports in the FRU. When creating an lport, DXX NMS specifies the xbusport and time slot(s) to be used for that lport. Each of the lports has to be separately locked, but the uneven 2M capacity allocation is made when the first lport within an xbusport is locked. Lports are created, deleted and configured by Ericsson DXX Node Manager.

Resources of the FRU are listed in the table below:

Resources of FRU

capacity of lport	**64 kbits/s - 2 Mbit/s**
# UNI-DCE lports	unlimited
# UNI-DTE lports	unlimited
# UNI-NN1 lports	unlimited
# Frame Relay Virtual Trunk lports	unlimited
max. # VCs per FRU	512
max. # VCs per lport	512
Address Field	2 octets
DLCI range for user VCs	16 - 991
CIR of VC	0 kbits/s - 2 Mbit/s

Frame Relay Virtual Trunks, MUAPs and Virtual Circuits

The FRU units are connected together by Frame Relay Virtual Trunks (see following figure). A single Frame Relay Virtual Trunk is realised by a point-to-point PDH circuit that consists of two Frame Relay Virtual Trunk type lports and a route between them. A Frame Relay Virtual Trunk can be either between two nodes or internal to a node (see following figure).

Frame Relay MUAP is a point-to-point PDH circuit that consists of a UNI-DCE, UNI-DTE or UNI-NNI lport and PDH SUAP/MUAP interface and a route between them.

Real access circuits called Frame Relay Virtual Circuits (VCs) use Frame Relay MUAPs and Frame Relay Virtual Trunks. The topology of VCs is limited to point-to-point graph. For every VC there is a dedicated DLCI at both endpoints (lport). DLCI numbers are unique only within one lport. They may be reused in different lports.

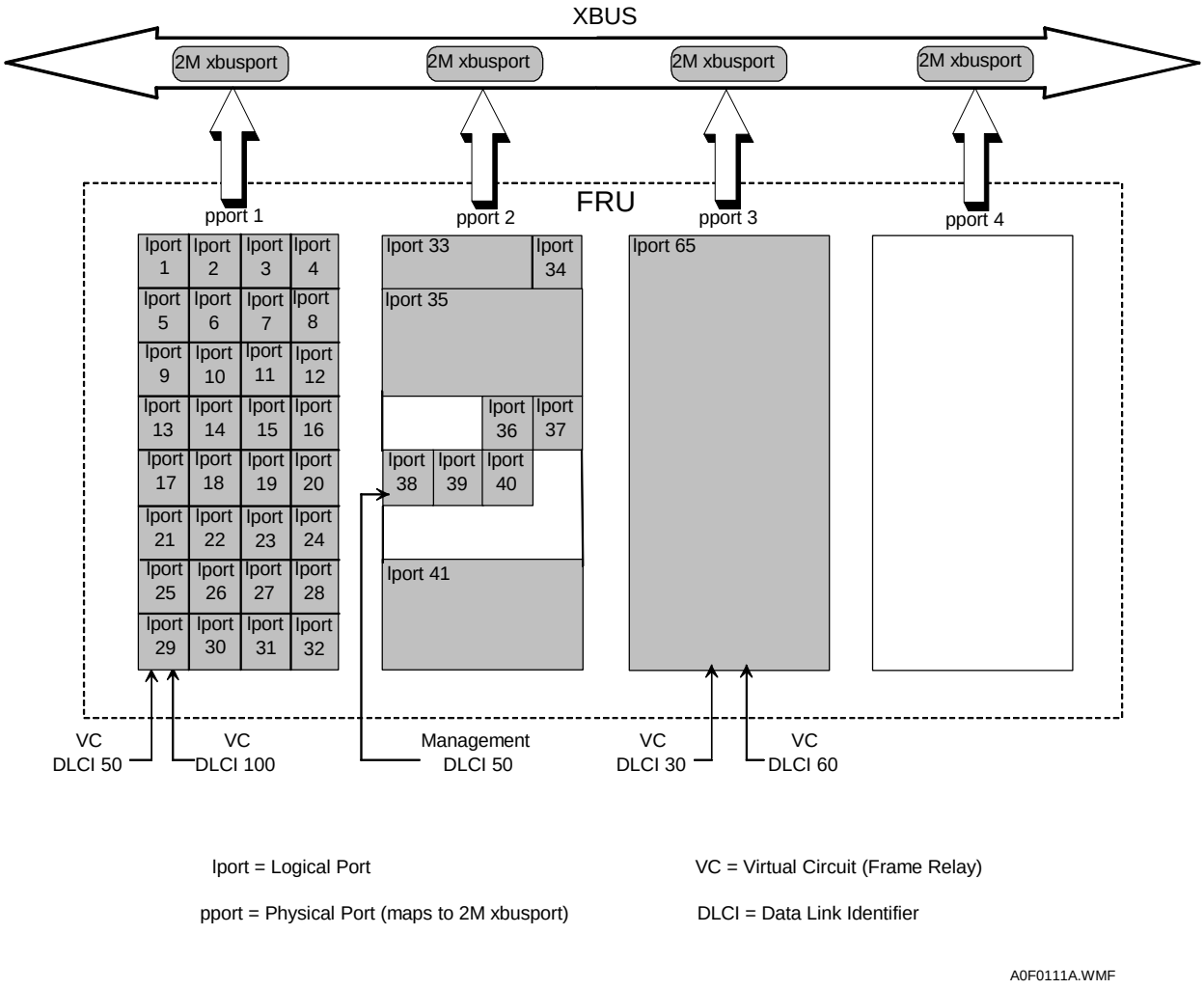


Fig. 67: Logical structure of the FRU

FRU in DXX Network
FRU contains some restrictions which should be observed:

— Frame Relay Virtual Trunk lport cannot be used as an access interface for frame relay traffic.
— The sum CIRs of those VCs which are terminated in the same lport must not exceed the capacity of the lport.
— NMS does not need to route VCs, NMS only informs the VC endpoint lports.

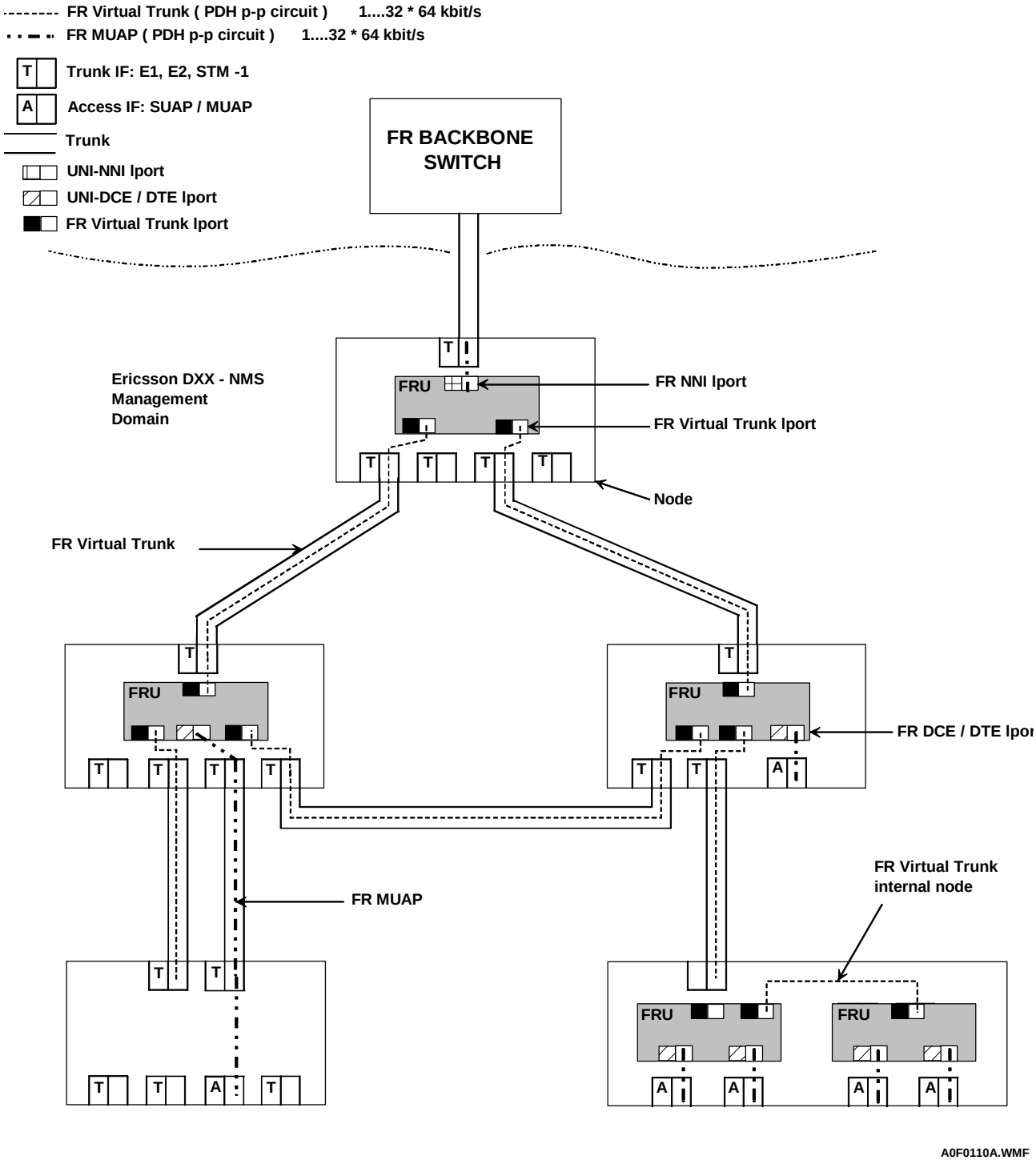


Fig. 68: FRUs in DXX Network- PDH Circuits

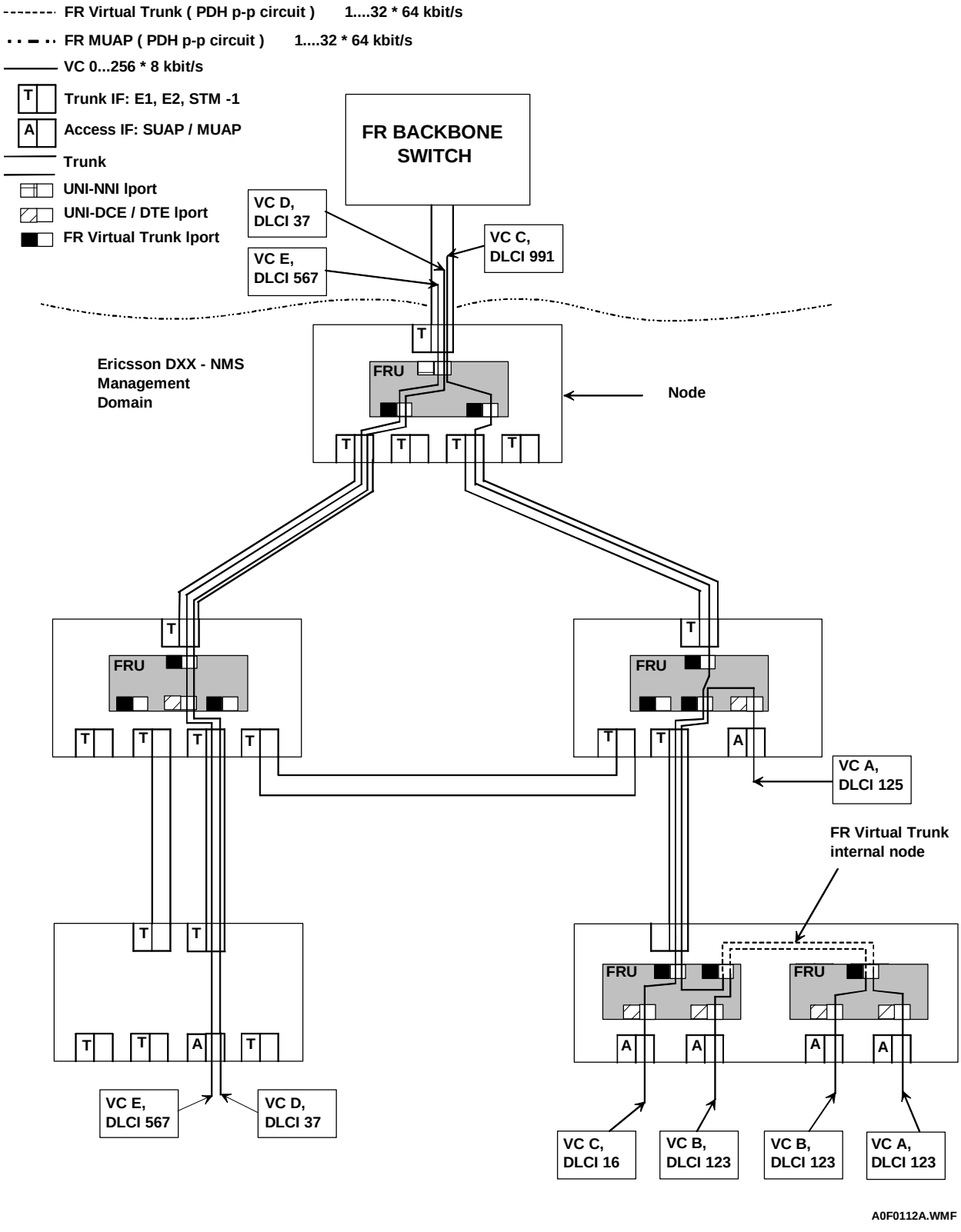


Fig. 69: FRUs in DXX Network- Frame Relay Virtual Circuits

Management Communication
DXX NMS uses embedded control channels of DXX to access FRUs. The DXX processor at FRU is responsible for DXX management communication. Each FRU in the DXX frame relay network has an IP address. The frame relay communication and services provided by FRUs are based on IP addresses.

An Embedded Frame Relay Management Channel is needed to support SNMP based management system. The management channel is based on a Management DLCI and only one external SNMP Manager per FRU is supported. The SNMP Manager is connected to a FRU using a Frame Relay Access Device (FRAD). The SNMP manager has a Frame Relay connection to that logical port in the FRU where the management DLCI resides (see next figure).

In order to enable SNMP management, an FRU can be configured to appear as a Gateway FRU (FRU that has a Management DLCI defined is a gateway FRU). A gateway FRU communicates directly with the SNMP manager. All other FRUs in the DXX frame relay network can be controlled and monitored through the Frame Relay Virtual Trunks. All FRUs in a DXX frame relay network can be accessed via the gateway FRU. There is no limitation as to how many gateway FRUs there can be in the DXX frame relay network. The SNMP Manager is enabled/disabled by the NMS Node Manager.

NOTE!

This gateway FRU concept is a pure SNMP management feature, NMS can always access any FRU in the DXX network.

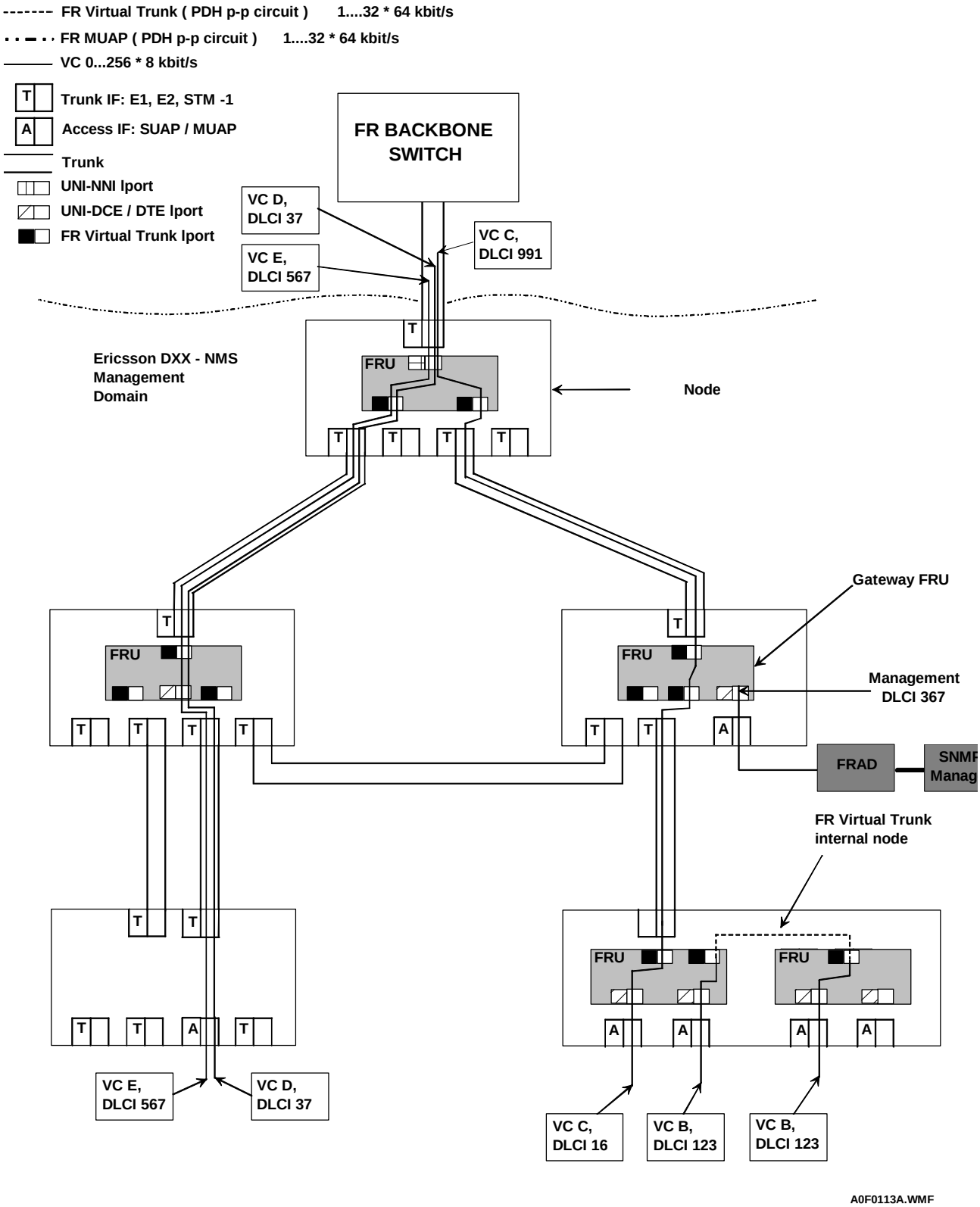


Fig. 70: FRUs in DXX Network- SNMP Manager

Lport Allocation
The maximum number of lports in FRU is 128 and the capacity of a lport is 1...32 * 64 kbits/s. Lports are dynamically created and deleted. Lport numbers 1-32 are reserved for lports in the first xbusport, 33-64 for those in the second, 65-96 for those in the third and 97-128 are reserved for lports in the fourth xbusport. The sum of the capacities of those lports which are located in the same xbusport must not exceed the 2M barrier and lport capacities must not overlap.

DLCI Allocation
Data Link Connection Identifier (DLCI) shall be unique within one lport. However, same DLCI can be used in different lports of an FRU. In practice the operator gives the DLCI values for both end points of a VC.

6.10.2 Operation

6.10.2.1 General

The main functional blocks of the Frame Relay Unit (FRU) include Universal Base Unit (UBU 259), Frame Relay Engine (FRE515), Frame Relay Processor (FRP516), Unit power supply (PDP518), and backbone bus (RMU517). The FRU occupies 2 slots in a DXX node.

6.10.2.2 Universal Base Unit (UBU259)

The UBU includes a power supply, a processor with its peripheral circuits, various interfaces for the interface module and an X-bus interface. The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus, the unit can communicate with other units in the subrack.

Communication between the DXX NMS and the FRU shall be via the UBU/FRU control interface. This control interface shall allow the DXX NMS to completely control the FRU's configuration management, fault management, performance management, accounting management, general MIB access and software download functions.

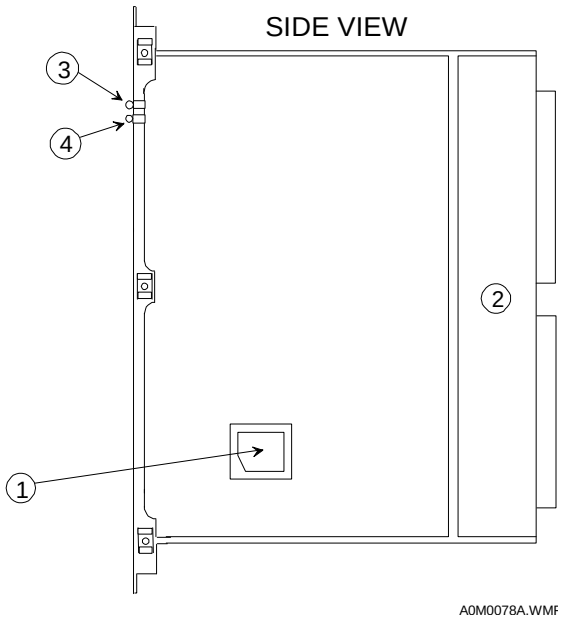


Fig. 71: Universal Base Unit (UBU 259)

1. EPROM (user replaceable)
2. Power Supply (PDF 518)
3. Red LED
4. Yellow LED

Processor and memory

The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM memory. A part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number, so that in the case of a power interruption, the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM-memory of the processor operates as a working storage.

6.10.2.3 Frame Relay Engine (FRE)

The Frame Relay Engine (FRE) is designed to function in the DXX. Major components of FRE are: RISC processor, memory, and FPGAs. Following is a brief functional description of the major component.

Processor

The FRE contains one high speed I960 RISC 25MHz CF processor to satisfy all processing requirements. The processor shares the instruction bus with SRAM, boot PROM, DRAM, and FPGAs. The peripheral bus is shared with battery backed PRAM, UART, and FLASH memory.

Memory

Five types of memory are implemented in the FRE: SRAM, DRAM, battery backed PRAM, FLASH and PROM. Static RAM (SRAM) is used for fast instruction execution and DRAM (IRAM) is used for remainder instruction execution. The PRAM is a battery backed RAM use to store configuration parameters. The battery maintains the configuration information when power is removed from the unit. The FLASH memory contains the compressed operation code and is transferred to IRAM and SRAM after power up for execution. The boot PROM contains the initial boot code for the processor and is used at power up.

FPGA

There are three FPGAs on FRE board, used for timers, processor control and the UBU interface.

6.10.2.4 Frame Relay Processor (FRP)

FRP board includes four MUNICH32 chips, a 32-bit wide frame data shared memory, an FPGA for data shared memory control, an FPGA for MUNICH32 control and an UART.

MUNICH32

There are four (4) MUNICH32 chips on the FRP board providing four (one each) full duplex serial interfaces to the UBU. These chips provide HDLC formatting and de-formatting capability. They receive serial data and store it as 32bit wide data in a shared memory. They also take 32bit data from the shared memory and transmit it out serially. It shall support the following:

— E1/DS1 32 channel PCM byte format.
— Provide for concatenation of any, not necessarily consecutive, timeslots to superchannels independently for receive or transmit operation.
— Support for HDLC protocol
— Provide a buffer for transmit and receive frames
— Support a 32 bit frame memory interface

Frame Data Shared memory

This DRAM memory is shared between four MUNICH32 chips and processor (on FRE board). An FPGA controls access to this 32 bit wide memory, so that most efficient sharing is accomplished.

FPGA

There are two FPGAs on FRP boards to provide control for shared memory and MUNICH32.

UART

The UART provides a serial interface to load and monitor off board diagnostics and to download application code into the FLASH memory via a diagnostic interface inside of the FRU. Some of the features of UART include:

— Fully independent dual functionality
— Transmit and receive blocks have 16 byte FIFOs
— Programmable baud rate generator
— Programmable serial interface characteristics
— Internal diagnostics
— Prioritised interrupt system controls

6.10.2.5 Mechanical Design

The mechanical design of the FRU unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack. However, the general recommendations for subrack equipping should be followed.

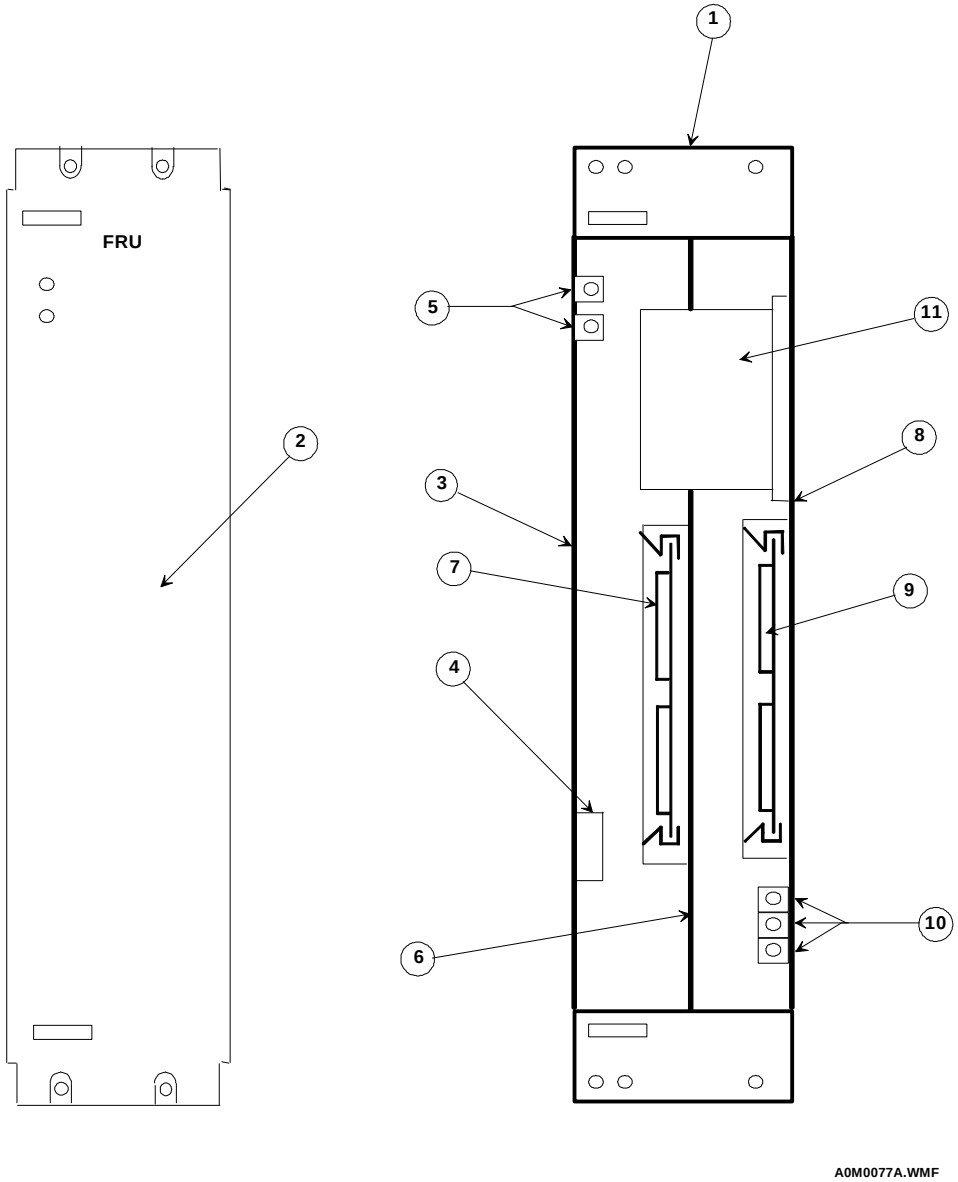


Fig. 72: FRU Mechanical Structure

1. Front view of FRU without front panel
2. Front panel of FRU
3. Universal Base Unit (UBU 259)
4. EPROM on UBU (user replaceable)
5. LED on UBU
6. Frame Relay Processor (FRP 516)
7. Memory module on FRP
8. Frame Relay Engine (FRE 515)
9. Memory module on FRE
10. LED on FRE (Behind front panel and not visible)
11. Heatsink on FRE

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

6.10.2.6 Block Diagram

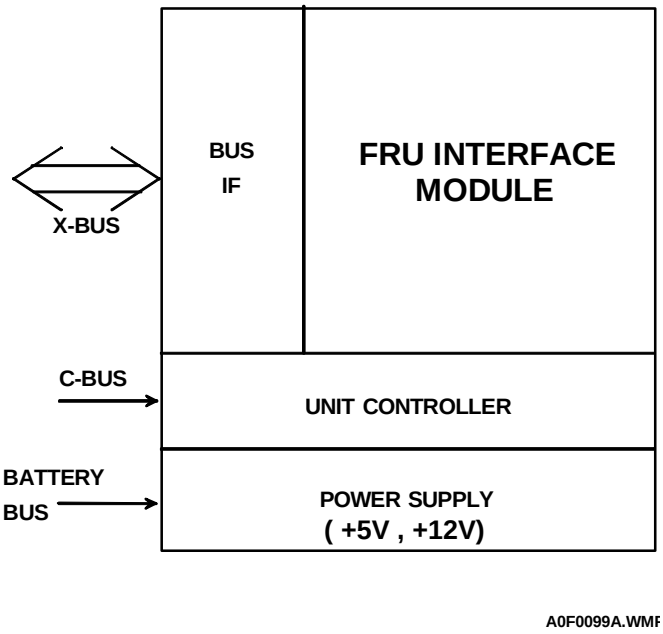


Fig. 73: Functional Structure of FRU

The FRU unit consists of the power supply, the processor and its peripheral circuits, various interfaces for the interface module and an X-bus interface.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

NOTE! ***The power supply will function only with a -48V battery input. 24V Battery operation is not supported.***

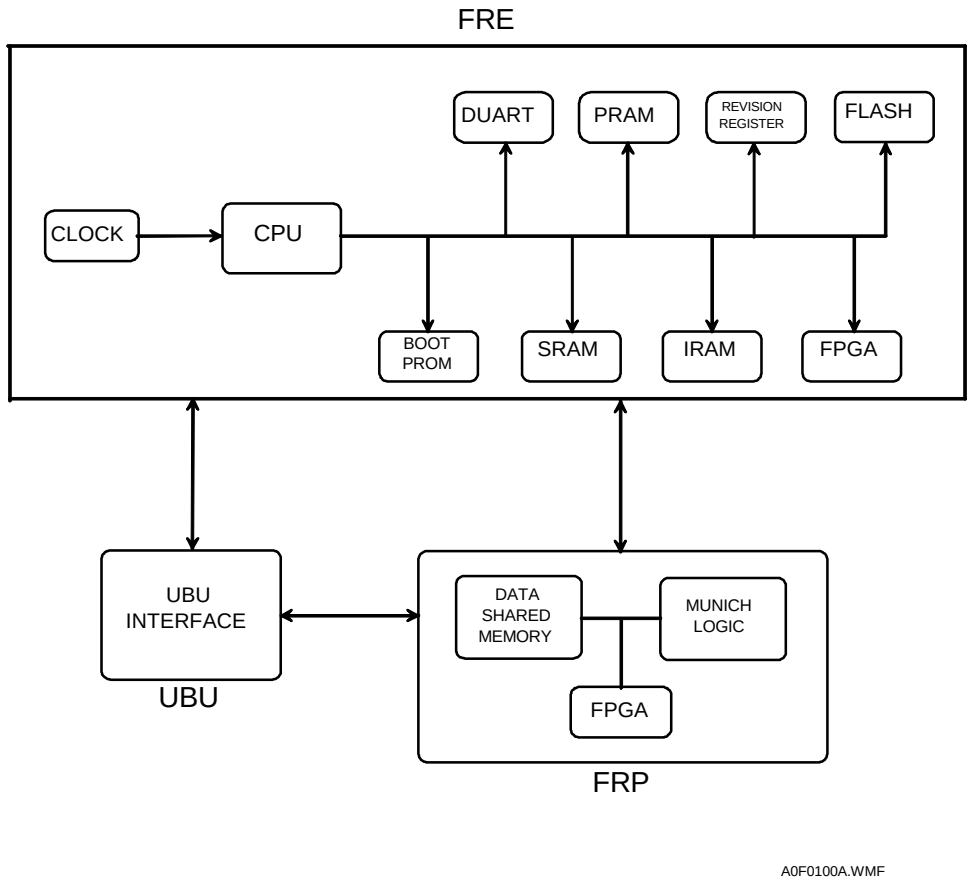


Fig. 74: Block Diagram of FRU

The FRU consists of the following base unit and modules:

1. Universal Base Unit (UBU259)
2. Backbone bus unit (RMU517)
3. Power Supply Unit (PDF518)
4. Frame Relay Processor (FRP516)
5. Frame Relay Engine (FRE515)

6.10.2.7 Power Supply

The unit receives its operating voltage from the power supply module PDF. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in the place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The PDF on the FRU only allows operation from a -48v battery supply. The module provides the operating voltages +5V, and +12V to the UBU, FRE, and FRP modules. The module also receives from the shelf backplane a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the backplane buses. The +5V operating voltage from the PDF is monitored with a reset-circuit with a low operating voltage resulting in unit reset.

6.10.3 Modules

6.10.3.1 General

There are no line interfaces on the FRE itself. All frame relay traffic will enter the DXX through an appropriate line interface module (e.g. T1, E1) and will be switched through the SXU to the FRU. The FRU will provide four physical 32x64k links to the SXU via two CIFs (contained on the UBU). Any of these links may be further subdivided into a M number of Nx64k logical ports (where N <= 32 i.e. the size of the physical ports, where M <= 32 and the sum of the bandwidths of the M logical ports <=32x64k). Each CIF (containing 2x2M) will be connected to two MUNICH chips on the FRE. These logical ports will then be used by the FRE to carry Frame Relay traffic over PVCs.

Interface Modules

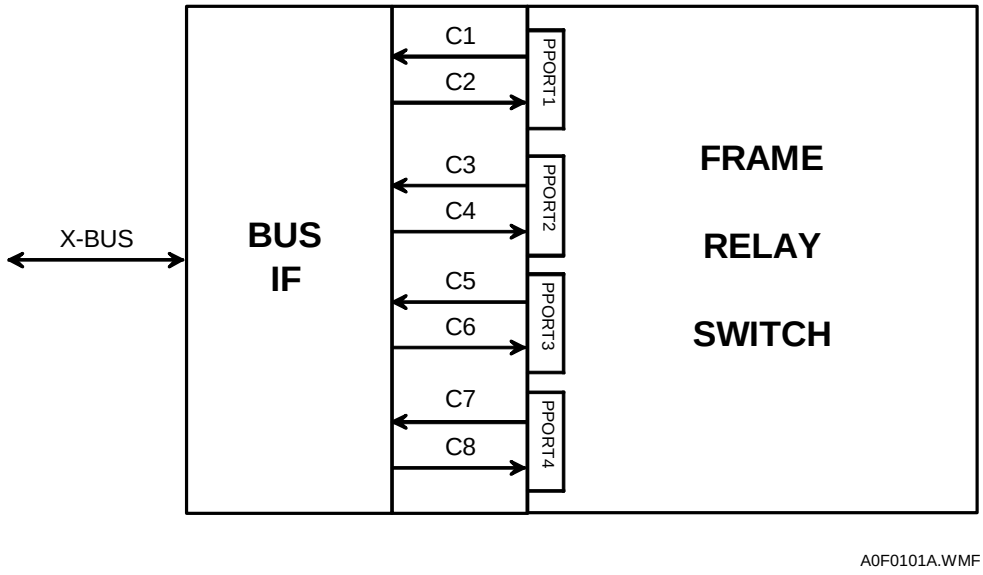


Fig. 75: FRU interface block diagram

The logical ports will be referenced using physical port IDs. These logical port IDs will be allocated by the NMS. As stated, each physical port will contain up to 32 logical ports. The only restriction on the NMS for the allocation of the IDs is that logical port IDs 1-32 are on physical port one, 33-64 on physical port two, 65-96 on physical port three and 97 to 128 on physical port four.

6.10.4 Faults

6.10.4.1 Fault Tables

The following table contains all the faults that can be monitored in FRU, as well as the reaction of the unit to each fault. In the “Indication” column, R or Y indicates that the red or yellow LED is turned on, respectively. The block number defines the source of the fault indication as follows:

Block 0	FRU unit level block that includes UBU faults and the FRE node and possible card and pport traps.
Blocks 1…128	FRE lport traps for corresponding logical ports 1..128. Blocks 1…32 belong to first physical port (CIF highway), blocks 33…64 to second physical port, blocks 65…96 to third physical port and blocks 97…128 to fourth physical port REGARDLESS of the actual number of logical ports defined per physical port.
Blocks 129…131200	FRE VC traps corresponding to possible max. 128*1024 = 131072 VCs: Block# = (129 + ((lport#-1) * 1024) + DLCI#)

BLOCK 0:

Index	Fault Condition	Severity	Indication	GPT	SPT
1	Software Unpredicted	MON+MAJ	PMA+S+R	1	1
2	UBU Reset	MON+MAJ	PMA+S+R	2	2
3	Set-up Structure Corrupted	MON+MAJ	PMA+S+R	3	3
4	Power Supply Fault: +5V in the subrack	MON+MAJ	PMA+R	4	4
5	Power Supply Fault: +5V in unit	MON+MAJ	PMA+R	4	5
6	Power Supply Fault: +12V in unit	MON+MAJ	PMA+R	4	6
7	Power Supply Fault: -10V in unit	MON+MAJ	PMA+R	4	7
8	RAM fault (UBZ534)	MON+MAJ	PMA+S+R	5	8
9	Shared Memory fault (detected by UBZ534)	MON+MAJ	PMA+R	5	9
10	EPROM fault (UBZ534)	MON+MAJ	PMA+S+R	5	10
11	Flash write error (UBZ534)	MON+MAJ	PMA+R	5	11
12	Flash copy error (UBZ534)	MON+MAJ	PMA+R	5	12
13	Flash erase error (UBZ534)	MON+MAJ	PMA+R	5	13
14	Flash duplicate error (UBZ534)	MON+MAJ	PMA+R	5	14
15	Flash shadow error (UBZ534)	MON+MAJ	PMA+R	5	15
16	Flash checksum error (UBZ534)	MON+MAJ	PMA+S+R	5	16
17	Missing settings (UBZ534)	MON+MAJ	PMA+S+R	5	17
18	Missing module	MON+MAJ	PMA+S+R	10	18
19	Conflict in module type	MON+MAJ	PMA+S+R	10	19
20	CIF ASIC loop on physical port 1	MON+WARN	MEI+S+Y	27	20
21	CIF ASIC loop on physical port 2	MON+WARN	MEI+S+Y	27	21
22	CIF ASIC loop on physical port 3	MON+WARN	MEI+S+Y	27	22
23	CIF ASIC loop on physical port 4	MON+WARN	MEI+S+Y	27	23
24	ASIC fault in base unit	MON+MAJ	PMA+S+R	32	24
25	No valid FRE application software	MON+MAJ	PMA+S+R	55	25

Index	Fault Condition	Severity	Indication	GPT	SPT
26	Start permission (i.e., cross-connection permission) denied by SXU	MON+MAJ	PMA+S+R	36	26
27	Bus sync fault	MON+MAJ	PMA+S+R	38	27
28	Missing IA activity	MON+MAJ	PMA+S+R	40	28
29	Software in flash incompatible with EPROM	MON+MAJ	PMA+R	55	29
30	Checksum error in downloaded software	MON+MAJ	PMA+S+R	55	30
31	Faults masked	MON+WARN	MEI+Y	58	31
32	HW fault in base unit (UBU)	MON+MAJ	PMA+S+R	62	32
33	HW fault in module	MON+MAJ	PMA+S+R	62	33
34	UBU to module comm. error	MON+MAJ	PMA+S+R	62	34
35	Set up data mismatch	MON+MAJ	DMA+R	69	35
36	Backup unit (SCP) fault	MON+MAJ	PMA+Y	72	36
37	UBU SW incompatible with FRE SW	MON+MAJ	PMA+S+R	89	37
38	FRE fatal error	MON+MAJ	PMA+S+R	1	38
39	FRE non-fatal error	MON+MIN	DMA+R	1	39
40	FRE reset	MON+MAJ	PMA+S+R	2	40
41	FRE flash error	MON+MAJ	PMA+R	5	41
42	FRE PRAM error	MON+MAJ	PMA+S+R	5	42
43	FRE I/O error in DRAM or SRAM	MON+MAJ	PMA+R	5	43
44	FRE Power-On Self Test failure	MON+MAJ	PMA+S+R	62	44
45	Insufficient memory for PVC faults	MON+WARN	MEI	85	51

BLOCK 1…128:

Index	Fault Condition	Severity	Indication	GPT	SPT
1	Faults masked - masks also all related VC faults	MON+WARN	MEI+Y	58	31
2	FR link protocol (LMI) status down	MON+MAJ	PMA+S+R	77	45
3	FR trunk protocol (OSPF) down	MON+MAJ	PMA+S+R	77	46
4	FR logical port one minute congestion threshold exceeded	MON+WARN	MEI	80	47
5	FR frame errors per minute exceeded the threshold on this logical port	MON+MAJ	PMA+S+R	86	48

BLOCK 129…131200:

Index	Fault Condition	Severity	Indication	GPT	SPT
	FR virtual circuit operational status down	MON+MAJ	PMA+S+R	1	49
	FR virtual circuit loop on	MON+WARN	MEI+S+Y	27	50
	Logical port forced to unlock state	MON+MAJ	PMA+S+R	69	51

6.10.5 Front Panel

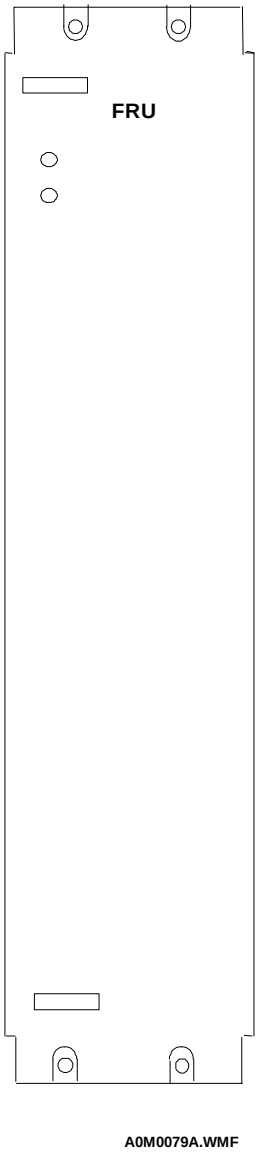


Fig. 76: FRU front panel

Above is a front view of FRU front panel. It can be removed for replacing user configurable EPROM on UBU.

6.10.6 Technical Specifications

Total bidirectional capacity (kbits/s)	8196
Number of physical ports (pport)	4
Maximum capacity per physical port (kbits/s)	2048
Frame relay links (lport) per physical port	1 to 32
Capacity of each frame relay link (kbits/s)	N*64
(Total capacity of all frame relay links in a physical port must be less than 2048 kbit/s.)	
NOTE: 5% of each frame relay link is reserved for overhead management traffic and is not available for frame relay traffic.	
Number of bytes per frame	3 to 8189

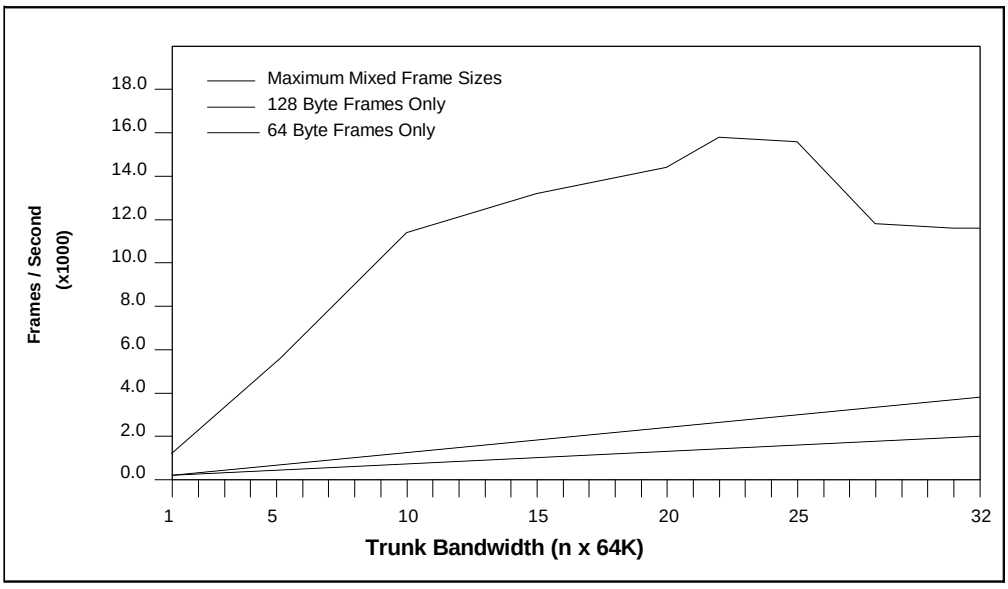


Fig. 77: Frames/Second vs. Trunk Bandwidth (Mbits) of FRU

NOTE: n=32 can be achieved only when a frame relay trunk is routed over a physical trunk larger than 2Mbits due to the 5% overhead management traffic.

Maximum Number of PVCs	512
CIR for each PVC (Kbytes/s)	8 to 2048
CIR step increment size (kbits/s)	8
Maximum number of frame relay units per DXX Node	2
Maximum number of frame relay nodes per DXX network	254
Input Voltage	-30V to -60V DC
(FRU will work only on a -48v battery supply)	
Power Consumption	12.5W

Physical Dimensions

Width	50 mm
Height	244 mm
Depth	160 mm

Environmental Specifications

Temperature and Humidities

The FRU shall be capable of continuous operation at ambient temperatures of +5 ×C to 40 ×C and relative humidities <85%, non-condensing and exceptional operating conditions of ambient temperature -5 ×C to +45 ×C and relative humidities < 90%. Refer to ETS 300 019-1-7: 1992 classification of environmental conditions.

Electromagnetic

FRU meets standard of Public Telecommunication Equipment, ETS 300386-1:1994, Table 4.

6.11 GCH-A Data Interface Unit

6.11.1 General

The GCH-A unit accesses unframed user signals at rates 2.4 kbit/s…2048 kbit/s and V.110/X.30 rate adapted signals at 8, 16, 32 and 64 kbit/s. It supports two data interfaces, which are independent of each other and may be equipped with G.703, 2 Mbit/s line terminal, fiber optical or baseband interfaces. User signals at bit rates below 64 kbit/s are rate-adapted according to the frame structure V.110/X.30 either in the NTU at subscriber's site, or in the GCH-A unit.

The signals are transported as 8, 16, 32 or 64 kbit/s signals across the DXX network. There is a special communication channel called SMUX toward NTU-A with user bit rates up to 64 kbit/s. N x 64 kbit/s signals are transported at user rate across the network. GCH-A also supports end-to-end CRC supervision of the user signals and plesiochronous data timing, whenever required. At rates below 64 kbit/s these additional features are supported in the V.110 frame. At rates n x 64 kbit/s 8 or 16 kbit/s extra transmission capacity is required across the DXX network.

When equipped with baseband interface modules, the GCH-A unit can interface access lines with entry level (E-type) baseband NTUs from Ericsson. Advanced level (A-type) NTU's are supported at user rates up to 64 kbit/s. The modules for HDB3 G.703, LTE or OTE interfaces support framed or unframed signals at 1088 or 2048 kbit/s. The bit rate to be transported across the DXX network is called XB.

6.11.1.1 User Rates

User Rates up to 64 kbit/s, BTE-64

The 2 or 4-wire baseband access line interface BTE-64 operates at user bit rate when a SBM 64E type modem is used at the subscriber end. The user rate is adapted to 8, 16, 32 or 64 kbit/s in GCH-A using the ITU-T V.110 (see Relevant Recommendations) or X.30 method.

105/109 control signal is transferred between the NTU and GCH-A using either ITU-T V.13 simulated carrier method. The control signal is transferred across the DXX network either using V.13 or, when required, at rates below 64 kbit/s using the S bits of the V.110 frame. The subscriber line quality is monitored by the BTE module. Whenever desired, the network operator can activate the CRC monitoring of the path from GCH-A to the far-end of the connection. In case the user timing signal cannot be frequency-locked to the DXX clock, plesiochronous operation should be selected in the GCH-A unit.

GCH-A Support of User Bit Rates ≤ 64 kbit/s When Utilizing SBM 64E NTUs

User Bit rate	XB Rate	Rate Adaptation Method	CRC Support
2,4 kbit/s	8 kbit/s	V.110	Yes
4,8 kbit/s	8 kbit/s	V.110	Yes
7,2 bit/s	16 kbit/s	V.110	Yes
8 kbit/s	8 kbit/s	none	No
9,6 bit/s	16 kbit/s	V.110	Yes
14,4 kbit/s	32 kbit/s	V.110	Yes
16 kbit/s	16 kbit/s	none	No
19,2 kbit/s	32 kbit/s	V.110	Yes
32 kbit/s	32 kbit/s	none	No
38,4 kbit/s	64 kbit/s	V.110	Yes
48 kbit/s	64 kbit/s	V.110	Yes
64 kbit/s	64 kbit/s	none	No
64 kbit/s	64+8 kbit/s	none	Yes

There are bit rates for using baseband NTUs from other suppliers.

GCH-A Support of User Bit Rates ≤ 64 kbit/s When Utilizing Other NTUs

User Bit Rate	XB Rate	Rate Adaptation Method	CRC Support
3 kbit/s	8 kbit/s	V.110	Yes
6 bit/s	16 kbit/s	V.110	Yes
12 kbit/s	32 kbit/s	V.110	Yes
24 kbit/s	64 kbit/s	V.110	Yes

When using the SBM 64A NTU unit, the user data is rate-adapted according to V.110 or X.30 in the NTU. The 2 or 4-wire baseband access line interface BTE-64 operates at bit rates 16, 32, 48 or 80 kbit/s. The user bit rate and transfer of control signals are selected in the NTU.

SBM 64A Support of User Bit Rates ≤ 64 kbit/s

User Rate kbit/s	Rate Adaptation Meth-od	XB Mapping kbit/s	Baseband Rate kbit/s	Control Signals	Plesio-chronous Clocking
1.2, 2.4	V.110	8	16	SA, SB, X	No
1.2, 2.4	X.30	8	16	S	No
4.8	V.110	8	16	SA, SB, X	Yes
4.8	X.30	8	16	S	No
9.6	V.110	16	32	SA, SB, X	Yes
9.6	X.30	16	32	S	No
19.2	V.110	32	48	SA, SB, X	Yes
19.2	X.30	32	48	S	No
38.4	V.110	64	80	SA, SB, X	Yes
38.4	X.30	64	80	S	No
7.2	V.110	16	32	SA, SB, X	Yes
14.4	V.110	32	48	SA, SB, X	Yes
48	V.110	64	80	SA, SB, X	Yes
56	V.110/7b	64	80	-	No
56	V.110/7c	64	80	SA, SB, X	Yes
64	-	64	80	-	No

End-to-end CRC monitoring can be supported at bit rates below 64 kbit/s. ITU-T Rec. V.110 and X.30 do not support CRC monitoring. The frame type is renamed to V.110M or X.30M when CRC is activated.

8 kbit/s or 16 kbit/s extra capacity (baseband rate - XB) is used for SMUX frame. SMUX frame supports control channel from GCH-A to SBM 64A.

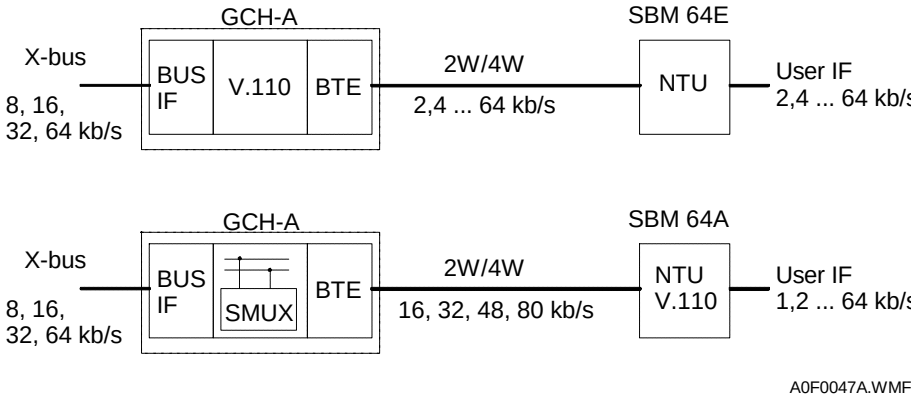


Fig. 78: GCH-A Applications at User Bit Rates ≤ 64 kbit/s

User Rates up to 384 kbit/s, BTE-384

The 2 or 4-wire baseband access line interface BTE-384 operates directly at the user bit rate. 105/109 control signal is transferred between the NTU and GCH-A using either ITU-T V.13 simulated carrier. The V.13 simulated carrier is transparently relayed by GCH-A. The subscriber line quality is monitored by the BTE module. Whenever desired, the network operator can activate an additional 8 kbit/s path through the DXX network. The path supports CRC monitoring of the path from GCH-A to the far-end of the connection. In case the user timing signal cannot be frequency-locked to the DXX clock, plesiochronous operation should be selected in GCH-A. Plesiochronous timing requires an 8 kbit/s path through the DXX network. The path can carry both timing and CRC data.

Transmission Support at Rates ≤ 384 kbit/s and Using SBM 384E NTU

User Bit Rate	XB Rate	Rate Adaptation Method	CRC Support
48 kbit/s	64 kbit/s	V.110	Yes
56 kbit/s	64 kbit/s	V.110	Yes
64 bit/s	64 kbit/s	none	[a]
80 kbit/s	64 + 2 x 8 kbit/s	none	[a]
128 kbit/s	2 x 64 kbit/s	none	[a]
160 kbit/s	2 x 64 + 4 x 8 kbit/s	none	[a]
192 kbit/s	3 x 64 kbit/s	none	[a]
256 kbit/s	4 x 64 kbit/s	none	[a]
320 kbit/s	5 x 64 kbit/s	none	[a]
384 kbit/s	6 x 64 kbit/s	none	[a]

a The transfer of the CRC check sum requires 8 kbit/s additional XB capacity.

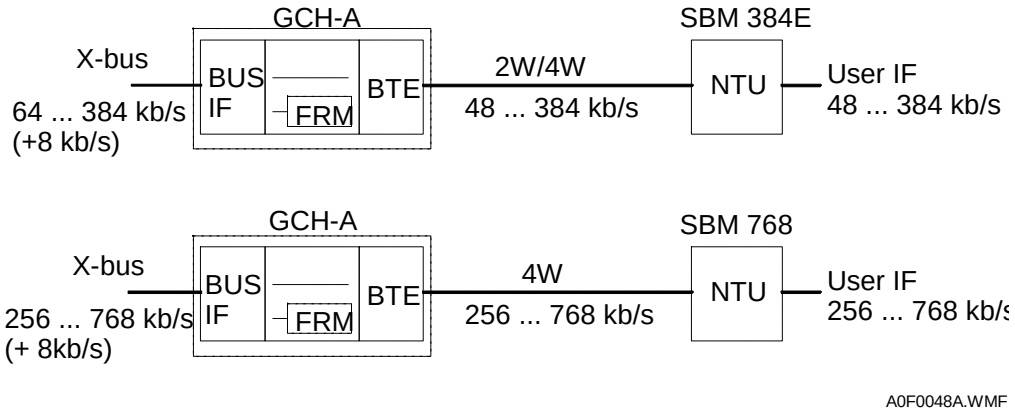


Fig. 79: GCH-A Applications at User Bit Rates ≤ 384 or ≤ 768 kbit/s

User Rates up to 768 kbit/s, BTE-768

The 4-wire baseband access line interface BTE-768 operates directly at the user bit rate. 105/109 control signal is transferred between the NTU and GCH-A using either ITU-T V.13 simulated carrier. The V.13 simulated carrier is transparently relayed by GCH-A. The subscriber line quality is monitored by the BTE module. Whenever desired, the network operator can activate an additional 8 kbit/s path through the DXX network. The path supports CRC monitoring of the path from GCH-A to the far-end of the connection. In case the user timing signal cannot be frequency-locked to the DXX clock, plesiochronous operation should be selected in GCH-A. Plesiochronous timing requires an 8 kbit/s path at rates below 512 kbit/s and 16 kbit/s at > 512 kbit/s. The path can carry both timing and CRC data.

Transmission Support at Rates ≤ 768 kbit/s and Using SBM 768A NTU

User Bit Rate			
	XB Rate	Rate Adaptation Method	CRC Support
256 kbit/s	4 x 64 kbit/s	none	[a]
320 kbit/s	5 x 64 kbit/s	none	[a]
384 kbit/s	6 x 64 kbit/s	none	[a]
448 kbit/s	7 x 64 kbit/s	none	[a]
512 kbit/s	8 x 64 kbit/s	none	[a]
576 kbit/s	9 x 64 kbit/s	none	[a]
640 kbit/s	10 x 64 kbit/s	none	[a]
704 kbit/s	11 x 64 kbit/s	none	[a]
768 kbit/s	12 x 64 kbit/s	none	[a]

a The transfer of the CRC check sum requires 8 kbit/s extra XB transmission capacity.

User Rate 2048 kbit/s

At user bit rate 2048 kbit/s the GCH-A may be equipped with any of the following interface modules: G703, LTE, OTE-LED or OTE-LP. The physical interfaces are HDB3-coded G.703 or copper line terminal (LTE), CMI-coded fibre optical terminal (OTE). The interfaces are intended for applications where a transparent 2048 kbit/s channel is required end-to-end. The DXX network does not set any requirements on signal content or formatting other than the interface signal code.

If required, end-to-end CRC monitoring of the path in DXX may be used. Normally, the user bit rate is synchronized to the DXX clock. If the synchronization cannot be established, the GCH-A is configured for plesiochronous clocking. CRC transfer requires 8 kbit/s additional XB capacity, plesiochronous clocking with or without CRC transfer requires 16 kbit/s. The additional capacity can be supported only in cases where 8 Mbit/s trunks or n x2 Mbit/s split trunks are used.

User Rate 1088 kbit/s

At user bit rate 1088 kbit/s GCH-A may be equipped with the LTE interface module. The physical interface is copper line terminal (LTE). The interfaces are intended for applications where a transparent 1088 kbit/s channel is required end-to-end. The DXX network does not set any requirements on signal content or formatting other than the interface signal code.

If required, end-to-end CRC monitoring of the path in DXX may be used. Normally, the user bit rate is synchronized to the DXX clock. If the synchronization cannot be established, the GCH-A is configured for plesiochronous clocking. CRC transfer requires 8 kbit/s additional XB capacity, plesiochronous clocking with or without CRC transfer requires 16 kbit/s.

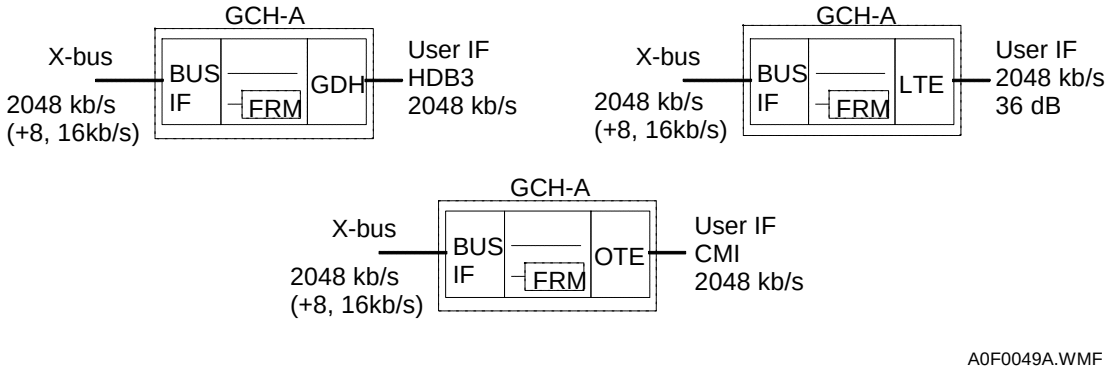


Fig. 80: GCH-A Support of Signals at 2048 kbit/s

6.11.2 Operation of GCH-A Data Interface Unit

6.11.2.1 Mechanical Design

The mechanical design of the GCH-A unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; however, the general recommendations for subrack equipping should be followed.

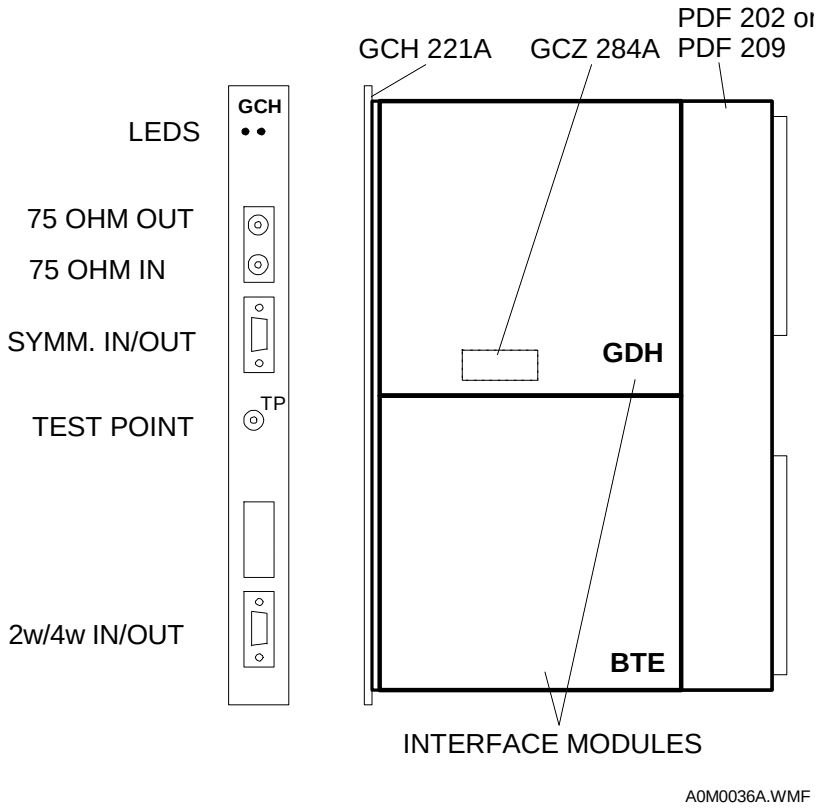


Fig. 81: GCH-A Unit Equipped with GDH 230 and BTE 232 Modules

The body of the GCH-A unit consists of an E2-sized GCH-A base unit, a PDF 202 or PDF 209 power supply and a GCZ 284A program memory. Each channel needs an interface module providing the physical subscriber line interface suiting the particular application. The two channels can use interface modules of a different type.

Functional Structure

The basic functional blocks of the GCH-A unit are:

— data formatting circuitry
— X-bus interface
— controller
— interface modules
— power supply

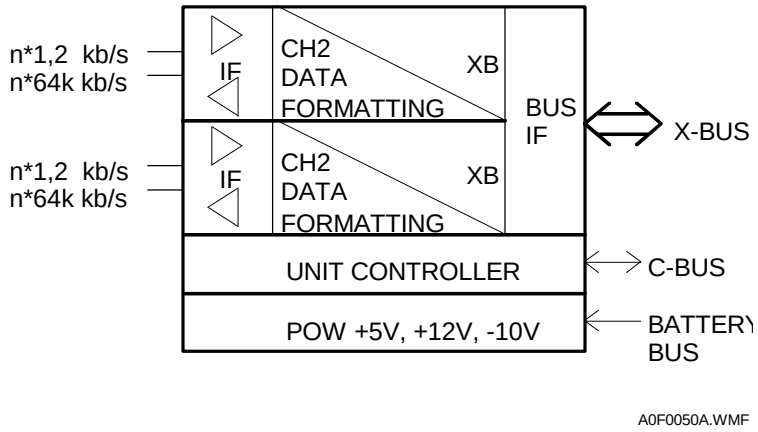


Fig. 82: Functional Structure of the GCH-A Unit

Block Diagram

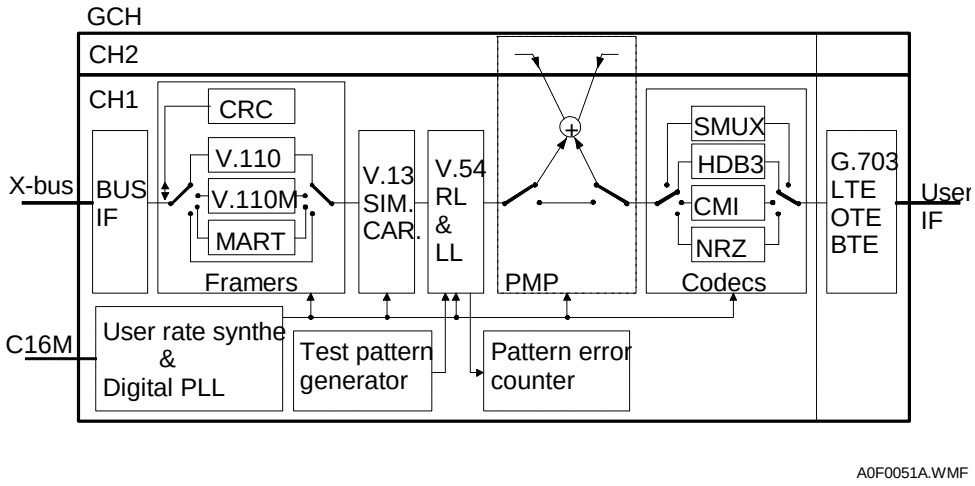


Fig. 83: Functional Block Diagram of the GCH-A Unit

6.11.2.2 Data Formatting Circuitry

The data formatting circuitry determines a majority of the characteristics of the data interfaces provided by GCH-A and provides the main data processing functions which will be described below in detail:

- rate adaptation and framing
- V.13 simulated carrier
- bit rate generation
- user interface signal coding (e.g. HDB3, CMI, NRZ)
- point-to-multipoint bridge function
- V.54 test loops
- test pattern generation and error counting

6.11.2.3 Rate Adaptation and Framing

Bit Rates ≤ 64 kbit/s and NTU Type SBM 64E

The BTE-64 module of the GCH-A accesses an NTU of type SBM 64E at the user data rate. The user rate is adapted to 8, 16, 32 or 64 kbit/s suitable for the cross-connection unit and routing tools of DXX. The GCH-A uses ITU-T V.110 rate adaptation for the lower bit rates. The V.110 frame is transparently transported through the DXX network and it can support end-to-end monitoring of the channel quality.

The V.110 and V.110S configurations use bit-oriented data buffering with +/- 2 bits jitter/wander margin. User rates n x 1.2 kbit/s (up to 38.4 kbit/s), n x 3.6 kbit/s (rates 7.2 and 14.4 kbit/s) and 48 kbit/s are supported in V.110 and V.110S. At the rate of 56 kbit/s both ITU-T V.110b and V.110c (b, c refer to table 7b/V.110 and table 7c/V.110) framing is supported.

The V.110 frame offers three channels for transfer of control signals. They are called SA, SB, and X. The signal SB or SB+SA can carry 105/109, and the signal X carries the far-end alarm. For 105/109 control the NTU uses V.13 simulated carrier which is automatically transferred to the far-end. If required, the BTE module can convert the V.13 signal to an internal 105/109 signal, which is carried by the SB or SA+SB channel of the V.110 frame. In the Management window the use of SB only is called V.110, and the use of SA+SB is called V.110S.

Bit Rates ≤ 64 kbit/s and NTU Type SBM 64A

NTUs of type SBM 64A perform the V.110 rate adaptation in the NTU. They are interfaced at rates 8, 16, 32 or 64 kbit/s. The GCH-A unit passes the regenerated interface signal from the BTE module transparently to the X-bus interface. The support of user bit rates, control signals, timing mode and supervision are determined by the NTU.

Bit Rates n x 8 kbit/s

At bit rates 8, 16, 32 kbit/s user data is transferred on 1, 2 or 4 bits of a time slot. At bit rate 160 kbit/s two full time slots are used and additionally 2 or 4 bits of a third time slot. No data framing is needed for the data transfer. These data rates usually originate from the NTU equipment.

Bit Rates n x 64 kbit/s

At n x 64 kbit/s bit rates 64…2048 kbit/s the unframed user data is transferred on 132 time slots. The data buffer length may vary from 3 to 64 bytes. The nominal buffer length selection allows for + 18 s or a minimum one byte of wander.

Bit Rates n x 64 + 8 kbit/s

The n x 64 + 8 kbit/s rate is basically intended for the T1 rate 1544 kbit/s. So far, no G.703 module is available for 1544 kbit/s.

6.11.2.4 Framing and Mapping

The frame structures used are described in the Appendices. In the GCH-A unit the signals and control signals are rate-adapted and mapped as follows:

User Rate kbit/s	Rate Adaptation Method	XB Mapping kbit/s	Control Signals	Plesiochronous Clocking
2.4	V.110	1 x 8	SA, SB, X	No
4.8	V.110	1 x 8	SA, SB, X	Yes
9.6	V.110	2 x 8	SA, SB, X	Yes
19.2	V.110	4 x 8	SA, SB, X	Yes
38.4	V.110	8 x 8	SA, SB, X	Yes
7.2	V.110	2 x 8	SA, SB, X	Yes
14.4	V.110	4 x 8	SA, SB, X	Yes

NOTE!

The transfer of the CRC check sum requires a slight modification of the V.110 frame called V.110M, because the CRC transfer is not included in the original ITU-T Recommendation.

User Rate kbit/s	Rate Adaptation Method	XB Mapping kbit/s	Control Signals	CRC Support	Plesiochronous Clocking
48	V.110	1 x 64	SA, SB, X	No	No
48	V.110M	1 x 64	SA, SB, X	Yes	Yes
56	V.110/7b	1 x 64	-	No	No
56	V.110/7c	1 x 64	SA, SB, X	No	No
56	V.110M	1 x 64	SA, SB, X	Yes	Yes
64	-	1 x 64	-	No	No
64		1 x 64 + 8 + 8	SB	Yes	Yes
80	-	1 x 64 + 2 x 8	-	No	No
80		1 x 64 + 2 x 8 + 8 + 8	SB	Yes	Yes
160	-	2 x 64 + 4 x 8	-	No	No
160		2 x 64 + 4 x 8 + 8 + 8	SB	Yes	Yes
N x 64	-	N x 64	-	No	No
N x 64		N x 64 + 8 + 8	SB	Yes	Yes N < 9
N x 64		N x 64 + 8 + 8	SB	Yes	No N > 8
N x 64		N x 64 + 24	SB	Yes	Yes N > 8

NOTE!

V.110/7b refers to ITU-T Rec. V.110 Frame Table 7b, and V.110M/7c is a slightly modified V.110 frame. is a proprietary V.110-like frame (56 kbit/s). 8, 16 denote extra capacity carrying CRC and plesiochronous timing control. SA, SB and X refer to the SA, SB, X bits in the frame.

At all data rates the channels can support simulated carrier according to V.13 for transfer of the 105/109 signal. V.13 is predominantly used at rates n x 64 kbit/s.

6.11.2.5 CRC Monitoring

The GCH-A unit can support end-to-end CRC monitoring of the user data. CRC-4 procedure used is similar to the one in G.704 frames. At rates n x 1.2 and n x 3.6 kbit/s the CRC check sum is transferred on the last five bits of the frame alignment signal of the V.110 frame. A modified V.110 frame is used at rates 48 and 56 kbit/s. When transferring the CRC check sum, the frames are called V.110M.

At n x 8 kbit/s, n x 64 kbit/s and n x 64+8 kbit/s the CRC check sum is transferred end-to-end in a proprietary frame, called , and using 8 kbit/s extra XB capacity.

End-to-end performance monitoring is based on end-to-end CRC monitoring, when activated. Channel associated end-to-end CRC monitoring is the only way to get accurate performance characteristics for a channel. The performance data is expressed in terms of G.821 parameters.

The data from the latest 24-hour period is stored for transfer to the DXX performance data base after midnight (00.00) every day. The performance data of the last 15-minute period is recorded separately. If the 15-minute performance degradation exceeds a preset limit, a transfer to the performance database is requested by the unit.

6.11.2.6 Control Signals

The GCH-A unit supports control signals for the user channel:

105/109 transfer is supported at all bit rates when using BTE modules. GDH, LTE and OTE modules do not support control signals.

The NTU transfers the control signal using method V.13. The V.13 signal can either pass the GCH-A unit unprocessed or it can be converted into a 105 signal in the BTE module. When applicable, the 105 control signal is transferred on SA, SB bits of frame V.110 or V.110M. At n x 8 and n x 64 kbit/s rates V.13 simulated carrier is always unprocessed.

6.11.2.7 V.13 Simulated Carrier

When processed, the V.13 simulated carrier is an in-band transfer method which does not require extra capacity. When 105 is turned OFF, the user data is substituted by a pseudo random pattern. After reception of 48 bits of that pattern, 109 is turned OFF and the user data (104) is blocked to OFF state. When 105 turns ON, the pattern generator input is changed from 1 to 0 for 8 bits.

If, due to transmission errors, the receiving end misses the turn on sequence, it will automatically return to ON state when more than 31 errors have been detected in the pseudo random pattern during a certain time period.

6.11.2.8 105 Supervision

In some applications 105 should continuously stay in ON condition. If desired, the GCH-A unit can monitor the 105 state and generate an alarm if 105 goes OFF. In point-to-multipoint applications the length of the talk period may be limited. When talk period supervision is activated, the GCH-A will block OFF the interface upon detection of an 105 ON period longer than the selected value.

6.11.2.9 Point-to-Multipoint Bridge

The GCH-A unit is provided with a point-to-multipoint data bridge which functionally is placed close to the user interface, between the simulated carrier blocks and the interface signal codecs. The bridge has four ports, two local user interfaces (local port) and two interfaces towards the X-bus (remote port). In point-to-point mode the pmp bridge is by-passed. One of the interface ports (typically, the port of channel 1) of the PMP bridge is used as master port, which means that it is connected to the master computer or to a previous PMP bridge. The other ports are slave ports, connected to local or remote slave data interfaces, or PMP bridges. Unused ports are not activated for pmp operation.

Data and control signals from the master port are broadcast to all slaves. Only one slave at a time can transmit data towards the master. A slave starts the transmission by turning signal 105 ON. 105 opens the path from the slave to the master. A BTE module must convert the V.13 simulated carrier into a 105 signal in order to control its pmp bridge port.

The 105 signal is transferred from a slave port to the master port as a V.13 simulated carrier, a control channel in V.110, or as an additional 8 kbit/s control channel.

If, in an error condition, more than one slave port turns 105 ON, a configurable priority control circuitry blocks the slave port with a lower priority. The talk period length of slaves can be limited to a configurable value. A slave port will be blocked off if its talk period exceeds the selected period length.

6.11.2.10 Test Loop Functions

The GCH-A unit is provided with V.54 test loop functions supporting local loop (loop 3, LL) and remote loop (loop 2, RL, RLB). The base unit supports V.54 loops towards the network and, if used, the BTE module towards the NTU. The loops can be controlled by the network manager only. The duration of the loop can be limited to a configurable value.

In general, the loops should be enabled as close as possible to the user interfaces and disabled in all intermediate equipment. Therefore, the loops should be blocked in the GCH-A unit and enabled in the NTU.

The loops are visible in the Loop window of the DXX management or service computer. The operator can also, close to the X-bus interface, make a line loop towards the user interface or, close to the physical user interface, a network loop towards the network.

6.11.2.11 Test Functions

GCH-A has per channel built-in test pattern generators and pattern error detectors. The test pattern is CCITT 511. Typically, a remote loop is activated before the pattern test is started. A unit test window facilitates activation of the test and presentation of the test results.

In general, the test resources are used via the test functions of the performance management software for DXX. These test functions utilize either the test resources of the interface unit or the common test resource of the SCU.

6.11.2.12 X-Bus Interface

The X-bus interface performs the adaptation between the data formatting circuitry and the data bus and address bus of the back plane of the DXX subrack. The X-bus interface utilizes the lower rear connector. The main signals of the X-bus interface are:

Signals of X-Bus Interface

Signal	Signal Description
C16M	Internal timing signal for the node
FSYN, MSYN	Frame and multiframe alignment signals

Signals of X-Bus Interface

Signal	Signal Description
DR10 - 17	8-bit wide data bus GCH-A towards SXU
DR20 - 27	8-bit wide duplicate of the data bus GCH-A towards SXU
T0 - 7	8-bit wide data bus SXU towards GCH-A
BAD0 - 7	8-bit wide addressing bus SXU to GCH-A

The X-bus interface transmits and receives one byte of data each time an interface of the unit is addressed by the BAD0 - 7 bus. For each 125 µs bus frame, the interface can be addressed once or several times depending on the XB capacity (n x 64 kbit/s). A channel below the bit rate 64 kbit/s is transferred between GCH-A and the cross-connection unit SXU using one byte per frame (64 kbit/s) and utilizing only one or several of the 8 data bits, 8 kbit/s each, of the byte. SXU maps only the used bits to the trunk.

6.11.2.13 Unit Controller

The microprocessor of the unit controls both the base unit and the interface modules. The data bus is extended to the interface modules. The unit is controlled by an 80C188 microprocessor. The basic unit software is stored in an interchangeable EPROM memory identified as GCZ 284A. The application programs are stored in an EPROM memory or in a non-volatile FLASH memory supporting remote controlled downloading of the application SW. The non-volatile memory also stores the configuration parameters and the HW and SW identifications of the unit. The interface modules are also controlled, monitored and identified by the unit controller. In the case of a power interruption the unit automatically restores the configuration prevailing before the interruption.

The GCH-A unit communicates with other units of the subrack and with the service and management computers of the DXX network via the unit's control bus interface, including a HDLC controller. Each unit position in the subrack has an individual address which is read from the back plane connector. This address is part of the unit identification address used by the DXX communication network. The functions of the unit are presented as management objects to the Network Management System of the DXX network.

6.11.2.14 A/D Converter

The GCH-A unit includes a multichannel analog-to-digital converter (A/D) which measures the operating voltages +5 V, +12 V, - 10V and the + 5 V bus interface voltage of the back plane and analog signals, e.g. wetting current of the BTE module (BTE).

6.11.2.15 Test Point

A 75Ω coaxial test point is provided on the front panel of the unit. The test point signal is isolated with a transformer, but the connector body is connected to the unit ground. Through the test point it is possible to measure the input and output signals of both channels as well as the corresponding clock signals. The signal to be measured is selected with the service computer in the window General Unit Parameters. The selection is stored in the non-volatile memory so that the selection is retained after a possible power interruption.

The input and output signals are HDB3-coded and the signal levels and formats are in accordance with G.703. HDB3-coded channel interface signals are measured without any recoding. Other signal codes are decoded to NRZ and thereafter coded by the test point encoder to HDB3.

6.11.2.16 Power Supply

The replaceable DC/DC unit power supply module PDF 202 or PDF 209 provides the operating voltages +5V, +12V and -10V for the GCH-A unit. The power supply operates directly on the station battery voltage which is supplied through the fuse unit (PFU) and the back plane of the DXX subrack. The X-bus interface circuits are powered from the back plane of the subrack during unit start-up conditions. The operating voltages of the unit are monitored, including the +5V back plane voltage. An alarm is generated if a voltage is out of its limits.

6.11.2.17 Timing Modes

The timing mode of a data interface depends on the type of interface, type of equipment interfaced and on the operating mode.

Bit Rate Generation

A variety of bit rates are required for the GCH-A user interfaces. The data timing signals are derived from the 16896 kHz system clock by built-in programmable frequency synthesizers. There is a synthesizer for each channel and direction of transmission.

Timing Sources

The timing signal for the incoming data (Tx-direction) comes from the user equipment. The clock for the outgoing data (Rx-direction) is supplied by the GCH-A unit.

Plesiochronous Clocking

There may be applications where the user data clock cannot be synchronized to the DXX clock, which leads to plesiochronous operation (same nominal bit rate). The GCH-A unit supports transfer of plesiochronous clocking at most bit rates.

Plesiochronous transfer is supported by the standard ITU-T V.110 Frame at rates n x 1.2 and n x 3.6. The modification of V.110 (V.110M) supports plesiochronous clocking at 48 and 56 kbit/s. Plesiochronous clocking requires an extra 8 kbit/s channel (frame) at rates n x 8 kbit/s and n x 64 kbit/s. The same 8 kbit/s channel supports both CRC and plesiochronous timing at bit rates up to 512 kbit/s. Above 512 kbit/s the plesiochronous clocking requires two 8 kbit/s channels, one for the frame and the other for the plesiochronous clock.

The V.110 method of transferring the data phase and ± stuffing is used at all bit rates. The synthesizers operate in a digital PLL mode, with jitter filtering of the input clock before phase comparison with the system reference clock. At the receiving end, the synthesizer adjusts its phase according to the value received from the far end. The phase adjustments take place in small steps in order to minimize the phase jitter amplitude and frequency spectrum.

At plesiochronous clocking the V.110 data buffer operates in bit mode. At n x 64 kbit/s data rates the data buffer operates in a so-called frame synchronous mode, where the data transferred during one X-bus frame forms a block. The stuffing bits are deleted and inserted at the border between two blocks.

6.11.2.18 Performance

The GCH-A unit supports circuit performance monitoring separately for each channel. When V.110, X.30 or framing is activated with CRC transfer, then the GCH-A performance signal quality monitoring is according to G.821. Performance data is collected in three ways:

The unit collects the G.821 data for 24-hour periods starting at 00:00 hours. The 24-hour data is available during the next day for automatic transfer to the DXX performance database.

If activated, the unit also calculates performance data for 15-minute time periods. If the signal impairments during a 15-minute period exceed a set limit, the data is transferred to the performance database.

A third set of performance counters is available for the network operator. The operator can start and terminate error monitoring at any time and gain performance data for periods that can be selected from seconds to days or months. The results are shown as error counts and as G.821 parameters.

Error Counters

The GCH-A unit is able to count, using SW and HW counters:

— number of frame losses (frame from the network side, C2)
— number of multiframe losses (frame from the network side, C2)
— number of frame word errors (frame from the network side, C2)
— number of CRC block errors
— code errors in the user interface (HDB3, CMI)
— buffer slips and adjustments

G.821 Statistics

The error counts are transformed into CCITT G.821 parameters

— total time (seconds)
— unavailable time (seconds)
— errored seconds
— severely errored seconds
— degraded minutes

6.11.3 Interface Modules

6.11.3.1 General

The unframed data interface modules used in the GCH-A unit are:

— BTE-64
— BTE-384
— LTE
— OTE-LED
— OTE-LP

A unit accesses the physical interfaces via the interface modules. The interface modules convert the CMOS-level data and timing signals to line signals (baseband, G.703 or optical signals). They regenerate the incoming line signals and convert them to CMOS-level data and clock signals. The modules also comprise crystal oscillators for line signal timing. The oscillator frequencies are phase-locked to the timing signals derived by the base unit from the DXX system clock.

The IF module monitors the level of the received signal; if it is too low or completely missing, the incoming signal is substituted by AIS at the module. A missing signal indication is reported to the unit controller which generates an alarm message.

The line signal encoders and decoders for HDB3 and CMI codes reside on the base unit. The biphase line coding for baseband rates 2.4 to 384 kbit/s and the partial response coding for rates 256 to 768 kbit/s take place in the baseband modules.

Interface to the Back Plane of the Subrack

The unit is connected to the DXX subrack through two euro connectors. The back plane supplies battery voltage to the power supply module, access to the control bus of the subrack and access to the 64 Mbit/s data cross-connection bus (X-bus). The X-bus interface uses the lower rear connector.

6.11.4 Fault Conditions in GCH-A Data Interface Module

6.11.4.1 Signals and Directions of Fault Conditions

GCH-A holds two identical interface blocks, which are numbered 1 and 2. The common parts are named block 0. The signals and directions are identified as follows:

Signals and Directions of Fault Conditions

Reference Point	Signal Description
UI1	Input signal at the receive part of the user interface
UI2	Output signal at the transmit part of the user interface
C1	XB output signal towards the X-bus interface
C2	XB input signal from the X-bus interface, net signal

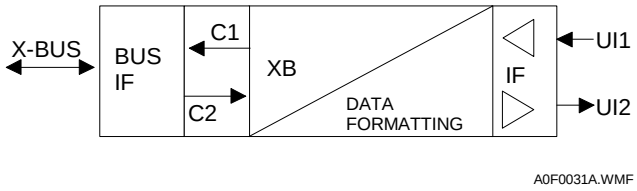


Fig. 84: Naming of Signal Reference Points

The following acronyms used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Affecting Fault
R = Red alarm LED
Y = Yellow alarm LED
AIS = Signal substituted by AIS
RAI = Remote alarm indication (bit X in V.110, X.30 or frame)

6.11.4.2 Common Parts

Faults in Common Parts (Block 0)

Fault Condition	Status	LED	UI2	C1
Power supply				
+5 V,+12 V,-10 V	PMA	R	-	-
+5 V back plane voltage	PMA	R	-	-
Memory faults				
RAM, EPROM fault	PMA, S	R	-	-
FLASH fault	PMA, S	R	-	-
Check sum error				
- in FLASH memory	PMA, S	R	-	-
- in downloaded SW	PMA, S	R	-	-
Incompatible SW revisions	PMA, S	R	-	-
RL program error	PMA, S	R	-	-
Operating status faults				
Unit reset	PMA, S	R	OFF	OFF
Unit unregistered	PMA, S	R	-	OFF
Setup parameter error	PMA, S	R	-	-
X-bus fault				
Timing fault	PMA, S	R	AIS	AIS
No interface (IA) activity	PMA, S	R	AIS	AIS
Fault masking	MEI, -	Y	-	-

6.11.4.3 Interface Blocks

General IF Faults (Block 1, 2)

Fault Condition	Status	LED	UI2	C1
Missing or wrong IF module	PMA, S	R	-	OFF/-
Wetting current low/high	MEI,-	Y	-	-
Power-OFF on input	MEI,-	Y	-	AIS
ASIC error	PMA, S	R	OFF	OFF

IF Signal Faults (Block 1, 2)

Fault Condition	Status	LED	UI2	C1	Note
Input signal faults (UI1)					
Loss of input signal	PMA, S	R	-	AIS	
Input signal code errors	PMA, S	R	-	AIS	
- HDB3 signal					
- optical CMI signal					
Signal 105 OFF	MEI, -	Y	-	AIS	Used when 105 should be continuously on
Timing errors					
Input signal (UI1) buffer slip	DMA	R	-	-	
Output signal (UI2) buffer slip	DMA	R	-	-	

Signal Faults on the Network Side (C2) (Block 1, 2)

Fault Condition	Status	LED	UI2	C1	Note
AIS from net side	MEI, S	Y	AIS	-	V.110, X.30 or frame in use
Loss of frame alignment	PMA, S	R	AIS	RAI	V.110, X.30 or frame in use
Loss of multiframe alignment	PMA, S	R	AIS	RAI	Used at bit rates < 2.4 kbit/s
Far end alarm (RAI) received	MEI, S	Y	-	-	V.110, X.30 or frame in use

Performance Conditions (Block 1, 2)

Fault Condition	Status	LED	UI2	C1	Note
G.821 unavailable state	PMA, S	-	-	-	Available when end-to-end CRC is activated.
G.821 data for last 15 minutes	DMA	-	-	-	Available when end-to-end CRC is activated.
CRC errors detected	DMA	R	-	-	Available when end-to-end CRC is activated.
Frame alignment signal error	PMA	Y	-	-	V.110, X.30 or frame in use

Test Loop Indications (Block 1, 2)

Loop Condition	Status	LED	UI2	C1
Operator activated loops				
- interface loop	MEI, S	Y	AIS	-
- line, local loop	MEI. S	Y	-	AIS
Customer activated loop	MEI, S	Y	-	-

6.11.5 Front Panel of GCH-A Data Interface Unit

The unit front panel houses two alarm LEDs (a red and a yellow), and cabling connectors for the user interface:

— one 9-pin D-type connector for each baseband and symmetrical G.703 interface
— two SMD coaxial connectors for each 75-ohm G.703 interface
— two FC type optical connectors for each OTE interface and a SMD test point connector

The input and output signals of each channel interface can be connected to the test point connector. The front panel openings are suited for all available interface modules.

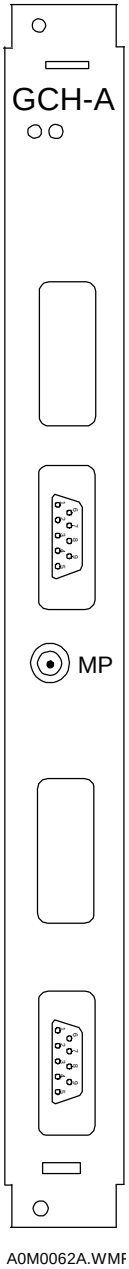
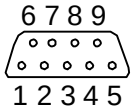


Fig. 85: Front Panel of GCH-A Data Interface Unit

D-type 9-pin female connector

	4-WIRE USE	**2-WIRE USE**
Pin	**Signal**	**Signal**
1	Transmit signal B	--------
2	Transmit signal A	--------
4	Receive signal B	Transmit/receive B
5	Receive signal A	Transmit/receive A
6	Cable shield output	--------
9	Cable shield input	Cable shield



A1C0001A.WMF

Fig. 86: D-type 9-pin female connector

6.11.6 Technical Specifications for GCH-A Data Interface Unit

6.11.6.1 BTE Line Interfaces

Line rate (kbit/s)	BTE-768	BTE-384	BTE-64
	768	384	64
	704	320	48
	640	256	38.4
	576	192	32
	512	160	24
	448	128	19.2
	384	64	16
	320	56	14.4
	256	48	12
			9.6
			8
			7.2
			6
			4.8
			3
			2.4

Input to DXX

rate accuracy	
mesochronous operation	clock looped back in the NTU or better than $\pm 10^{-9}$
plesiochronous operation	±100 ppm

Output from DXX

rate accuracy	
mesochronous operation	clock derived from the DXX node
plesiochronous operation	±100 ppm

6.11.6.2 G.703, LTE and OTE Interfaces

Line rate (kbit/s)	GDH	LTE	OTE
	2048	2048	2048
		1088	

Input to DXX

rate accuracy	
mesochronous operation	clock frequency locked to DXX or better than $\pm 10^{-9}$
plesiochronous operation	±50 ppm

Output from DXX

rate accuracy	
mesochronous operation	clock derived from the DXX node
plesiochronous operation	±50 ppm

6.11.6.3 Power Requirements and Mechanical Data

DC Supply

Input voltage: -30…-60 V DC

Mechanical Dimensions

Width: 25 mm (0.98")

Depth: 160 mm (6.30")

Height: 244 mm (9.6")

6.12 GMH G.704 Framed Interface Unit

6.12.1 General

The GMH unit processes framed signals at 8448 kbit/s, 2048 kbit/s and n x 64 kbit/s. The unit includes two independent transmission channels to carry data and also to provide an internal communication link of the DXX system. Transmission channel interfaces are independent of each other and they may, for example, be G.703 interfaces, optical interfaces and, at certain rates, also baseband interfaces. The frame structure is in accordance with G.704 for 2048 kbit/s and 8448 kbit/s. A modified G.704 frame structure is used for other speeds.

6.12.1.1 Mechanical Design

The mechanical design of the GMH unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; the general recommendations for subrack equipping should, however, be followed.

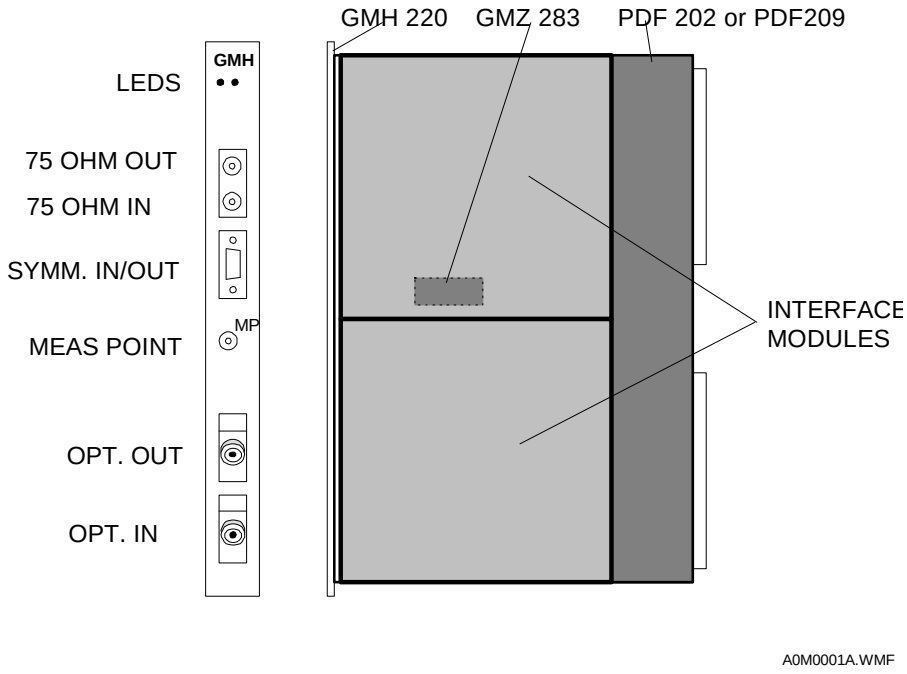


Fig. 87: GMH Unit Equipped with G703 and OTE-LED Modules

The minimum configuration of the GMH unit consists of a unit power supply PDF 202 or PDF 209, program memory GMZ 283 and a GMH unit interface module for both channels. The interface modules are selected to suit the particular application in order to provide the physical interface to the transmission line. The two channels can have interface modules of a different type.

The unit front panel houses alarm LEDs and a measurement point (75 Ω) connector. Input and output signals of both channels can be switched to this measurement point. The front panel openings are suited for all available interface modules.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

6.12.2 Operation

6.12.2.1 Functional Structure

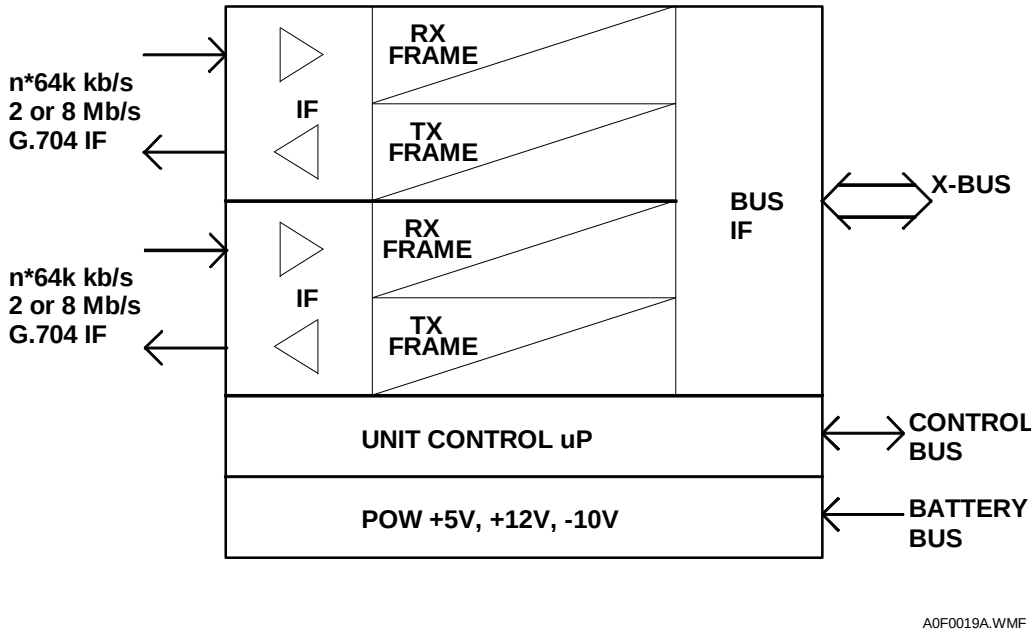


Fig. 88: Functional Structure of the GMH Unit

The main functional blocks of the GMH unit include the power supply, the processor and its peripheral circuits, line interfaces for both channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for both channels.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analog line signals to/from signals suited for the unit's digital circuits. In the transmitting direction data pulses are created in a form suitable for transmitting in the required format. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic. The line interfaces are realised as interface modules so that a unit can have two interface modules of different types at the same time. The available data transmission speeds of the unit depend on which interface modules are used, but the speed can be programmed within the limits of each module.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx-frame and Rx-frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC check sum, and by generating the HDLC channel at a required position within the frame, with the aid of the processor. In the receiving direction the Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the RX-frame block can extract the data transmission time slots, check the CRC check sum, and recover and supply the HDLC channel to the processor. The frame structure and the use of the special bits in the frame depend on the transmission speed. At 2048 kbit/s and 8448 kbit/s the frame structure is in accordance with G.704. A modified G.704 frame structure is used for other speeds. If required, it is also possible to remove the framing and have the channel to operate in a transparent mode.

The transmit buffers of the channels are used to store data received from the cross-connect through the X-bus, so that there is always a time slot available for transmit by the Tx-frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that the required time slots are always available to the cross-connect unit. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation slips are desired to occur as seldom as possible.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

6.12.2.2 Block Diagram

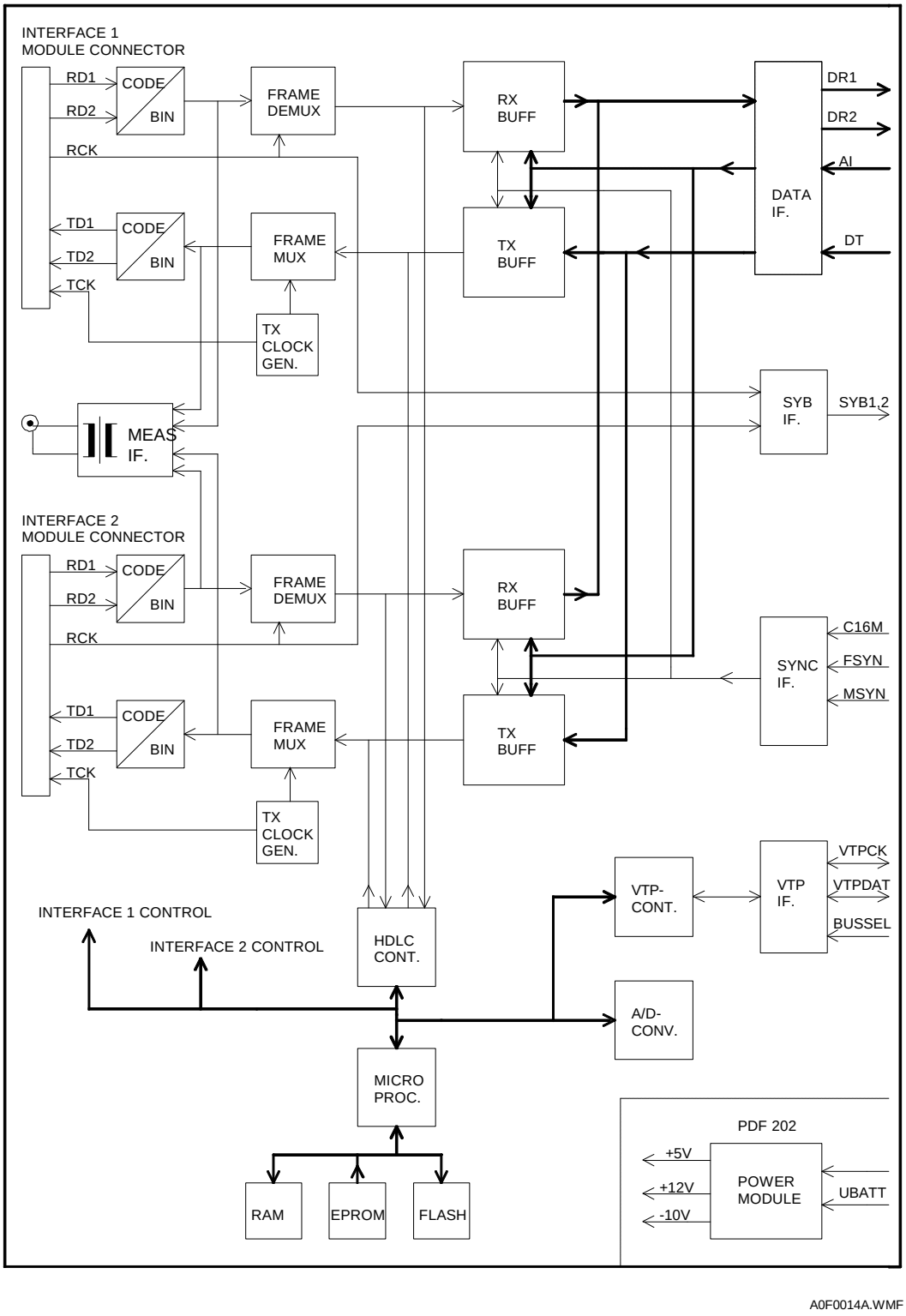


Fig. 89: Functional Block Diagram of the GMH Unit

Power Supply

A unit receives its operating voltage from the power supply module PDF 202 or PDF 209. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

Processor

The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM memory identified as GMZ 283. A part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM memory of the processor operates as a working storage containing i.e. error counters and data buffers for the HDLC-links and the frame control bus.

Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

A/D Converter

The unit includes a multichannel analog to digital converter (A/D) which monitors the operating voltages and also the control voltage from the interface module connectors. The control voltage is, for instance, a voltage received from a baseband module which controls the baseband line power-off situation.

Measuring Point

A 75 Ω coaxial cable measuring point is provided on the front plate of the unit. The measuring point is isolated with a transformer, but the connector body is connected to the unit ground. Through the measuring point it is possible to measure the input and output signals of both channels as well as the corresponding clocks. The signal to be measured is selected with the service computer in the General Unit Parameters window. This selection is stored into the unit's non-volatile memory so that the selection is retained also after a possible power interruption.

When measuring the output or input signal of the channel, the output signal of the measuring point is HDB3 coded and the signal levels and formats are in accordance with G.703. HDB3 coded channel interface signals can be measured without any coding/decoding. If the measured channel interface signal is coded in another code, then the measuring point coder is automatically used to transform the NRZ signal into an HDB3 signal.

6.12.2.3 X-Bus Interface

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with the data bus DR2. The cross-connect unit decides with the aid of the BUS test which bus to use, and this information is supplied to other units through the control bus. From the cross-connect unit the GMH unit receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are monitored also by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure for each transmission speed. In the DXX system the frame repetition frequency is always 8 kHz so that frames of different length, i.e. frames containing a different number of bits, must be used for different transmission speeds. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronization by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a two-channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronization words and the transmitted data channels, the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organization can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

The frame structures are described in Appendices.

6.12.2.4 2048 kbit/s Frame Structure

The DXX system utilizes a frame structure for 2048 kbit/s according to G.704. The first time slot of a frame, ts0, contains the Frame Synchronization Word (FSW). The bits of this frame synchronization word have a different meaning in odd and even frames. Even frames contain the frame alignment signal and odd frames specify one bit of this word as a frame alignment signal, one bit as the far-end alarm bit and five special bits. Four of these five special bits are recommended to be used by the internal HDLC channel of the DXX system. The function of these bits is defined in the user interface through the GMH Parametrization window. However, if CRC check is used, then the first bit in time slot ts0 of every frame is used by the CRC check and cannot be defined for other purposes in the user interface.

The first bit of 16 consecutive time slots ts0 form a CRC multiframe consisting of 16 frames. This multiframe has six frame synchronization bits, eight bits for the CRC check sum, and two bits used to transmit far-end block error information. The period of 16 frames is divided into two subgroups, each consisting of eight frames. A check sum is separately calculated for both subgroups and sent during the next subgroup. The receiving end performs the CRC check, and if a faulty block is detected, then information about this is sent to the far-end by setting the corresponding block error bit to state 0 during one multiframe.

Time slots ts1...ts15 and ts17...ts31 are reserved for payload data transmission. Each data time slot has a corresponding 4-bit signalling word, which is transmitted in time slot ts16 of a multiframe. The bits in time slot ts16 can be utilised by other functions if no signalling capacity is required by a data time slot.

The length of a multiframe is 16 frames. Within the multiframe the first ts16 time slot (in the first frame) is used to transmit the multiframe synchronization word (four bits in the 0 state), the multiframe far-end alarm and three special bits. The function of the special bits can be defined through the user interface. It is recommended to set these bits in state 1 when they are not used. The ts16 time slots of the other frames carry signalling data for two time slots each, four bits for each data time slot. For example, ts16/Fr1 carries signalling data for the time slots ts1 and ts17.

An HDLC channel can be placed in any free time slot where it can occupy a required number of bits. A time slot bit can carry 8 kbit/s of data, and thus the total capacity of the 8 bits in a time slot is 8 x 8 = 64 kbit/s. It is, however, recommended to locate the HDLC channel in the bits B5, B6, B7 and B8 of the time slot ts0. Due to the frame alternation the time slot TS0 capacity is only 4 kbit/s per bit, and these four bits together provide a 16 kbit/s transmission channel. If the HDLC channel is located in bit B1 of time slot ts0, replacing the CRC check, then no other bits can be used to form the HDLC channel.

N x 64 kbit/s Frame Structure

The n x 64 kbit/s frame structure is a modified 2048 kbit/s frame structure. A frame is again repeated with the frequency 8 kHz, as with other transmission speeds, but because the transmission speed is now lower, the frame must be shorter. The modified frame consists of n time slots to be transmitted. The time slot ts0 has the same structure as for 2048 kbit/s, and the frame special bits and CRC check have the same function as for 2048 kbit/s. The signalling multiframe is constructed in the same way as for 2048 kbit/s, but now the last time slot in a frame is used for signalling purposes.

Frame Multiplexing and Demultiplexing at 2048 kbit/s

A frame to be transmitted is multiplexed in the Frame Mux and clocked by the Tx clock. The data to be transmitted is received through the X-bus into a transmit buffer, from which the Frame Mux fetches data, one time slot at a time, controlled by the bus frame clock. The time slot ts0 can also be received via the transmit buffer from the bus, but usually the frame alignment signal is generated in the Mux. The other bits for the ts0 are read into the transmitted frame from positions defined through the user interface. E.g., the HDLC channel data is received from the HDLC controller in serial form and clocked by the Tx clock. The data for the first frame in the signalling multiframe is generated in the Mux and the time slot signalling data is received via the transmit buffer from the X-bus. Before the frame is transmitted, a CRC check sum is calculated and the CRC multiframe structure is placed into the first bit of time slot ts0.

The receiver will search for the frame alignment signal in the received decoded signal. When the alignment is found at the correct position in consecutive frames, the receiver is synchronized and the frame demultiplexed. The frame alignment search is performed in accordance with a state diagram which should ensure that the receiver will be correctly synchronized even on noisy connections.

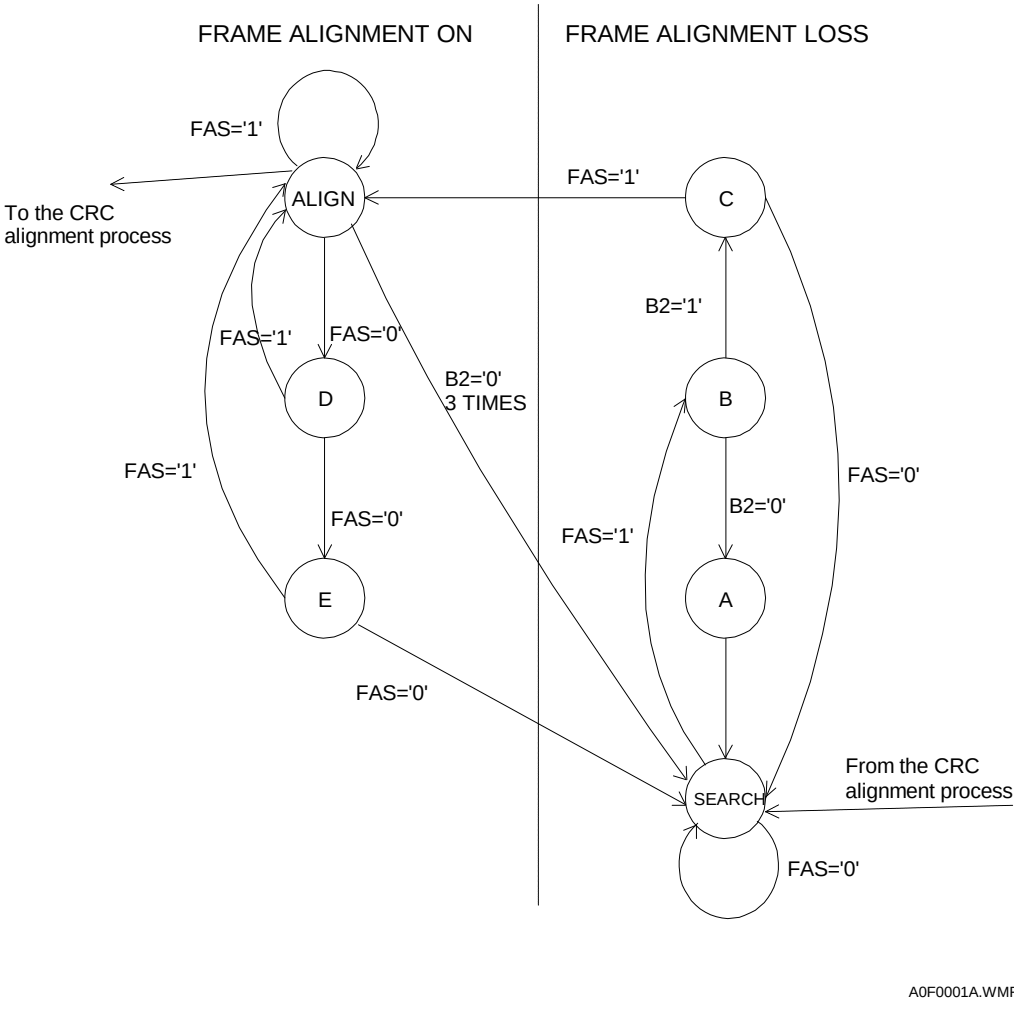


Fig. 90: Frame Alignment State Diagram at 2048 kbit/s

The right-hand side of the figure above shows the states in the search mode: the frame alignment alarm is activated and the data to the X-bus is set to AIS. On the left-hand side the receiver is synchronized to a received frame and the alarm is inactive. In the search mode the correct frame synchronization word must be found, thereafter the time slot ts0 in the next frame must have the bit B2 in state 1, then the frame synchronization word again has to be in the correct position in the next frame, and only then the frame is synchronized. If any of these conditions is not fulfilled, the search is repeated from the beginning. When the frame is synchronized, the frame alarm is inactivated and at the same time the AIS is removed from the data supplied to the X-bus.

When the frame alignment is found, the receiver monitors the received frame synchronization words. The frame alignment is considered lost if a corrupted frame synchronization word is received in three consecutive frames. In this case the frame synchronization alarm is activated and a new frame alignment search is started. The receiver monitors also the state of bit B2 in time slot ts0 of odd frames. The frame alignment is considered lost if the bit B2 is 0 in three consecutive frames.

The number of faulty frame synchronization words is also counted in the receiver in order to calculate the error rate of the connection. Normally, the error rate limit is set to 10E-3. If the error rate exceeds this value, the reception is inhibited and the receiver sets AIS as data to the X-bus and activates the error rate alarm. The error rate is not calculated when the frame alignment is lost.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are less than three bits in state 0 during two frames and a corresponding alarm is activated. The far-end alarm bit is extracted from time slot ts0 in a received frame. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates the functions defined in the alarm table.

In receiver fault situations - if the error rate is too high or if the frame alignment is lost, for instance - the receiver transfers corresponding information to the transmitter which then activates the far-end alarm bit in the transmitted time slot ts0.

The CRC check is used to increase the reliability of frame alignment and to prevent alignment on words only simulating the frame synchronization word. The receiver is synchronized to the first word found to be identical with the frame synchronization word. If this detected word is sent by some data equipment in a data slot and if this word remains the same for a longer period, the receiver can falsely synchronize to this simulating synchronization word. This situation is detected with the CRC check.

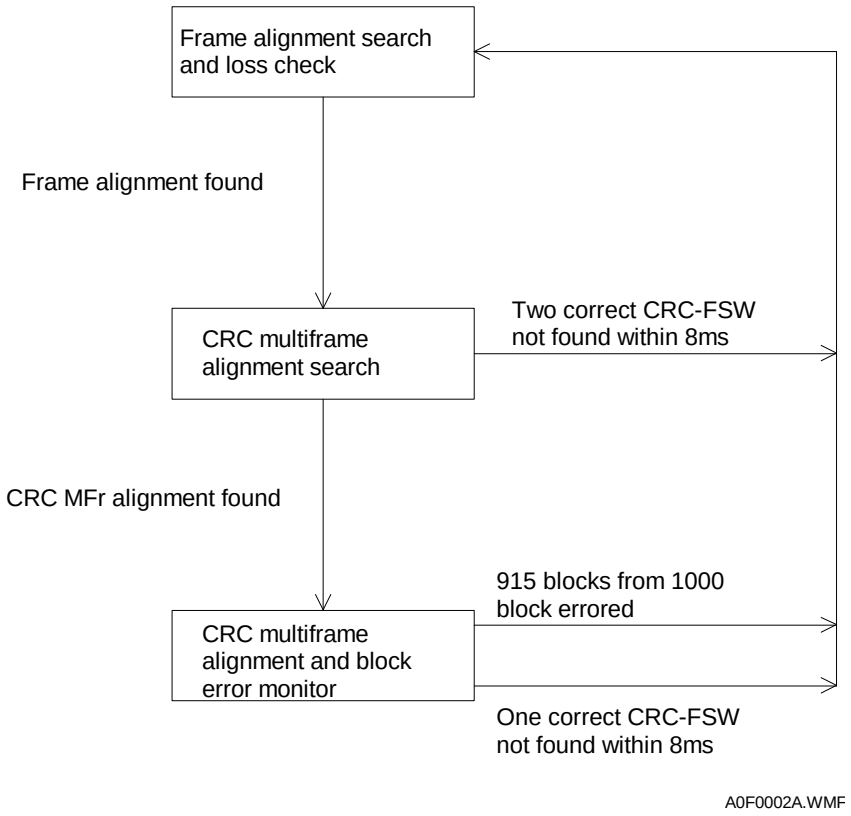


Fig. 91: CRC Multiframe Alignment State Diagram at 2048 kbit/s

The CRC multiframe alignment state diagram is shown in Fig. 91. The state at the top contains the 2048 kbit/s frame alignment state diagram. When frame alignment is found, the receiver starts the search for the CRC multiframe alignment signal. The CRC multiframe alignment is found when the receiver finds two correct CRC multiframe alignment signals in the correct position within a period of 8 ms. Then the CRC error count is started. If two CRC multiframe alignment signals are not found within the period of 8 ms, then also a new frame alignment search is started and a frame synchronization alarm is activated.

The receiver starts to count CRC block errors when the CRC multiframe alignment is found. The frame alignment search is started and an alarm is activated if there are more than 914 faulty blocks out of 1000 blocks. The CRC multiframe synchronization words are also monitored: if no correct CRC multiframe synchronization word is found within 8 ms, then a new frame alignment search is started.

The signalling multiframe consists of the time slots ts16 of 16 consecutive frames. The first four bits of time slot ts16 in the first frame form the multiframe synchronization word. These bits are all zeroes (0). The other time slots ts16 contain signalling information for the data time slots.

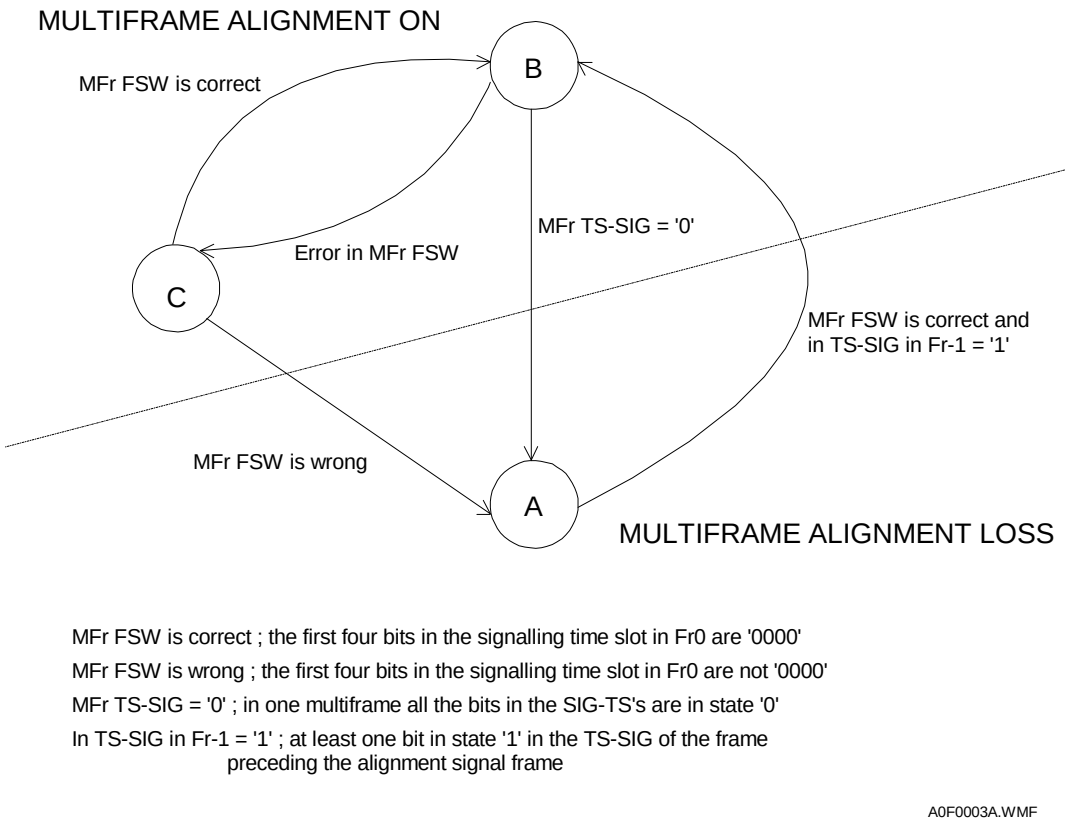


Fig. 92: Signalling Multiframe Alignment State Diagram

The signalling multiframe alignment signal search begins when the frame alignment is found. When the first four bits of time slot ts16 are found to be zeroes (0), this is considered to be the multiframe synchronization word. However, in order to avoid a false alignment it is required that the prior time slot ts16 had at least one bit in state 1. The AIS is removed from the signalling information to the X-bus and the multiframe alarm sent to the far-end is inactivated when the alignment is found.

The multiframe synchronization word monitoring function is started when the multiframe is synchronized. If errors are found in two consecutive synchronization words, the multiframe alignment is considered to be lost. In the synchronized state the contents of all time slots ts16 are monitored, and if all time slots ts16 in one multiframe contain only zeroes (0) the multiframe alignment is considered to be lost. A corresponding alarm is activated if the alignment is lost, the signalling data to the X-bus is set to AIS and the transmitted far-end alarm is activated (ts16/B6).

The far-end alarm is extracted from the received signalling multiframe synchronization time slot. The alarm state is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates an alarm. Through the user interface it is possible to define that the alarm state also puts the signalling data to the X-bus to AIS. In such case the frame far-end alarm bit will also put the signalling data directed to the X-bus to AIS.

If the signalling multiframe synchronization is lost, the received signalling time slot data is monitored in order to detect an AIS. A signal is considered to be AIS if the signalling time slot during one multiframe contains only one bit or no bits in state 0.

Frame Assembling and Disassembling at n x 64 kbit/s

A frame is assembled and disassembled at n x 64 kbit/s in a similar way to that of 2048 kbit/s. The minor differences are due to the smaller number of bits in the frame.

A different number of faulty frame synchronization words is required in the error rate count to trigger an alarm and to inactivate it.

The number of CRC block errors required to start a new search for the frame alignment depends on the transmission speed. The number decreases when the transmission speed is lowered.

The signalling frame time slot is the last time slot in a frame. Multiframe alignment is achieved in the same way as at 2048 kbit/s.

6.12.2.5 8448 kbit/s Frame Structure

The DXX system uses a frame structure in accordance with G.704 at 8448 kbit/s. The frame contains 132 time slots of eight bits each, and thus the frame length is 1056 bits. The frame is repeated at a frequency of 8 kHz. The frame synchronization word (FSW) consists of 14 bits and it is divided into two time slots: eight bits in time slot ts0 and six bits in time slot ts66. The time slot ts66 also contains a frame level far-end alarm bit and one special bit (ts66/B8). The use of this special bit can be defined via the user interface.

CRC6 checkbits are located in time slot ts99. The first six bits are reserved for the transmission of the calculation results, the bit B7 is the far-end block error bit and the use of the bit B8 can be defined through the user interface. The CRC check uses no multiframe, but the check sum is always calculated for each frame and sent in the next frame. If an error is detected in the received block, corresponding information is sent to the far-end by setting the transmitted bit B7 to 1 during one frame.

Time slots ts5...ts32, ts34...ts65, ts71...ts98 and ts100...ts131 of a frame are reserved for data transmission. Signalling capacity is reserved for each data time slot in the signalling multiframes defined by time slots ts67...ts70. The data time slots are divided into four groups, Gr1...Gr4. Each signalling group contains 30 time slots and has an individual signalling time slot, which is independently processed. The multiframe structure and the synchronization time slot are similar to those used at 2048 kbit/s.

It is possible to use the time slots ts1...ts4 and TS33 for data transmission, but there is no defined signalling capacity for these time slots.

It is recommended that the HDLC channel is located in time slot TS33 or in TS1, which gives this channel a capacity of 64 kbit/s. For special purposes the HDLC channel position can be put in any time slot through the user interface, through which it is also possible to select any of the time slot bits 1...8 to be used by the HDLC channel.

Frame Multiplexing and Demultiplexing at 8448 kbit/s

A frame for 8448 kbit/s is assembled in the same way as for 2048 kbit/s. The data is received via the X-bus and inserted, clocked with the Tx clock, into the time slots of the frame to be transmitted. Frame synchronization words are generated or extracted from the transmit buffer, special bits are set at their positions, and, eventually, the CRC check sum for the whole frame is calculated and inserted into the transmitted frame in an individual time slot.

A frame alignment signal search is performed on the received decoded line signal. When the alignment is found, the receiver is synchronized to the received frame clock in a defined sequence.

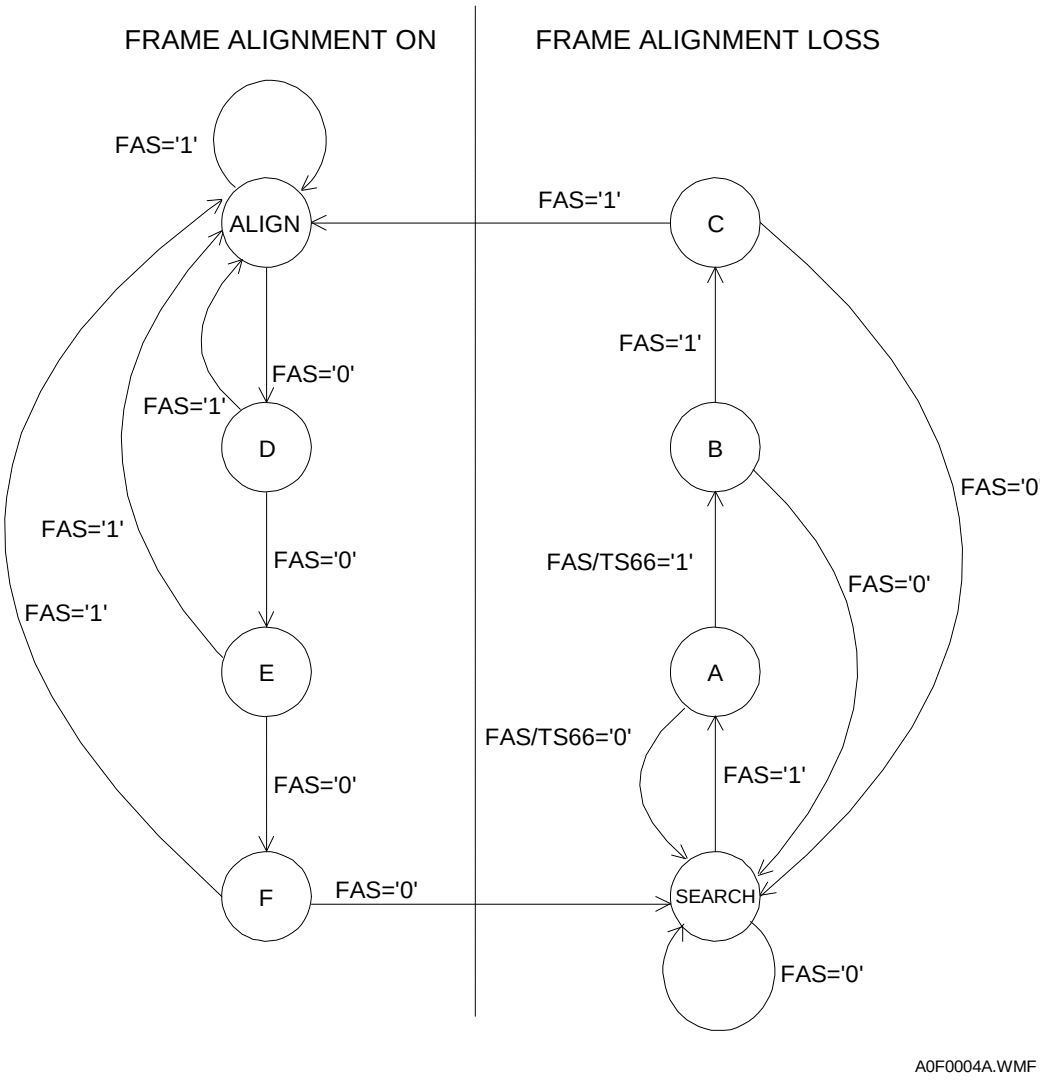


Fig. 93: Frame Alignment State Diagram at 8448 kbit/s

A frame alignment sequence is shown on the left side in the figure above, where the receiver is synchronized to the received signal. The right-hand side of the figure shows the alignment loss sequence.

The frame alignment is found when the whole frame synchronization word in three consecutive frames is received without errors at the correct position. The frame alignment is considered lost if a corrupted frame synchronization word is received in four consecutive frames. In this case the frame synchronization alarm is activated and AIS is set as data to the X-bus.

The receiver counts the number of faulty frame synchronization words when synchronization is achieved. Frame synchronization word bits in time slot ts0 and time slot ts66 are counted. The number of faulty frame synchronization words is used to calculate the error rate of the connection. If the error rate exceeds 10E-3, the receiver sets AIS as data to the X-bus and activates the error rate alarm.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are seven or fewer bits in state 0 during two frames and a corresponding alarm is activated. If the alarm is activated, at least 12 bits have to be activated in state 0 during two frames before the alarm is inactivated.

The far-end alarm bit is located in bit B7 of time slot ts66. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. In the transmitter end the far-end alarm bit is activated in accordance with the situations defined in the alarm table, i.e. when there is a serious frame level fault in the Rx direction.

The CRC6 check is used to increase the reliability of frame alignment and to monitor the error rate of the data transmission. The number of blocks with errors is counted when the synchronization is achieved. If there are more than 825 faulty blocks out of 1000 blocks, the frame is not correctly synchronized and a new search is started. The CRC6 check is well suited to monitor low error rates.

Each signalling multiframe of the time slots ts67, ts68, ts69 and ts70 is independent. The alignment sequences and the multiframe construction are the same as for a 2048 kbit/s frame.

6.12.2.6 Buffers

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus, it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control that write and reading operations do not simultaneously address the same time slot. In the GMH unit there are two ways to avoid such conflict situations:

1. The transmit buffer length is set to two frames. Then the frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one frame or 125 µs.

2. The read and writing operations are performed on the same frame area, but the transmitted frame is synchronized to the bus frame clock and data are written to the buffer in a defined sequence and at a regular speed so that a read/write conflict is effectively prevented. In this case there is only a small frame delay, but the data must be evenly distributed in time slots on the X-bus. The bus has a limited capacity for even distribution: it is reserved for 2048 kbit/s and 8448 kbit/s connections, and it is recommended to use this capacity for trunk lines.

Through the user interface the Rx Buffer can be set to the 2 Fr alternative. In this case the transmit buffer is set to the short form which provides a short delay. The other alternatives create a two-frame buffer.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the cross-connect unit requests data from the interface units through the X-bus, it also specifies the time slot concerned. Usually, the phase of the received frame does not coincide with the frame phase of the X-bus; on the other hand, the receiver writes time slot data into the Rx buffer clocked by the received frame. Therefore the Rx buffer has to control that the read and writing operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the GMH unit the centring is made by changing the read address, the change being always one frame or a multiple of a frame. The centring causes a certain number of frames to be lost or re-transmitted; the number is proportional to the distance which the read address is moved. Through the user interface it is possible to select four different lengths for the receiving buffer, in order to meet different requirements, such as a minimum delay or the ability to tolerate large speed fluctuations.

Centring is required when the equipment is powered up, when a received signal contains disturbances, or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

Operating Modes of Buffers

Rx Buffer	Rx delay	Tx length	Tx delay
2 Fr	0…2 Fr	1 Fr	approx. 0 Fr
4 Fr	1…3 Fr	2 Fr	1 Fr
8 Fr	1…7 Fr	2 Fr	1 Fr
8 Fr Split trunk	2…6 Fr	2 Fr	1 Fr
64 Fr	1…63 Fr	2 Fr	1 Fr

2 Fr Rx Buffer

The length of the receiving buffer is two frames, which provides a minimum connection delay.

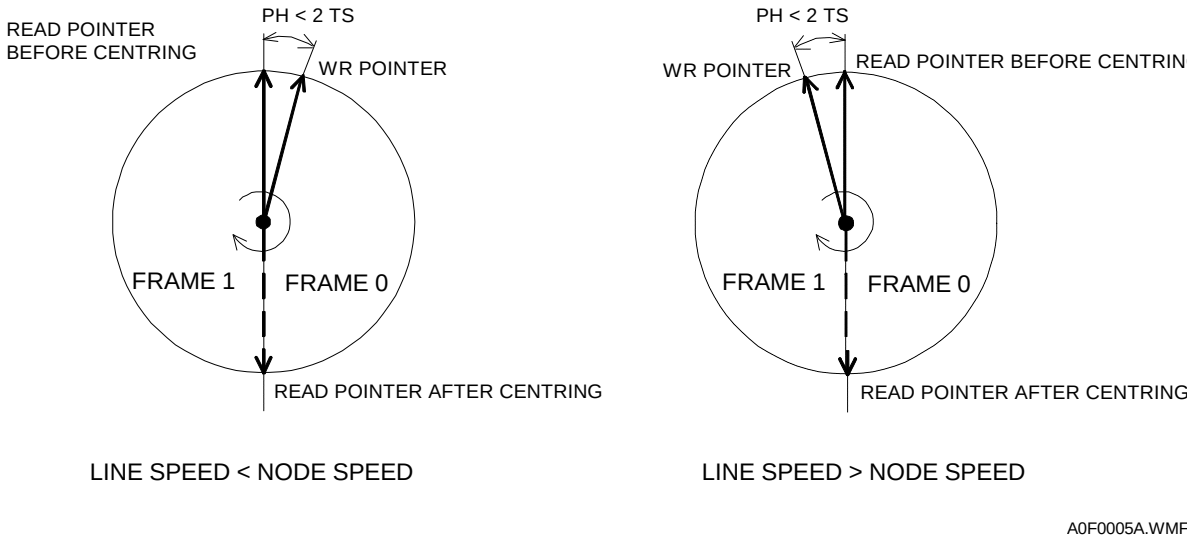


Fig. 94: Centring in an Rx Buffer of Two Frames

In a short buffer the minimum allowed distance between the read and write addresses is one time slot. The distance is checked at intervals of two frames when the read address moves to a new frame. If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. This means that one frame is either lost or repeated once. In a plesiochronous system the distance from the centred position to the position where a new centring occurs is one frame as in , and the interval between the centring situations is:

at 2048 kbit/s	240/df
at 8448 kbit/s	1024/df

where df is the frequency difference between the signal received from the line and the receiving frequency generated by the X-bus clock frequency.

The short buffer can be used for 2048 kbit/s and 8448 kbit/s connections, and then an even distribution is used on the X-bus. This is recommended for trunk lines in order to keep the transmission delays as short as possible.

4 Fr Rx Buffer

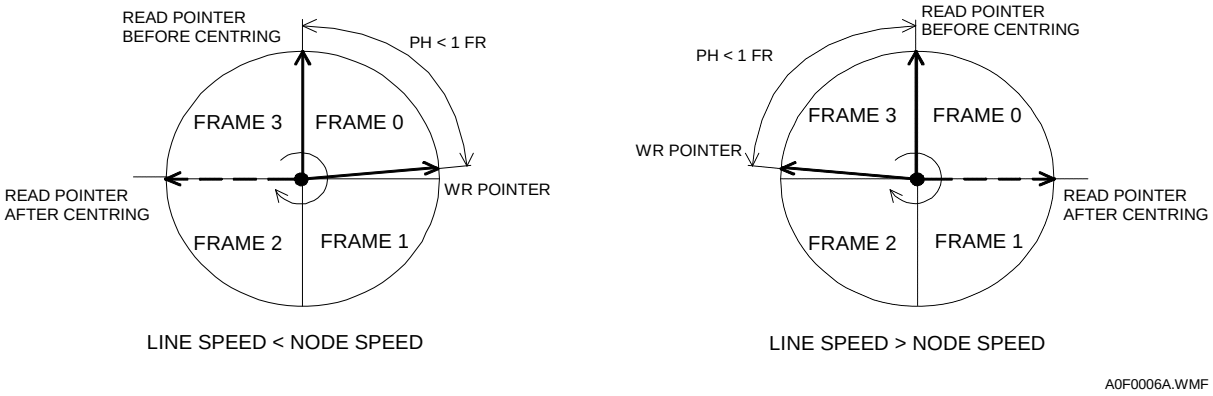


Fig. 95: Centring in an Rx Buffer of Four Frames

The minimum allowed distance between the read and write addresses is one frame. The distance is checked at intervals of four frames when the read address moves to frame Fr0 (from the frame Fr3). If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. The address jump direction depends on the direction from which the write address was closing in on the read address. Centring means here that one frame is either lost or repeated once. In a plesiochronous system with a four-frame Rx buffer the interval between centring situations is:

at n x 64 kbit/s	n x 8/df
at 2048 kbit/s	256/df
at 8448 kbit/s	1056/df

It is recommended that the 4 Fr buffer is used for framed user interfaces and for n x 64 kbit/s trunk lines.

8 Fr Rx Buffer

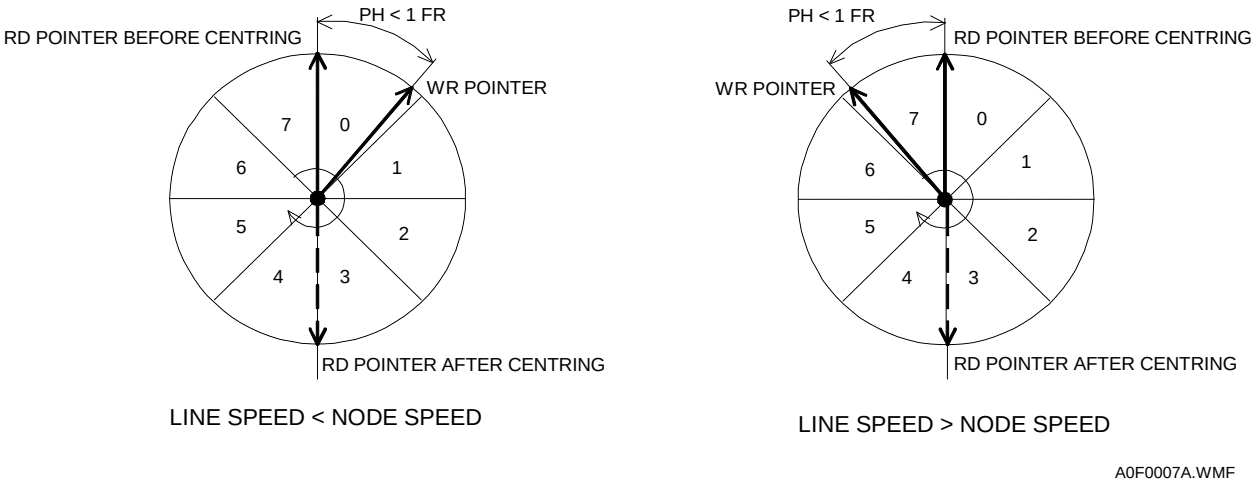


Fig. 96: Centring in an Rx Buffer of Eight Frames

The allowed distance between read and write addresses in an Rx buffer of eight frames is one frame. If a shorter distance is detected by the check, then the read address is moved to a new position four frames farther away. In this case centring means that four frames are either lost or repeated once. The eight frames buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure or a n x 64 kbit/s framing structure is used.

The 8 Fr buffer is the only possibility for Split Trunks. The centring for Split Trunks is defined so that the minimum allowed distance between the read and write addresses is two frames. In other respects the centring is equal to the 8-frame buffer's basic mode.

In a plesiochronous system the interval between centring situations is:

at n x 64 kbit/s	4 x n x 8/df
at n x 64 kbit/s Split Trunk	2 n x 8/df
at 2048 kbit/s Split Trunk	512/df
at 2048 kbit/s	1024/df
at 8448 kbit/s	4224/df

A buffer with a length of eight frames is used for Split Trunk operation. It may also be used for other applications, in particular if unusually large fluctuations have to be handled correctly or if the frame alternation has to be intact also after the centring.

64 Fr Rx Buffer

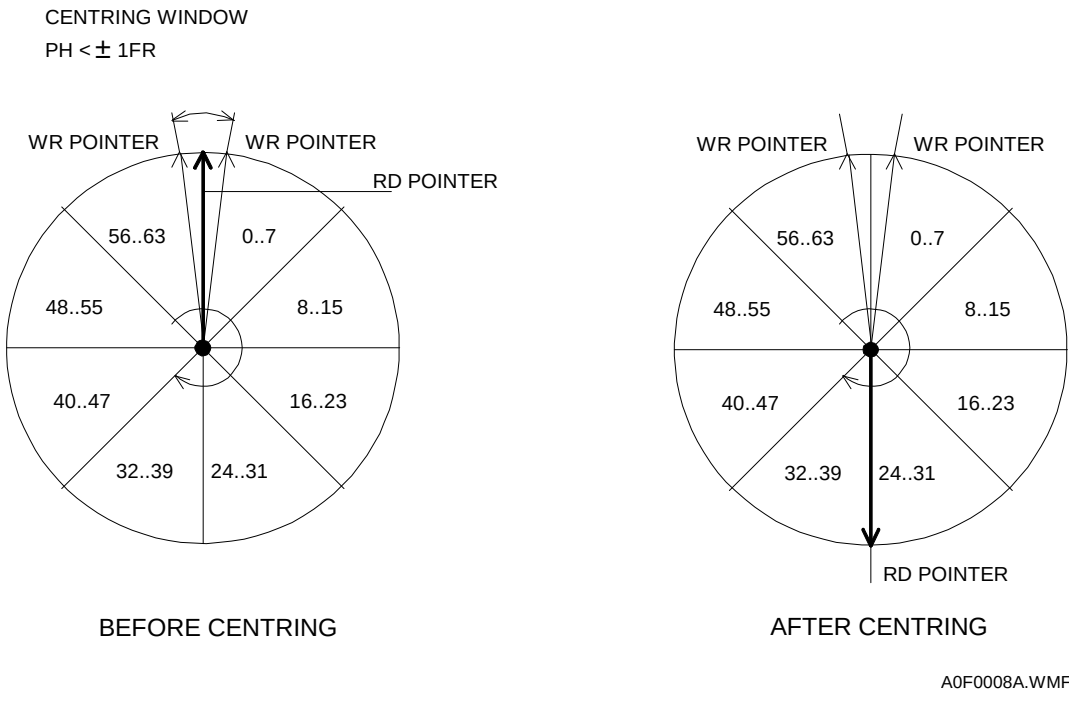


Fig. 97: Centring in an Rx Buffer of 64 Frames

In an Rx buffer of 64 frames a new centring is triggered if the distance between the read and write addresses is less than one frame. Centring means now that 32 frames are either lost or repeated once. The long buffer leads to a delay of up to 63 frames and thus this buffer mode is recommended for special purposes only. The slip distance is very large in a plesiochronous system and the buffer is well suited for large frequency fluctuations. This buffer mode can be used at 2048 kbit/s and n x 64 kbit/s.

In a plesiochronous system the interval between centring situations is:

at n x 64 kbit/s	32 x n x 8/df
at 2048 kbit/s	8192/df

Multiframe Buffers

In the transmitting direction the signalling data is directed through the same buffer as the time slot data. The signalling multiframe of the frame to be transmitted is synchronized to the multiframe clock of the X-bus. The cross-connect unit supplies frame signalling data together with other time slot data of the frame. The GMH unit generates a synchronization time slot in the first frame of the signalling multiframe. Thus the signalling data and time slot data have equal delays in the transmitting direction.

In the receiving direction the phase of the received signal multiframe usually differs from the phase of the X-bus multiframe. Thus the received signalling data has to be buffered until the cross-connect unit performs the cross-connect function for the concerned data. There are two alternatives for the multiframe buffer length: two and four multiframes. The multiframe buffer length depends on the selected length of the frame buffer.

Multiframe Buffers

Frame buffer mode	Multiframe buffer mode	MFr-Rx delay	MFr-Tx delay
2 frames	2 MFr	0…2 MFr	0 Fr
4…8 frames	2 MFr	0…2 MFr	1 Fr
64 frames	4 MFr	1…3 MFr	1 Fr

The length of a frame is 125 μs; the multiframe length is 2 ms.

In both multiframe buffer modes the centring is triggered if the distance between the received multiframe phase and the X-bus multiframe phase is less than one frame. In a buffer with two multiframes the centring is made by moving the write address one multiframe further, which means that the information of one multiframe is lost or repeated. In a buffer with four multiframes the centring means that the information of two multiframes is lost or repeated.

In GMH and cross-connect units the time slot data and signalling data have separate buffers. Therefore there are different delays in the processing of signalling data and time slot data. This means that the signalling data and time slot data which are placed in a transmitted frame do not necessarily originate from the same frame.

6.12.2.7 GMH Operating Modes

Trunk interfaces and user access interfaces are the two categories of DXX node interfaces. Trunk lines are lines connecting the DXX nodes, and the trunks are always framed interfaces. User access interfaces connect lines from users to a node. The user access interfaces can be channel interfaces or framed channel interfaces. GMH units can be used as trunk interfaces or user access interfaces. The user interface presents a G.704 framed channel interface to the user. The most important difference between the trunk mode and the user mode is that the use of time slots in the trunk interface is determined by the Network Management System whereas the use of time slots in a framed channel interface is determined by the user.

GMH Unit as a Trunk

2048 kbit/s Trunk

When a line is used as a trunk line, a part of the frame is dedicated to transfer internal system information. This information will contain data on e.g. network management channels that use the HDLC format. The transmitter will always regenerate the frame synchronization word and the CRC check in a trunk line.

The framing and CRC check have to be selected when a trunk line connection is established. The corresponding HDLC channel has to be activated and bits B5…B8 in time slot ts0 are recommended bits for the link. The trunk buffer is short in order to ensure minimal delay trough the node. It is recommended to activate the signalling time slot CAS of the trunk so that it is always reserved for signalling and not used as a data time slot by the Network Management System.

Split Trunk Lines

A split trunk line can be used to combine several parallel n x 64 kbit/s or 2048 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the n x 64 kbit/s is connected through physically separated cables. The split trunk mode can be used for line speeds n x 64 kbit/s and 2048 kbit/s when a frame with CRC4 is used. The split trunk mode always requires long buffers (eight frames). One of the interfaces will function as a master and the others as slaves. All split components must have same bit rate.

The interfaces are synchronized to each other by their CRC4 multiframe structure. In the transmitting direction the interface transmit buffers and Tx frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will center their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the SXU unit of the receiving node.

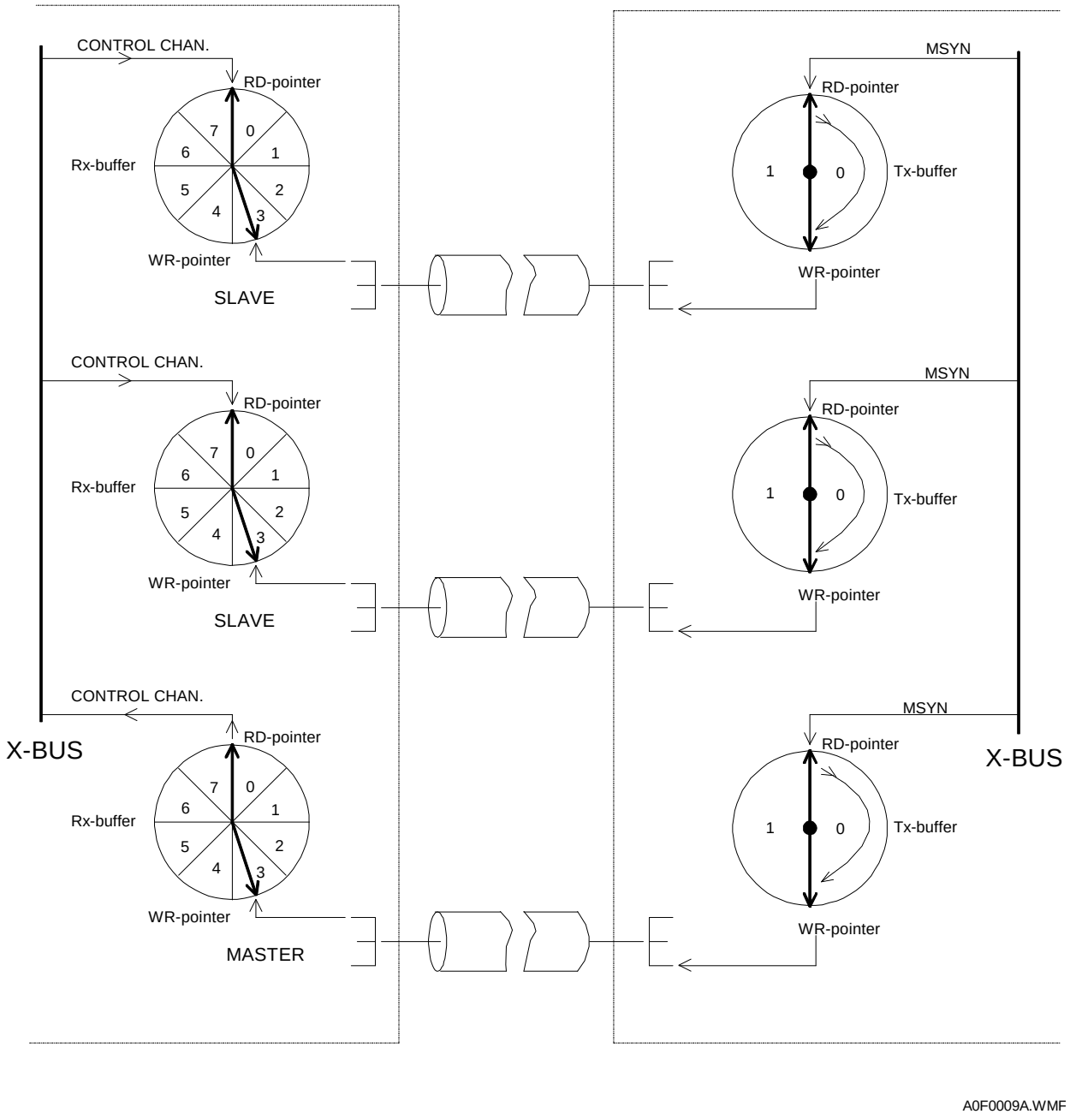


Fig. 98: Split Trunk Line Operating Principle

Theoretically, the maximum delay allowed between lines in a split trunk line is 0.5 frames: due to the centring the master read address occurs when the write address is in the area 6…2. Due to technical reasons, however, the maximum delay is 50 µs.

Each line of a split trunk line will handle its own signalling data. Those lines which carry one or more data channels with signalling data will use the last time slot or ts16 if it is possible as a signalling channel with a multiframe structure. It is not necessary to use a CAS time slot for lines that do not include data channels with signalling.

GMH as User Access Point

The GMH unit can provide a G.704 framed channel interface to the user. The framed user access point has the same features as a corresponding trunk interface. The special bits are used in accordance with customer requirements. There are many possibilities to use the GMH unit as a user access point. Some examples are discussed below.

Framed; With or Without CRC

This is the basic way to connect pieces of equipment which use the G.704 frame structure to a DXX node. Only the data channels in time slots ts1…ts31 are transmitted over the network together with signalling data in the time slot ts16, if required.

The framing structure is demultiplexed at the interface point and only payload data will be supplied to the cross-connect system for further processing. In the transmitting direction the whole framing structure and the frame synchronization word are created in the interface and payload data from the cross-connect is added to the frame. The user equipment to be connected has usually no information about the protocol of the DXX system control channel. Therefore the HDLC channel will not be connected to the interface (with the exception of some DXX system modems). The free bits in time slot ts0 can be set to a state required by the user equipment. The synchronization remote end alarm indication bit RAI may be used, if required by the equipment to be connected. It is recommended to use the CRC check in the interface when the user equipment supports the use of CRC. Some equipment use the CRC E bits in a way not conforming to standards and in such cases unnecessary alarms can be avoided by setting the bits in a fixed state, usually 1.

When individual channel signalling is used, the multiframe structure in the receiving direction is demultiplexed in the interface and the signalling for each channel is transferred to the cross-connect for further processing. In the transmitting direction the multiframe synchronization time slot is created in the interface and stuffed with free bits. Signalling data from the cross-connect is placed into the signalling time slot. The free bits usually have the Permanent 1 state. If no signalling is used, then also time slot ts16 may be used to transmit payload data.

Framed; Transmission of Free Bits in ts0 Through the Network

It is possible to transmit the free bits of time slot ts0 through the DXX network when the equipment connected to a DXX node can utilise these free bits. Other functions may be the same as in the previous example. The free bits of time slot ts0, which are utilised by the application and transmitted through the network, are set to the X-conn state when the GMH unit parameters are defined. The unit will then transmit these bits in the same state as it receives them from the cross-connect. Accordingly, bits received in time slot ts0 are supplied to the cross-connect in the same state as they are received.

On the transmission line the data transmission capacity is 4 kbit/s for one free bit in time slot ts0 due to the frame alternation. The total data transmission capacity of all five bits B4...B8 is thus 20 kbit/s. However, the DXX system utilises a format where one free bit of time slot ts0 uses a capacity of 8 kbit/s on those connections on which it is transmitted through the network. Thus, a total capacity of 40 kbit/s is required to transmit all bits B4...B8 through the network. Transmission of the free bits of time slot ts0 always uses 64 kbit/s of the DXX node internal X-bus capacity for each interface, regardless of the number of transmitted bits.

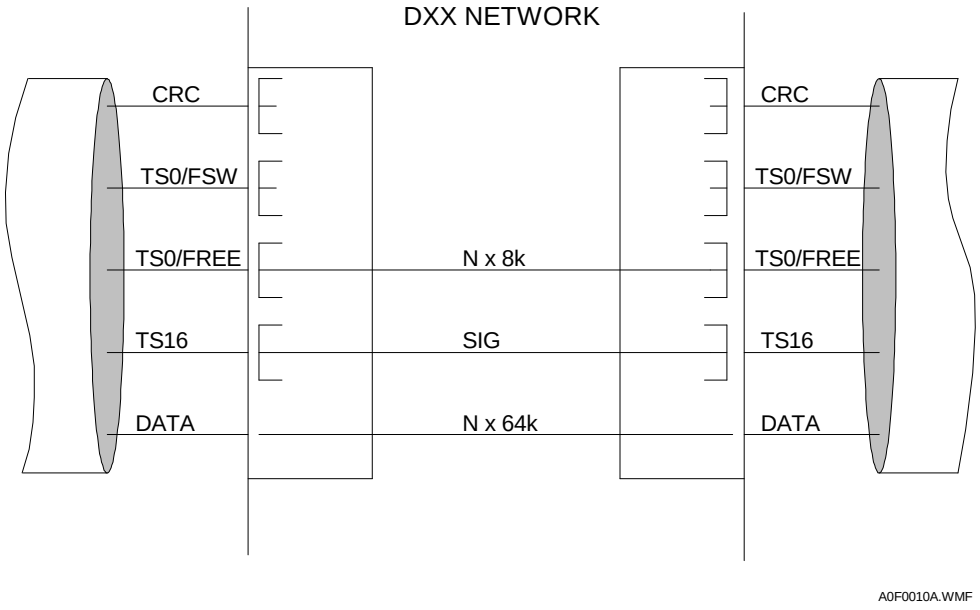


Fig. 99: TS0 Free Bits Connected Through the Network

Framed; Transmission of Time Slot ts0 Through the Network

It is possible to use the frame synchronization word to monitor the complete connection through the DXX network. In this case the whole time slot ts0 is directed via the cross-connect and transmitted to the far-end equipment. In this case the frame synchronization word, the free bits of time slot ts0 and the frame remote end alarm are transmitted over the whole connection. If it is required to connect signalling data separately over this connection, then the CRC check has to be regenerated in the user access interface. A new CRC check sum has to be calculated because the frame contents will change due to the different treatment of signalling data and normal data. The CRC check may be inactivated when the user equipment does not support the use of CRC.

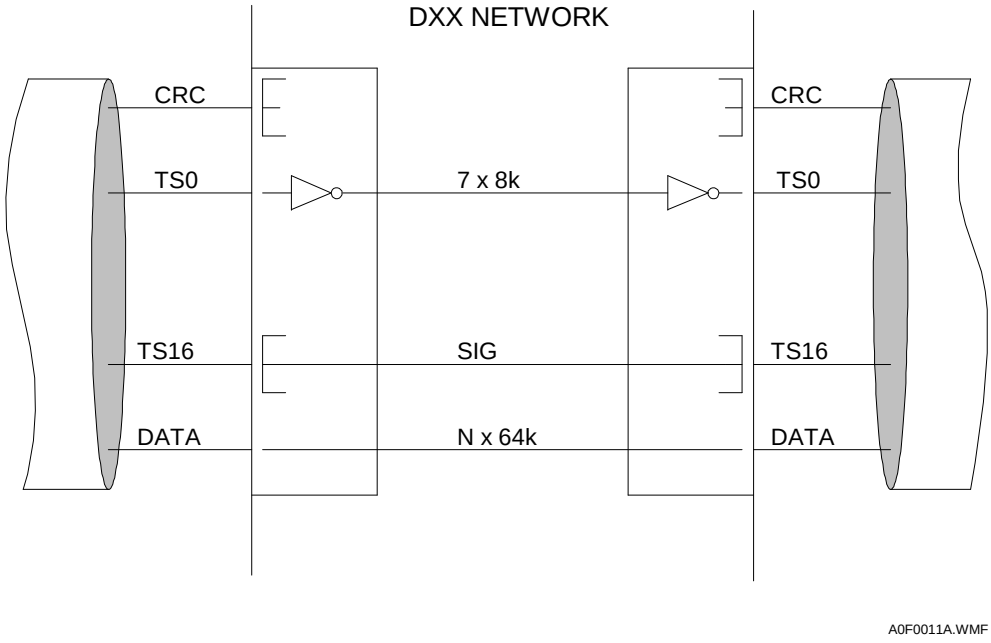


Fig. 100: Ts0 Connected Through the Network

When it is connected to the transmission network, the time slot ts0 is inverted in the receiver before it is forwarded to the cross-connect. The time slot is in the inverted state when it is transmitted through the network, and in the far-end user access interface it is again inverted into its original format and then added to the frame as the synchronization time slot. The time slot ts0 is inverted so that it cannot cause false synchronization of the trunks when it propagates through the network. A trunk capacity of 56 kbit/s is used in order to transmit the whole time slot ts0 through the network. The transmission of the time slot ts0 uses 64 kbit/s of DXX node internal X-bus capacity for each interface.

When the interface parameters are set (during commissioning), the Fault consequence BER 10E-3 should be set Off. This causes received data with a bit error rate worse than 10E-3 (calculated with the aid of the frame synchronization word) to be connected through the network, and not to be set AIS as in normal transmission.

When the time slot ts0 is transmitted through the network, he user access interface will respond to errors in a way different from the normal. The remote end frame level alarm bit is not activated when the user access interface receiver detects a serious frame error, because this error will cause the remote end user equipment to respond, e.g. through the AIS, and to activate the remote end alarm bit. The remote end alarm bit is then transmitted back to the near-nd user equipment. Moreover, the GMH unit will not respond to a received FrFEA bit. If an interruption occurs in the transmission network and an AIS is given instead of a payload signal to the interface, then this condition will be detected in the transmitter and an AIS is sent to the user equipment. The interface simultaneously activates the AIS from X-bus alarm.

Framed; Ts0 and CRC Connected Through the Network

It is possible to monitor the quality of the user's connection over the whole network with the aid of the CRC check. To enable this, a combination of the time slot ts0 and the CRC check is sent through the network from the near-end user equipment to the far-end user equipment. The CRC check sum is calculated for the total signal. In order to get equal results in the unit creating the CRC check sum and in the unit evaluating the CRC check sum, all bits must have the same state at both locations. The receiver will receive signalling data and payload data through different delays, and therefore it is not possible to use cross connected channel signalling, if the CRC check is transmitted over the connection. The idle data of possibly unused time slots has to be the same at both ends of the connection.

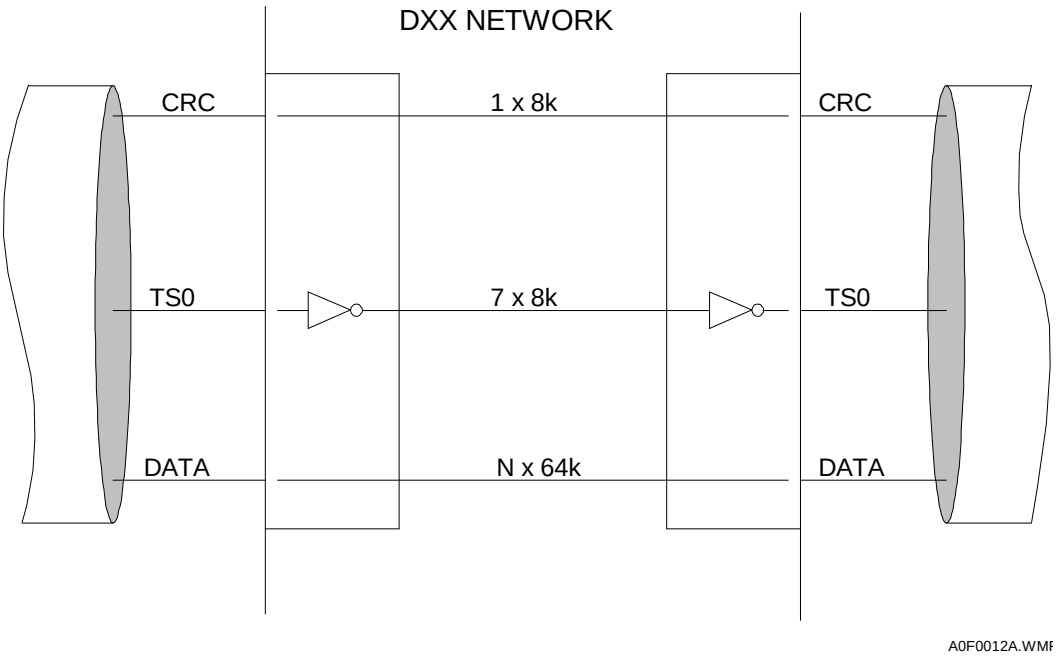


Fig. 101: Ts0 and CRC Connected Through the Network

The time slot ts0 is inverted before it is transferred to the transmission network. A capacity of 64 kbit/s is used on a trunk line to transmit the combination of time slot ts0 and the CRC check, and 64 kbit/s of the internal DXX node cross-connect bus. CRC check E-bits indicating remote end block errors are also connected through the network. If these bits are not used they must set to the state 1. The interface responds to errors in the same way as when only time slot ts0 is connected through the network.

Transparent Without Frame

The interfaces of a GMH unit can also operate in a transparent mode. In this mode the received signal is connected through the network without any manipulations. The receiver is not synchronized to the incoming signal frame structure; no additions to the output signal are made in the transmitter. However, the receiver does cut the signal into slices of eight bits, which are transmitted through the network and from these slices a signal conforming to the original signal is then reconstructed in the receiver. In the transmission network a transparent signal requires a capacity according to its interface bit speed.

In order to use the interface in the transparent mode the interface parameter Framing must be set Off during parametrization. No frame errors are detected in the transparent mode, as the frames are not processed in any way. An alarm for error rate 10E-3 will be calculated only from code errors, whereas the error rate in a normal mode is calculated using also frame synchronization word errors.

Transparent With CRC Monitoring

The interface can be set to a function mode, in which the signal is transparently connected through the network, but in which the user access interface receiver synchronizes to the received signal frame structure and performs a CRC check on the signal. In the transmit direction the signal contents is not changed. The interface is set into this mode by defining the Framing parameter as CRC monitor during parameterization. The interface will also output framing error information, but actions on these errors are prevented.

6.12.2.8 1+1 Protection

The interface can be 1+1 protected by another interface of the same unit. In protected mode both channels must have the same speed and framing mode settings. A unit working in the protected mode will look like a cross-connect port towards the X-bus. In the protected mode both channels transmit the same data signal coming from a buffer. Both channels use their own frame mux to create the frame structure. The receiving direction includes a change-over switch that selects the active receiver. Rx signal faults are classified into several categories. The switch uses fault categories to select the interface to be used. The fault categories are indicated in the fault table. For example 1.x means first category (worst or most serious fault).

The operating modes of the change-over switch are:

— normal operation
— prefer operation
— forced operation

In the normal operating mode the switch will automatically switch to the other interface if the Rx signal fault category (1, 2, 3, 4, 5, OK) of the active interface continuously is worse than the fault category of the other interface, for a longer period than the given time delay. No switchover operation is activated when the categories are equal for both interfaces.

In the prefer operating mode a switch-over is triggered if there is a difference between the interface fault categories; the better interface is switched active. In a situation with equal fault categories for both interfaces the switch selects the preferred interface.

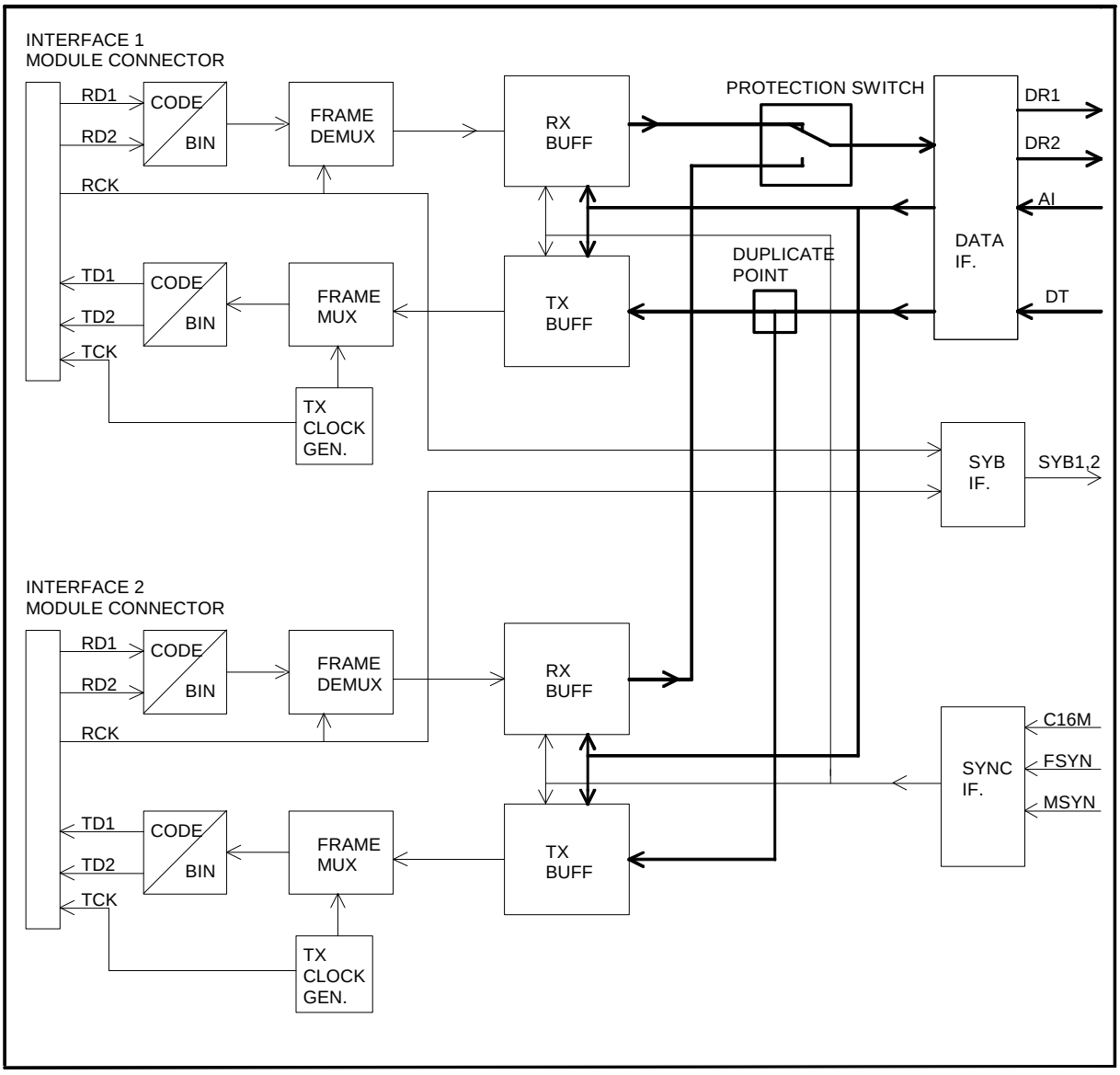


Fig. 102: Block Diagram of Protection

In forced operating mode the switch is forced to switch over without delay. Received data from the active interface is immediately connected to the X-bus. In this situation the Protection switch forced fault message with status MEI appears, and the red LED is turned on.

A switch operating time delay is defined for the prefer operating mode and the normal operating mode. The delay is defined as n x 10 ms, where n=0...6000; i.e. the delay is 0...1 minutes. The delay defines the allowed fault duration before the switch is triggered to switch over.

Fault and Service Status (PMA, DMA, MEI, S) in 1+1 Mode

In principle both interfaces generate their own alarms (alarm messages with fault status). PMA and S statuses are processed in this mode.

PMA Status Processing

In the protection mode the normal PMA status is changed to the DMA status and there is an additional fault condition, Loss of protected signal, with a PMA status. In normal or prefer operating modes this special condition is created when both interfaces have a fault with fault category 3 or worse. In the forced operating mode this condition occurs if the forced interface has a fault with fault category 3 through 1. The inactive interface is not able to generate a fault with the PMA status.

S Status Processing:

In the protection mode an S status is generated only in the Loss of protected signal fault condition.

Far-End Alarms in 1+1 Mode

A far-end alarm indicates that the Rx signal is out of service (S status)

FrFEA	= Rx frame out of service
MFrFEA	= Rx multiframe out of service

Tx far-end alarms (FrFEA, MFrFEA) of both interfaces are generated assuming a fault status of the active interface. During a short period, when the change-over switch is in a transition phase, the far-end may generate an alarm even if there is no fault in the better interface. In forced operating mode only the active forced interface can cause far-end alarms to be sent.

RxAIS Processing

RxAIS and RxAIS to SigTS are always generated when FAE or MFrFAE is sent. AIS generating depends on the fault status of the selected interface.

6.12.2.9 Loops in GMH

The NMS is able to control several loops in the GMH unit. Loops and measurement points are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop time-out control which will turn off a loop when the user defined time has come to an end.

Interface Loop

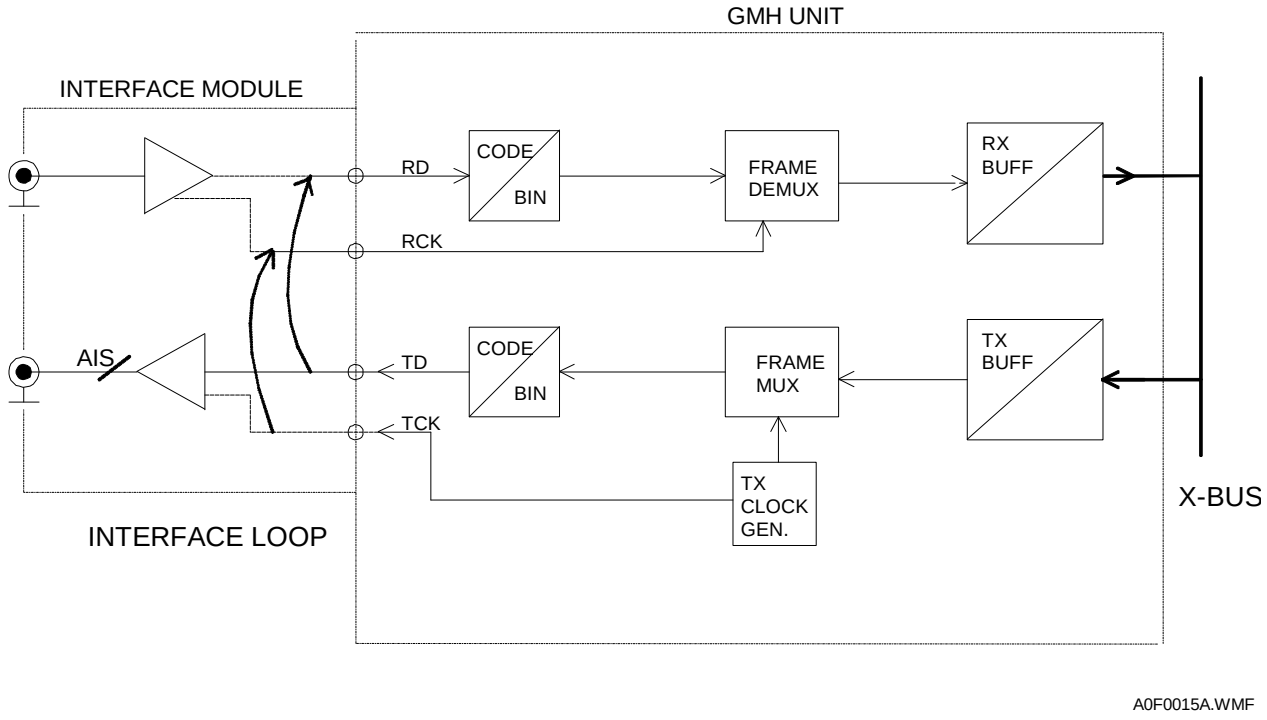


Fig. 103: Interface Loop

An interface loop is created in the interface module. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm LED is switched on.

The type of the module determines the point where the loop is created in the module. In most cases, due to technical reasons, the loop is not made using a signal with line level. The loop will, however, always test the interface module control bus and connectors and a part of the module logic. The line coder and decoder as well as the frame multiplexer and demultiplexer are also tested in the loop. There should be no other faults in the unit's fault list when the loop is created.

Equipment Loop

In an equipment loop the transmit data from the G.704 multiplexer before the interface module is looped back to the demultiplexer. The interface sends an AIS and the yellow alarm LED is switched on.

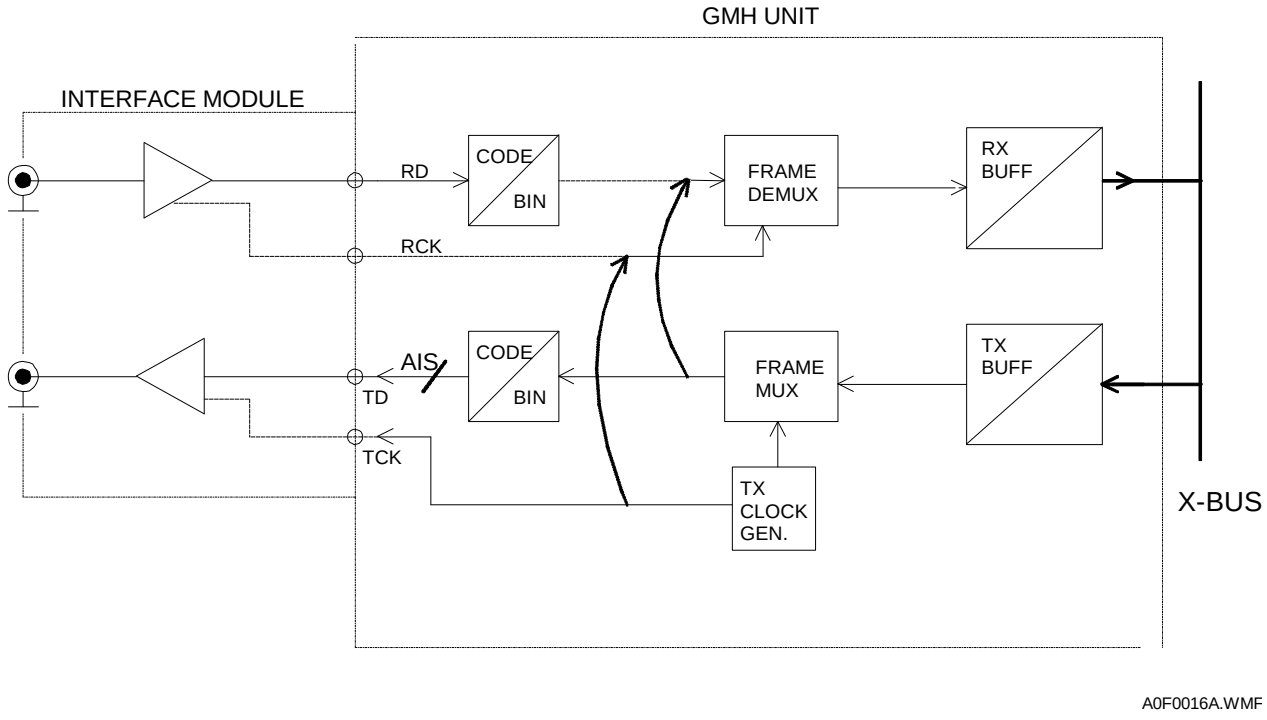


Fig. 104: Equipment Loop

The equipment loop is made in the unit. This loop tests the frame multiplexer and demultiplexer. Neither the line coder/decoder nor the interface module are included in the loop. It is also possible to detect faults in the transmitting and receiving buffers when a test signal from a measurement equipment is added to the signal passing through the looped channel. If no problems are detected with the interface loop, it is suggested to perform a test with the equipment loop to ensure that the module is in order.

Line Loop

In the line loop the Rx data received by the interface module is looped back to the interface transmitter. The received clock signal is used as the transmitter clock. AIS is connected to the X-bus instead of the received signal. The yellow alarm LED is switched on.

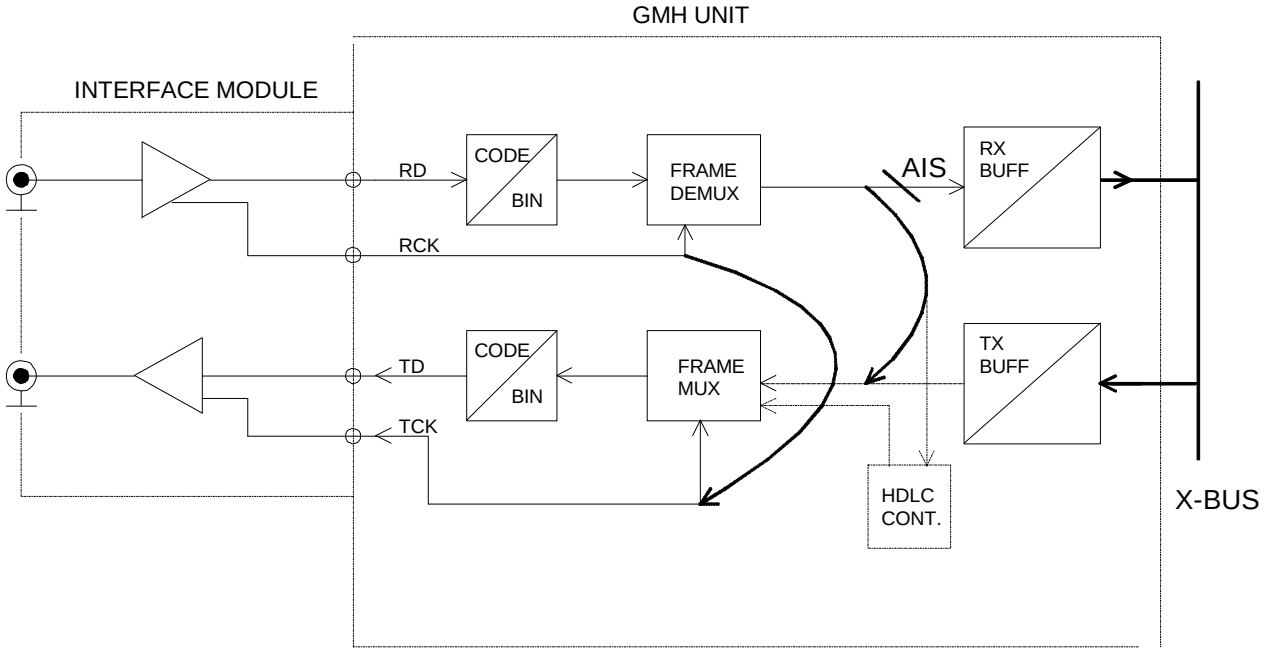


Fig. 105: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the Line Loop Test. When it is used, the HDLC controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made, the yellow LED of the unit which controls the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

Clock RAI

The GMH unit can employ a dedicated bit of the frame structure as a far-end clock alarm bit. When a node loses the synchronization with the network, it activates the alarm bit. When the node receiving synchronization from the faulted node detects the alarm state of this bit, it can cease to use the corrupted clock and select the next clock source from the fallback list.

The NMS is able to select the bit used as a clock RAI. The user must choose a time slot and a bit for the clock RAI. The clock RAI time slot cannot be used for payload data. Special bits like HDLC can, however, be used in the same time slot with the clock RAI. The user must also select the polarity (active state).

The interface activates the clock RAI in the transmitting direction when it receives an alarm message from the SXU unit via the control bus. The clock RAI is inactivated in a corresponding manner.

In the Rx direction the clock RAI bit is separated from the incoming data and sampled by the processor with a sampling period of about 10 ms. The state of the bit is preserved when two consecutive equal states are detected. When a unit in the active state receives the clock RAI bit, it will cut off the SYB clock if it has one. If the SXU loses the SYB clock, it will select the next clock source in the fallback list. If the clock signal is lost for a short period, the GMH unit returns the clock to the SYB bus when the clock RAI is inactivated and then the SXU unit again will use the clock. If the synchronization is lost for a longer period, the SXU unit will remove the faulted interface from the SYB bus by a command through the control bus; thereafter the SXU directs a command to the next object in the fallback list without an SYB bus to have it connect the clock to the cleared SYB line.

6.12.3 Interface Modules for GMH Interface Unit

6.12.3.1 The interface modules available for GMH unit:

- LTE
- OTE-LED
- OTE-LP
- G703-75
- G703-120
- G703-8M
- BTE-320
- BTE-384
- BTE-576
- BTE-1088
- BTE-2028-2W
- BTE-2048
- BTE-2304
- BTE-4096
- X21-G704-S
- V35-G704-BS

6.12.4 GMH Faults and Actions

6.12.4.1 Terminology

The following acronyms will be used in the tables below:

— PMA = Prompt Maintenance Alarm
— DMA = Deferred Maintenance Alarm
— MEI = Maintenance Event Information
— S = Service Alarm
— R = Red alarm LED
— Y = Yellow alarm LED
— RB = Red alarm LED blink
— TxAIS = AIS insertion to Tx signal
— RxAIS = AIS insertion to Rx signal
— TxTS-AIS = AIS insertion in time slots of Tx signal
— FrFEA = Frame level far-end alarm (ts0/B3 in 2Mbit/s frame, ta66/B7 in 8 Mbit/s frame)
— MFrFEA = Multiframe level far-end alarm (FR0/ta sig/B6)

MFrFEA is also transmitted if FrFEA is transmitted.

6.12.4.2 Tx Signal Faults (Block 1,2)

Fault Condition	Status	LED	Tx signal
Tx Clock fault (PLL)	PMA, S	R	TxAIS
Bus faults IA activity missing Bus sync. fault (block 0)	 PMA, S PMA, S	 R Y	 TxTS-AIS TxTS-AIS
AIS from X-bus	MEI, S	Y	TxAIS [a]
BTE Tx line test	MEI, S	Y	Test pattern

a Only when FAS is transferred through the network.

6.12.4.3 Rx Signal Faults (Block 1,2)

Signal & Frame Faults	Status	LED	Rx signal	Tx signal
1.1 Interface module missing	PMA, S	R	RxAIS	-
1.2 Wrong interface module	PMA, S	R	RxAIS	Tx signal cut
1.3 Rx signal missing	PMA, S	R	RxAIS	FrFEA
1.4 Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
1.5 Loss of frame alignment 1.5.1 Frame alignment lost 1.5.3 Frame alignment lost by CRC ≥ 915/1000 errored CRC-blocks 1.5.2 CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
1.6 BER 10^{-3} - frame alignment word (normal error response) - line code errors - n x 64 kbit/s baseband signal	PMA, S	R	RxAIS	FrFEA

Signal & Frame Faults	**Status**	**LED**	**Rx signal**	**Tx signal**
1.7 Wrong input signal				
1.7.1 Own NNM messages received	PMA, S	R	RxAIS	-
1.7.2 Wrong IDs in NNM messages (detection can be inhibited)	PMA, S	R	RxAIS	-
1.7.3 No response to NNM message	PMA, S	R	RxAIS	-
1.8 NTU problems	MEI	Y	-	-
1.8.1 NTU power off/local loop	MEI	Y	RxAIS	-
1.8.2 NTU line break	MEI	Y	-	-
1.8.3 NTU short circuit	MEI	Y	-	-
1.9 ASIC register error	PMA, S	R	-	-
Loops	Status	LED	Rx signal	Tx Signal
2.1 Local loops				
2.1.1 Interface back to equipment	MEI, S	Y	-	TxAIS
2.1.2 MUX/DEMUX back to eq.	MEI, S	Y	-	TxAIS
2.1.3 MUX/DEMUX back to line	MEI, S	Y	RxAIS	-
2.1.4 Line loop made by neighbour	MEI, S	Y	RxAIS	-
2.2 Remote loops				
2.2.1 Remote controlled line loop (2.1.4)	MEI, S	Y	-	-
Multiframe level faults	Status	LED	Rx signal	Tx signal
3.1 Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
3.2 AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Multiframe faults of the 8 Mbit/s signal are detected separately in each of the four signalling time slots (groups).				
Far-end alarms	Status	LED	Rx signal	Note
4.1 Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
4.2 Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Degraded signal	Status	LED	RxAIS	FrFEA
5.1 Error rate 10^{-3} - frame alignment word (AIS insertion inhibited)	DMA	R	-	-
5.2 Error rate 10^{-6} - CRC block errors - line code errors (used for speeds over 1 Mbit/s)	DMA	R	-	-
5.3 Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
5.4 Buffer slips/1 hour	MEI	RB	-	-

6.12.4.4 Miscellaneous Faults (Block 1, 2)

Fault Condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

6.12.4.5 1+1 Protection Switch Fault Messages (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	-	- [a]

a Signal actions depend on actions of the protected interfaces.

6.12.4.6 Common Logic Faults (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal	Note
Reset	PMA, S	R	Bus if off	Off	[a]
Power supply (5V,+12V,-10V)	PMA	R	-	-	[b]
CPU memory faults RAM fault EPROM fault FLASH faults	PMA, S	R	-	-	-
Incompatible EPROM/FLASH SW	PMA	R	-	-	-
Check sum err in downloaded SW	PMA	R	-	-	-
SW unpredicted	PMA	R	-	-	-
Missing settings	PMA, S	R	-	-	-
Start request denied	PMA, S	R	Bus IF off	AIS	-
Tx RAM error	PMA, S	R	-	-	-
Rx RAM error	PMA, S	R	-	-	-

a Fault message (with delta event) appears when the unit starts to operate.

b Rx signal action fdepends on the frame level alarm of the corresponding interface.

6.12.5 GMH Technical Specifications

6.12.5.1 Frame and Multiframe Operation

Filtering of FEA and MFrFEA bit:

The state of the alarm bit will switch if the opposite state is received three times consecutively.

AIS in frame 2048 kbit/s and n x 64 kbit/s:

Signal containing two or less zeros in a 2-frame period is recognised as an AIS signal.

After AIS is detected, a signal containing three or more zeros in a 2-frame period is recognised not to be an AIS signal.

AIS in frame 8448 kbit/s:

A signal containing less than eight zeros in a 2-frame period is recognised as an AIS signal. After AIS is detected a signal containing 12 or more zeros in a 2-frame period is recognised not to be an AIS signal.

AIS in multiframe:

A signal in the signalling time slots containing one or no zeros in a multiframe period is recognised as an AIS signal.

Error rate 10E-3 limits from frame alignment word:

2048 kbit/s and n x 64 kbit/s count time is four seconds	
Count to activate alarm:	94
Count to inactivate alarm:	17

8448 kbit/s count time is 2 seconds	
Count to activate alarm:	199
Count to inactivate alarm:	48

Error rate 10E-3 limits from code errors:

Speed kbit/s	**Activate**	**Inactivate**
8448	8296	893
2048	1973	229
1088	1033	126

Count time is one second

CRC spurious frame alignment limits:

speed kbit/s	values from 1000 counted to start a new frame search
256	613
320	637
384	660
448	681
512	700
576	719
640	736
704	753
768	768
1088	832
2048	915
8448	826

6.12.5.2 Measurement Point

Measurement signals	Selectable IF1 or IF2: Tx data or Rx data or Tx clock or Rx clock
Impedance	75 ohm
Connector	SMB connector plug
Grounding	Cable outer conductor is connected to the ground of unit
Code	Signal is HDB3 coded with all speeds and interface modules
Pulse shape	G.703 Fig. 15 at 2048 kbit/s when data measurement
	G.703 Fig. 16 at 8448 kbit/s when data measurement
	2048 kbit/s and 8448 kbit/s clock measurement:
	Vmax 1,5 V
	Vmin 0,75 V
	T = 488 ns at 2048 kbit/s
	T = 118 ns at 8448 kbit/s

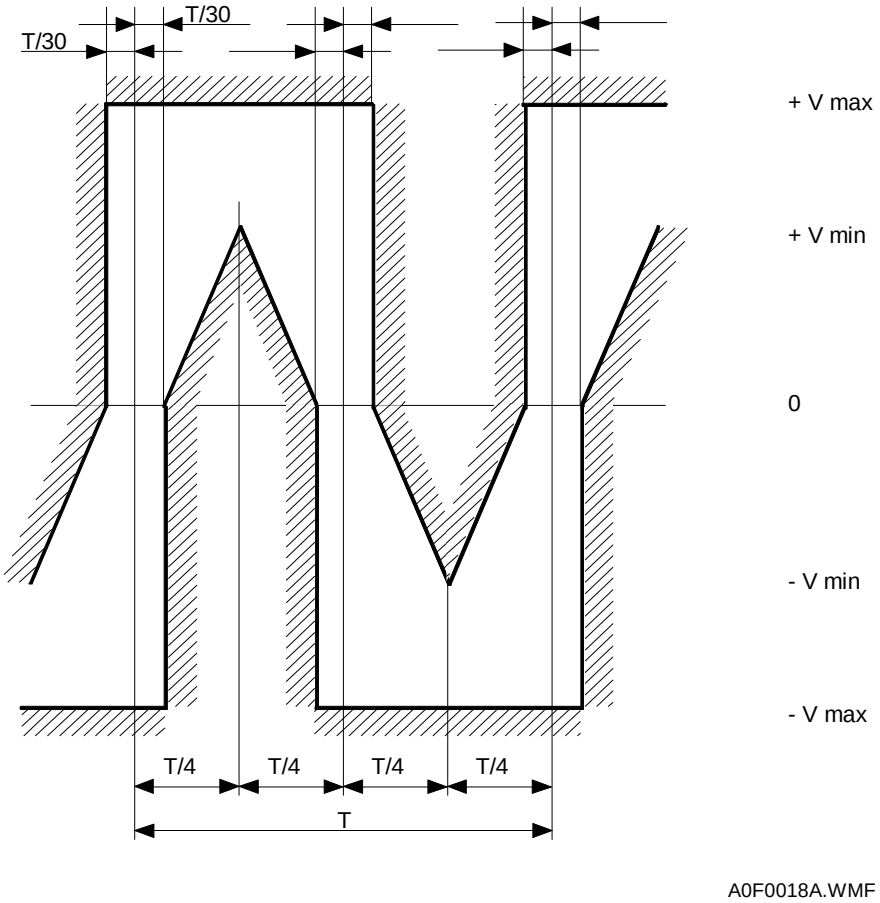


Fig. 106: Clock Output Pulse Mask for Measurement Point

6.12.5.3 Power from Battery

The power requirements depend on interface cards and line speed. The power may be calculated by adding values from the list below (values are prepared for calculating only, no absolute values)

GMH 220 without modules	3,6 W
BTE-384	1,5 W
BTE-768	3,0 W
G703 at 2048 kbit/s	1,1 W
G703 at 8448 kbit/s	1,8 W
LTE at 1088 kbit/s	1,0 W
LTE at 2048 kbit/s	1,1 W
V35-G704	1,2 W
V36-G704	1,0 W
OTE-LED at 2048 kbit/s	3,1 W
OTE-LED at 8448 kbit/s	3,7 W
OTE-LP at 2048 kbit/s	5,0 W
OTE-LP at 8448 kbit/s	5,4 W

6.12.5.4 Mechanics

Weight:

— 400 g with power module, without interface modules
— 620 g with two GDH 230 modules
— 650 g with two OTE 233 modules
— 660 g with two OTE 234 modules
— 665 g with two BTE 237 modules

Unit dimensions:

— 25 x 160 x 233 mm

6.13 GMM Interface Unit

6.13.1 General

The GMM unit processes framed and unframed signals received from the T1 interface module. The unit provides two independent T1 transmission channels as well as an internal communication link to the DXX system.

6.13.1.1 Mechanical Design

The mechanical design of the GMM unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; however, the general recommendations for subrack equipping should be followed.

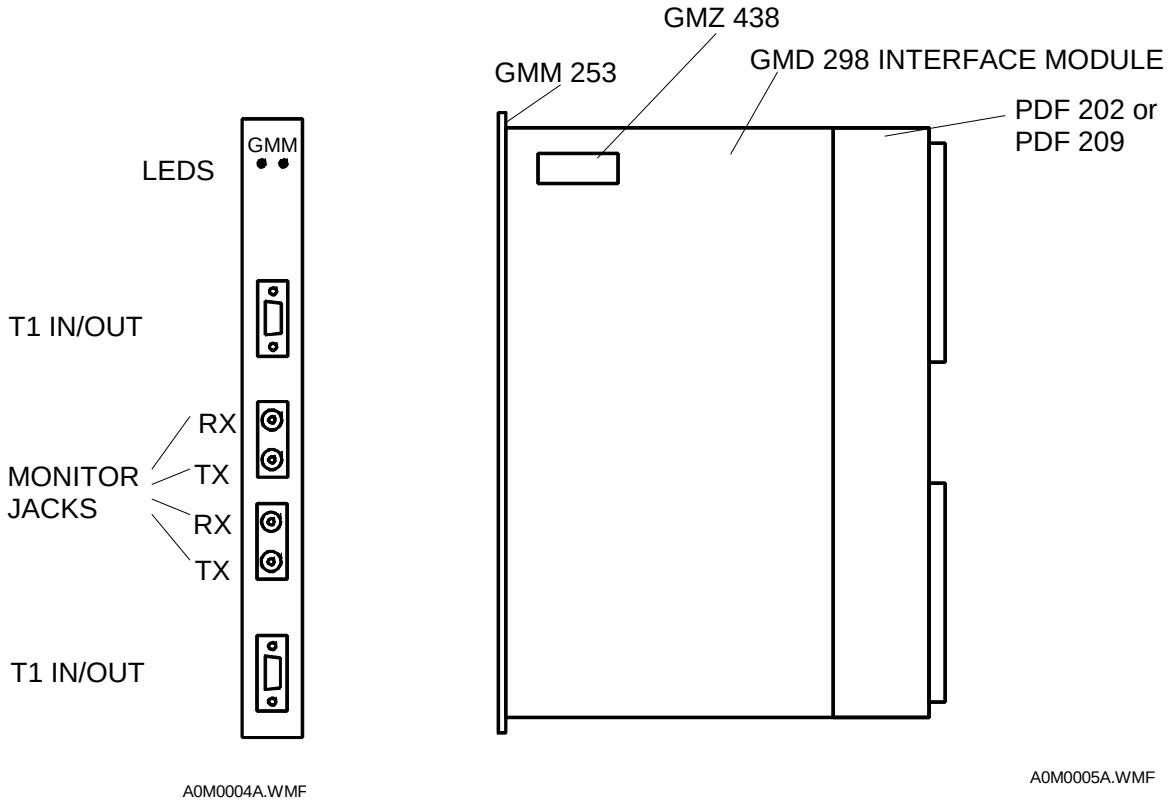


Fig. 107: GMM Unit Equipped with T1 Interface Module

The configuration of the GMM unit consists of a unit power supply PDF 202 (-48V) or a PDF 209 (-24V), program memory GMZ 438. It is used with a dual interface module T1.

The unit front panel houses alarm LEDs, input and output connectors (15-way D-shell) for both interfaces, and monitor points (mini bantam) for both transmit and receive signals.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the subrack control bus and for the data transmission processing.

6.13.2 Operation

6.13.2.1 Functional Structure

The main functional blocks of the GMM unit include the processor block, the communications circuitry, the signalling conversion circuit and the X-bus interface.

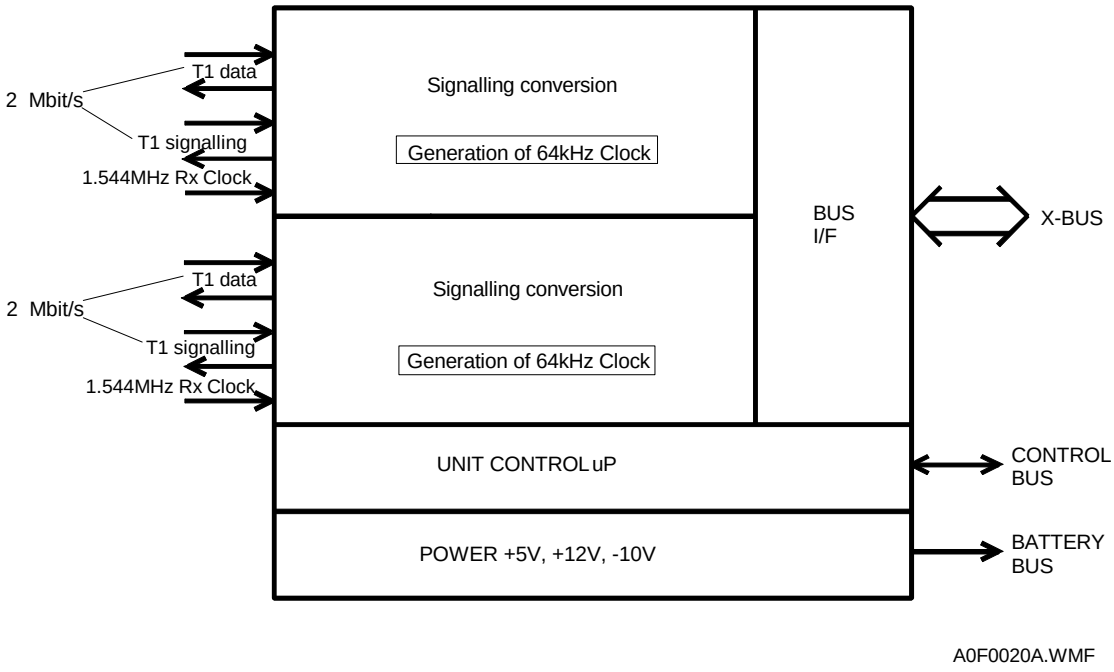


Fig. 108: Block Diagram of GMM Unit

The power supply generates the operating voltages required by the unit from the battery voltage provided by the X-bus. The operating voltages are monitored in the GMM so that an incorrect voltage level shall cause an alarm.

The processor block controls and monitors the operation of the unit. Control and status information is passed to and from the processor block via an internal control bus within the subrack. Through this control bus, the processor can also communicate with other units in the subrack. The processor generates HDLC messages and processes the HDLC messages received by the T1 interfaces.

The T1 interface circuits provided on the T1 interface module convert the analog line signals to/from signals suitable for the unit's digital circuits. These circuits provide SF and ESF framing circuits, various line coding schemes, line protection circuitry, line build-out circuits and HDLC data-link insertion. In the receive direction, a signal attenuated by up to 20dB may be recovered from the line and a 1.544MHz clock extracted. The reference clock extraction circuitry takes this recovered 1.544MHz clock and creates a 1536Hz signal acceptable to the SXU for use as a clock reference. In the transmit direction, data pulses are generated in the required format for transmission with line-build-out options of 0dB, 7.5dB, 15dB and 22.5dB.

The signalling conversion circuitry converts from the T1 robbed-bit signalling format to an E1 TS16 format, and vice versa, which allows signalling to be switched through the DXX between T1 and E1 modules.

The X-bus interface adapts the back plane bus to the unit. It transfers timing signals and control information to the unit and signals from the bus to the channels, and in the opposite direction, it transfers data and monitoring information from the channels to the bus. The X-bus interface circuitry prevents the unit from interfering with bus functions when the unit is inserted/removed into/from the subrack slot and during a unit failure.

Power Supply

A GMM unit receives its operating power from the power supply module PDF202. This module can be replaced a whole. It is plugged into the unit with connectors and fixed with screws in a position reserved for it on the unit. The battery voltage which is used as supply for the power supply module is connected from the DXX-bus through the bus connector. This battery voltage is a nominal -48V battery when a PDF 202 is used. The GMM unit also operates with a PDF209 power supply module which requires a +24V battery voltage from the DXX-bus. The power supply module generates +5V (VCC), +12V and -10V supplies for the unit. The unit also receives a +5V supply from the back plane which is supplied to the interface circuit connected to the bus during start-up. The operating voltage, VCC, of the unit is monitored by a power-reset circuit, and a low operating voltage causes a unit reset. All of the operating voltages as well as the +5V bus voltage are monitored by an A/D converter. An alarm is generated if a voltage exceed its limits.

Processor

The unit is controlled by a 80C188 microprocessor. The system and application parts of the code, identified as GMZ 438, are stored in an interchangeable EPROM memory. The application software may also be stored in non-volatile FLASH memory and thus it is possible to update this without removing the unit from its environment. Non-volatile memory is also used to store the unit's operating parameters and the unit identification so that in the event of power interruption, the unit is automatically restored to the conditions prevailing before the interruption. The unit also has RAM used as a working storage area, e.g. stack and data buffers.

Control Bus

The unit communicates with other units in the subrack via the control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit setting can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When the unit is transmitting, it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

6.13.2.2 X-Bus Interface

The X-bus interface provides the interface between the GMM unit and the back plane bus. The cross-connect unit supplies a 16.896MHz to the GMM through the X-bus. This 16.896MHz clock is the central clock of the subrack, and it is divided down to a 2.048MHz clock on the GMM. The X-bus also supplies a frame alignment signal at 8kHz and a multiframe alignment signal at 500Hz to the GMM unit.

The cross-connect unit exchanges data with the GMM unit by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Receive and transmit data is carried on separate 8-bit wide buses. The receive data bus DR1 is protected by the data bus DR2. The cross-connect unit determines with the aid of a bus test which bus to use, and this information is supplied to other units via the control bus. The GMM receives a time slot address from the cross-connect unit, and puts its transmit data onto the bus during that time slot. Allocation of time slots on the X-bus may be either Even or Uneven.

Bus functions are monitored by the GMM. When an interface is synchronized and a corresponding cross-connection made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and the multiframe synchronization signal. If the multiframe synchronization signal is missing, the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the IA Activity Missing alarm.

Even Allocation

When the T1 interface is configured for even allocation, 32 evenly allocated time slots are reserved on the back plane upon locking the interface. As the reserved time slots are evenly spaced within a frame, the delay through the system is minimized. Using even bus allocation allows the T1 interface to meet the transfer delay requirements of Bellcore TA-NWT-000170.

Uneven Allocation

When the unit is configured for uneven bus allocation, X-bus time slots are reserved for the T1 interface only when a cross-connection is made to a time slot on that interface. This time slot may be reserved anywhere within the frame depending on availability. As a result, extra buffering of data is required on the module and the transfer delay is increased. Using uneven allocation provides a more efficient use of X-bus time slots since time slots are only reserved as required, and a full T1 link uses only 24 time slots (or 25 if signalling is enabled) instead of the 32 required for even allocation. If the T1 interface is configured for G.802 operation, an additional time slot is reserved on the back plane so that the framing bit may also be cross-connected.

6.13.2.3 Synchronization

The GMM unit receives two extracted T1 clocks from the T1 module, and creates a 1536kHz rate. Under NMS control, either or both of these 1536kHz clocks may be placed onto the back plane synchronization busses, from where the SXU may use them as a system reference clock. Should a LOS (Loss of Signal), OOF (Out of Frame) or AIS (Alarm Indication Signal) defect occur on the selected interface on the T1 interface module, then the clock is no longer provided to the GMM.

6.13.2.4 Data Link Usage

When the GMM is operating in ESF mode, the data link may be configured for four different types of operation. If the data link is not configured for any specific communication, standard background tasks such as yellow alarm generation and detection are maintained.

T1.403

The data link supports communications requirements as per ANSI T1.403 (1989). This specification provides point-to-point communications between two T1 framing points. It provides details of transmission error events and general performance details of the trunk connecting the two points. In the event of an error condition, e.g. frame error, the GMM transmits alarm information, via the T1 interface module on the GDM298, to the far-end as required by the specifications. Reports generated every one second provide general performance-related statistics for the trunk.

A bit-oriented protocol is used to carry error event details and command/response messages. A message-oriented protocol (ITU-T recommendations Q.921 (LAPD)) is used to carry the one second reports. The unit responds to commands received on the data link for loop back enable and disable for both line and payload loop back. These loop backs are implemented in the framers on the T1 module and are not under the control of the NMS.

TR 56014

The data link may be configured via the NMS to support requirements of AT&T TR54016 (Sept. 1989). This specification outlines ESF requirements at the interface for an AT&T DS1 line. The data link uses a simplified X.25 structure for its messages.

The GMM maintains 15-minute and rolling 24-hour performance data on its two T1 interfaces. This data may be requested from the unit over the data link for each 15-minute interval in a 24-hour period, as well as the total data for the previous 24-hour period. Data for ES (Errored Seconds), UAS (Unavailable Errored Seconds), SES (Severely Errored Seconds), BES (Bursty Errored Seconds) and LOFC (Loss of Frame Counts) is maintained. Again, line and payload loop backs may also be enabled/disabled on the interface via the data link.

Both T1.403 and TR56014

The data link may be configured to support both T1.403 and TR56014 as described above.

DXX HDLC Channel

The DXX HDLC channel may also be inserted into the ESF data link. This control channel is used to connect the DXX NMS control between the nodes.

6.13.2.5 G.802

The CCITT recommendation G.802 outlines mechanisms which allow different trunk formats to be interworked. In particular, G.802 describes how a 1.544Mbit/s trunk may be carried transparently over an E1 network before being reconnected to another T1 trunk. All information, data, signalling, framing, etc. is carried through the network without change.

T1 channels 1 to 15 are connected to E1 timeslots 1 to 15. T1 channels 16 to 24 are connected to E1 time slots 17 to 25. The F-bit (in the case of framed T1 signals) or the extra data bit (for unframed T1) is carried in the most significant bit of TS 26. The free E1 time slots may be used for other purposes.

If a T1 interface is configured for G.802 mode, the whole interface (including the framing) must be connected to an E1 interface as described above. On the transmit side, the framer will take framing from the PCM trunk rather than regenerating it. In ESF mode the data link and CRC bits are also taken from the trunk.

The interface carries out alarm handling and consequent actions while in G.802 mode. This may mean that in some cases, the framing and data are not passed through transparently.

6.13.2.6 1+1 Protection

Each of the T1 interfaces supported by the GMM may be protected by the other interface on the same interface module. When the protection feature is used, all of the settings on the two interfaces, with the exceptions of line-code and line-build-out, are made identical. This is controlled by the unit software which copies all of the settings from the protected interface to the protecting interface when 1 + 1 is selected. As the line code setting is not copied by the unit software, it should be ensured that both interfaces have a non-corruptive line code if data is to be transmitted.

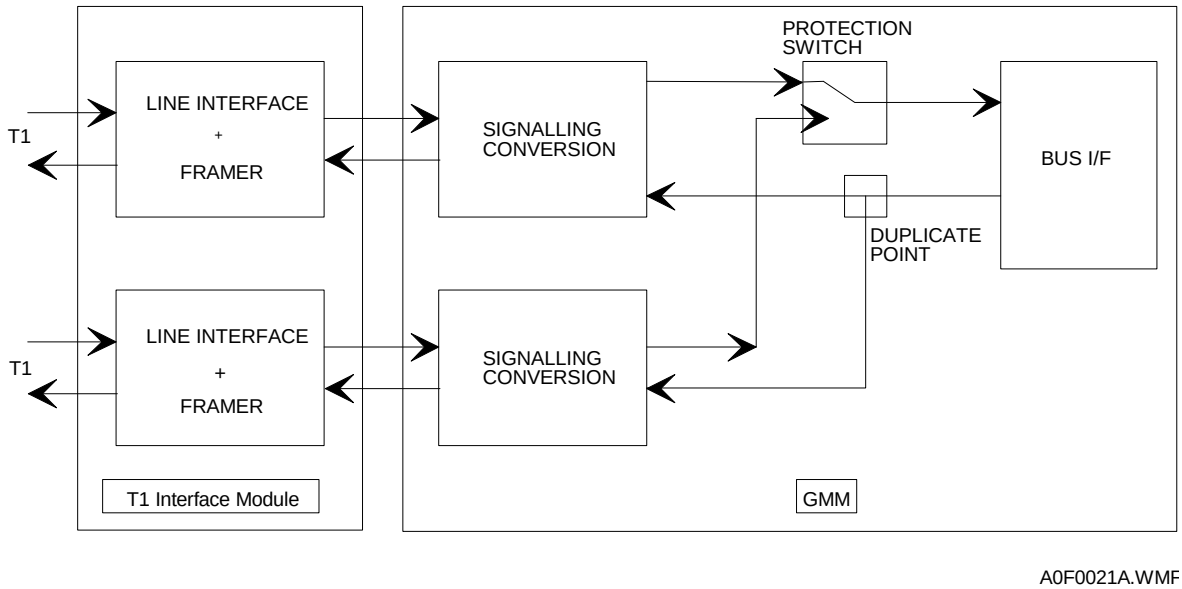


Fig. 109: Block Diagram of Protection Function

A unit operating in protected mode appears as a single port to the switch transmitting the same data to both interfaces on the unit. On the receive side, either of the received streams may be selected by protection switch, the selection being governed by the alarm status of the interfaces.

Receive alarm faults are divided into several categories (1, 2, 3, 4 and 5) depending on the seriousness of the fault. Examples of faults in these categories are:

Level 5	No fault
Level 3	Loop
Level 1	Red alarms, e.g. LOS

There are three operating modes for the protection switch:

Normal Operation

In normal operating mode, the protection switch will automatically switch to the other interface if the receive signal fault category of the active interface is continuously worse than the fault category of the other interface for a longer period than the given time delay. No switch-over will occur if the fault category is equal for both interfaces.

Preferred Operation

In preferred operating mode, switch-over to the better interface occurs if there is a difference between the interface fault categories. In a situation where fault categories are equal on both interfaces, the switch selects the preferred interface.

Forced Operation

In forced operating mode, the switch is forced to switch-over without delay. Received data is immediately connected to the X-bus. In this situation, the Protection switch forced fault message with status MEI appears and the red LED is turned on.

A switch operating time-delay is defined for preferred and normal operating modes. This delay is defined as n x 10 ms where n = 0…6000. The delay defines the allowed fault duration before the switch is triggered to switch-over.

Fault and Service Status (PMS, DMA, MEI, S) in 1+1 Mode

In principle, both interfaces generate their own alarms. PMA and S status are processed as follows.

PMA Status Processing

In protection mode, normal PMA status is changed to DMA status, and there is an additional fault condition, Loss of Protected Signal, with a PMA status. In normal or preferred operating modes, this condition is created when both interfaces have a fault category 3 or worse. In forced operating mode, this condition occurs if the forced interface has a category 3 or worse. The inactive interface is unable to generate a fault with PMA status.

S Status Processing

In protected mode, an S status alarm is generated only in the Loss of Protected Signal fault condition.

Yellow Alarm in 1+1 Mode

A yellow alarm is transmitted upstream from both T1 interfaces when a fault condition has been detected on the receive line of the active interface. Again, the implementation of the yellow alarm condition depends on the framing mode.

6.13.2.7 Loop Backs in GMM Unit

Four types of loop back may be implemented via the NMS on the T1 interfaces of the GMM unit. Physically, two of these loop backs are implemented on the GMM base unit and two are implemented on the T1 interface module. Of the two loop backs implemented on the GMM, one loops the signal to the line and the other loops the signal to the switch. Similarly on the T1 interface module, one of the loop backs loops the signal to the line and the other loops the signal to the switch. A programmable time-out is available on the unit to limit the duration of a loop back.

Two other types of loop back are configurable under the control of the T1.403 and TR 54016 data links. These loop backs, called line and payload loop backs, are implemented in the PCM framers on the T1 interface module.

When a loop back is enabled via the NMS, the yellow alarm LED on the unit is turned on and a MEI and service alarm generated. The alarm lasts for the duration of the loop back only. The SXU will not accept a looped interface as a synchronization source.

Equipment Loop Back

During equipment loop back, data from the switch is looped back towards the switch on the GMM unit. The HDLC data link is not looped backed during equipment loop back. The loop back is situated after the X-bus interface circuitry on the GMM but before the framing circuitry on the T1 interface module. Equipment loop back may be used to test the signalling conversion circuitry if CAS signalling connections are made to the unit. AIS is transmitted to the line during equipment loop back.

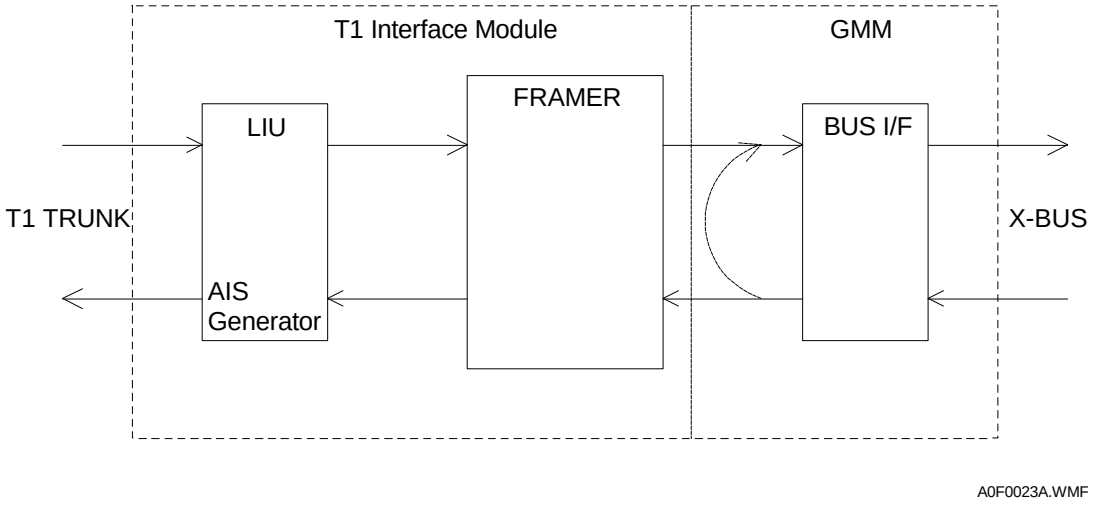


Fig. 110: Equipment Loop Back

Remote Line Loop

The remote line loop back is implemented in the X-bus interface circuitry of the GMM base unit. The loop is initiated by the far-end unit via the NMS control channel. During remote line loop back, the local clock is used to transmit the payload data and framing is regenerated. While this type of loop back is active, AIS is transmitted towards the switch, the PCM framer is disabled from transmitting idle patterns on unconnected channels, and the HDLC data link operates as normal.

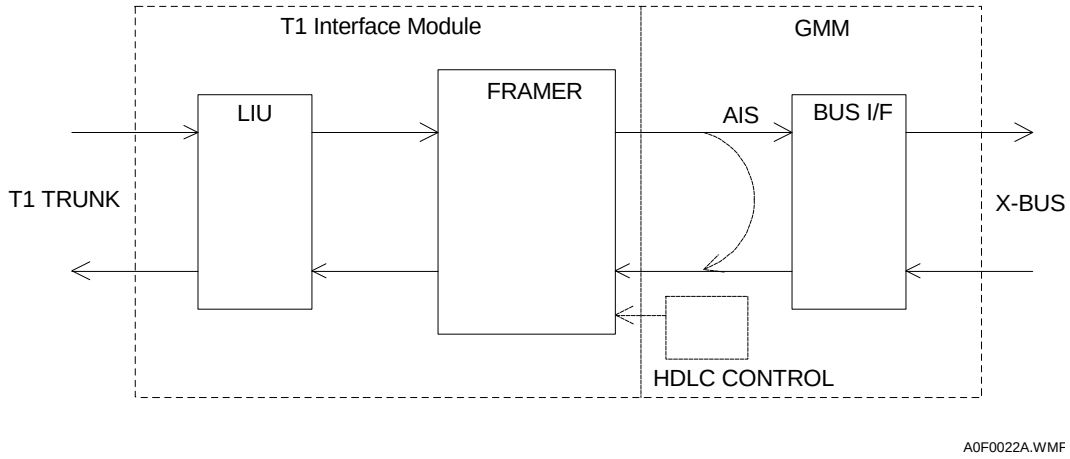


Fig. 111: Remote Line Loop Back

Interface Loop

During interface loop back, the line interface unit on the T1 module is configured for local loop back. This causes the receive data inputs to be disconnected; instead, the transmit outputs are routed back to the receive inputs. During this type of loop back, the line interface unit is also configured to transmit AIS to the line. If signalling is enabled on any channel, the BER tests during an interface loop back condition should be carried out on 56-kbit/s channels only.

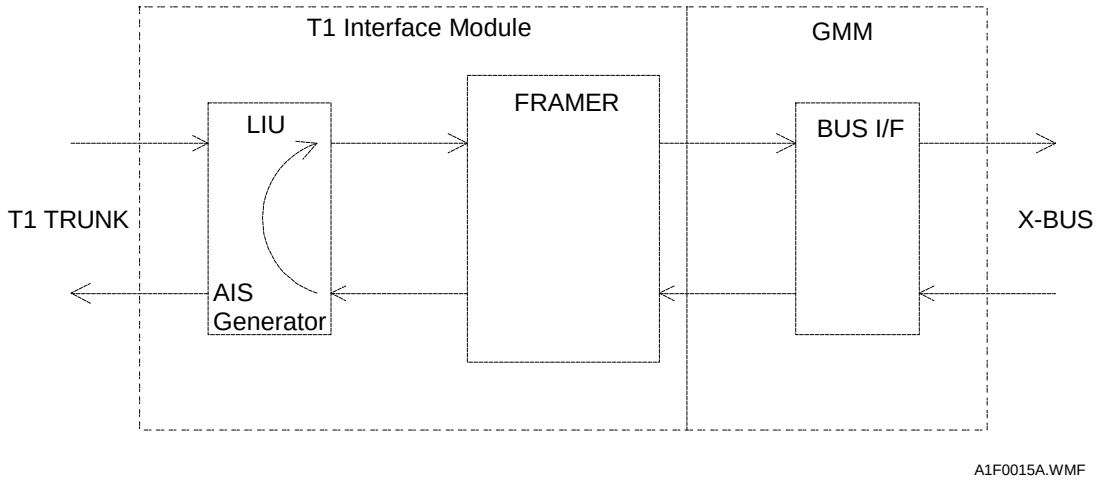


Fig. 112: Interface Loop Back

Line Loop

During line loop back, the line interface unit on the T1 module is configured for remote loop back. This causes it to ignore its transmit data and clock inputs, and loop the receive data outputs back through the transmit circuits and onto the transmit data outputs. AIS is transmitted to the switch from the framing circuit on the interface module during this type of loop back.

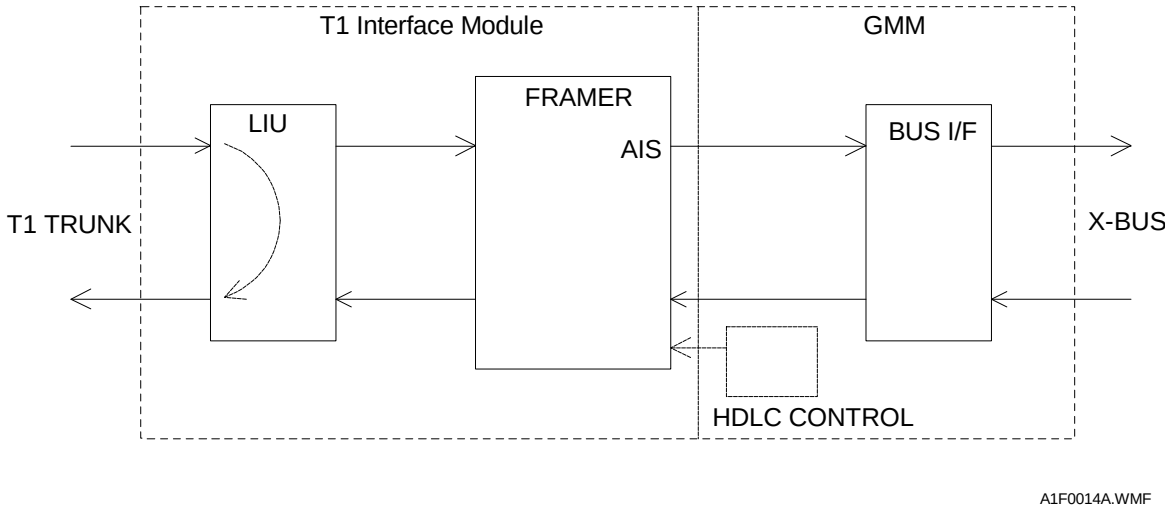


Fig. 113: Line Loop Back

ESF/CSU Loopbacks

When the ESF data link is configured for CSU operation via the NMS, the unit may be configured via the data link to enable a line loop back or a payload loop back. Both of these loop backs are physically located in the PCM framer on the T1 module. The loop backs themselves are not configurable from the NMS but are turned on by an appropriate message in the data link channel. The loop back remains on until a subsequent command, turning the loopback off, is received on the data link. AIS is transmitted to the switch during CSU loop back.

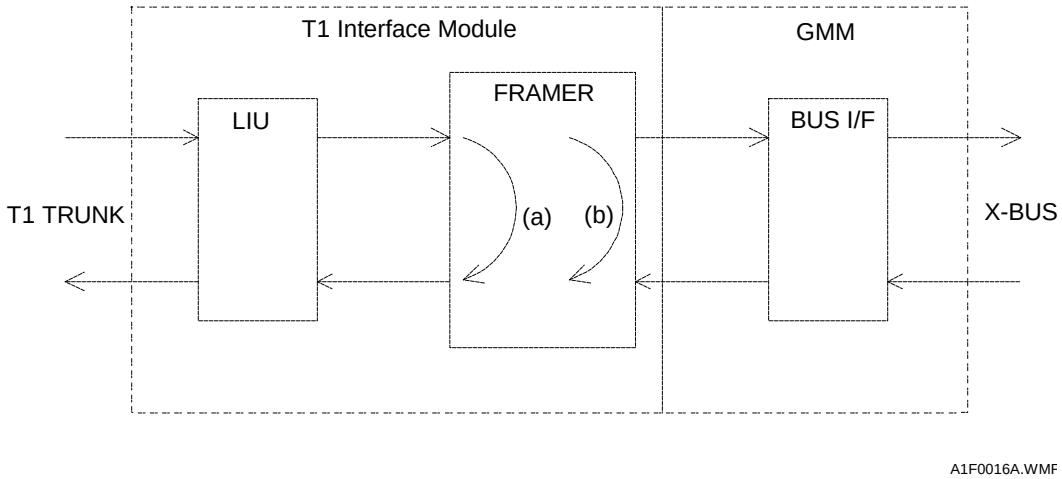


Fig. 114: CSU Loop Backs - a) Line and b) Payload

6.13.2.8 Performance Monitoring

Performance monitoring for T1 equipment is described principally by Bellcore TR-NWT-000820. This document defines the performance primitives and derived performance parameters for DS1 (T1) rates. The GMM monitors performance in accordance with this standard. Exceptions are outlined in Section .

T1 equipment in customer premises must also conform to AT&T TR54016 and ANSI T1.403. Support for these standards is provided by the GMM, with some exceptions noted under CSU Conformance.

In the first release of this product, there is no support for accessing the TR820 performance data directly from the NMS. Instead, the data is mapped to the G.821 equivalent and made available for display to the user in this format, using a mapping as defined below. This display format is the same as that used for the GMH and other E1/CEPT interface modules. Other TR820 performance data are mapped to the standard DXX Error Counters format, and can be accessed via the common Error Counters dialog. The mapping of TR820 statistics to G.821 statistics is shown in under Mapping TR820 Performance Data to G821.

TR820 Conformance

The GMM unit is compliant with Bellcore TR-NWT-000820 with the following exceptions:

- Several requirements relate to the ability to access certain data. Because the DXX NMS does not provide any direct interface to the TR820 function, other than via mappings from G.821 and Error Counters, many of these requirements cannot be met. These include:
  - The Invalid data flags (R3-10) are not visible to the user.
  - The 15-minute intervals should be aligned with the hour (R3-12) and the 24-hour intervals aligned with the day (i.e. at midnight, by default), but configurable to the start of any hour (R3-16). This feature is implemented but is not accessible via the DXX NMS.
  - Thresholds are provided but are not settable (R3-20).
  - The following counters, though maintained, are not visible to the NMS: ES-L, SES-L, SAS-P, PSD.
- Far-End Performance Monitoring (CR3-9) is not supported, with the exception that far-end CRC data is in fact reported via the G.821 and Error Counters if available.
- TCA (Threshold Crossing Alert) messages are not sent (R3-22). Instead faults are set and reported to the DXX NMS via the usual fault reporting mechanism.
- Protocols described in (R3-32) for communicating performance information to an OS are not supported (the DXX NMS protocols are the only ones supported). Scheduling of automatic performance reports (R3-34, R3-36, R3-37) is not supported.

Mapping TR820 Performance Data to G.821

The mapping of TR820 statistics to G.821 statistics is as follows:

G.821 Statistic	Description	TR820 Equivalent
ES	Errored Seconds	Same as ES-P except that CS do not contribute
SES	Severely Errored Seconds	Same as SES-P
DM	Degraded Minutes	No TR820 equivalent. Reported as 4 or more errors in a minute, where an error is a CRC error (ESF) or a FE (SF), or the occurance of a SEF or AIS defect
FSW	Framing Sync Word errors	FE
CRCE	Far-end CRC errors	Far-end CRC errors from CSU
PSC	Protection Switch Count	PSC
CV	Code Violations	CV-L
CRC	CRC errors	None in SF, CRC in ESF
FS	Frames lost	FC-P
BUFIN	Rx buffer slips	CS
BUFOUT	Tx buffer slips	None
RaiFlg	Used to count RAI seconds	RAIS

Mapping TR820 Performance Data to the Error Counters

The mapping of TR820 statistics to the DXX Error Counters is as follows:

Error Counter	TR820 Parameter
Frame loss count	FC-P
Errored Frame Words	FE
CRC block errors (near-end)	None in SF, CRC in ESF
CRC block errors (far-end)	Far end CRC errors from CSU
Buffer slips	CS
Code errors	CV-L

CSU Conformance

The CSU (Channel Service Unit), as implemented in the GMM unit, supports both AT&T TR54016 and ANSI T1.403[1] requirements for T1 equipment in customer premises.

The implementation of the CSU module is referred to as passive CSU. This means that requests to far-end CSU entities are not generated from the CSU module resident in the GMM unit. Thus, from a far-end perspective, the local CSU entity interprets TR54016 and T1-403 messages (BOP and MOP formats) and generates suitable responses where applicable. The CSU module also supports the generation of ANSI T1-403 One-Second Performance Report. Far-end statistics received by the CSU module are stored locally but are not available through the DXX NMS. The exception to this is that far-end CRC data is available via the G821 and Error Counters when CSU is enabled.

1 ANSI T1.403 specification is supported in ESF mode only.

6.13.3 Interface Module for GMM Interface Unit

6.13.3.1 General

The Interface Module used for GMM Interface Unit is GDM T1.

6.13.4 Faults and Actions

6.13.4.1 T1 Faults and Actions

Yellow Alarm

A yellow alarm is transmitted upstream from a T1 interface which has detected a fault condition on its receive line. The implementation of the yellow alarm condition depends on the framing mode.

Yellow Alarm in SF Framing Mode

There are two mechanisms for carrying yellow alarms on T1 trunks in SF mode. The most common method sets bit 2 in every channel to zero. The second method sets the F-bit in frame 12 (Fs bit) to a one. Both methods are supported by the GMM 253 unit via the NMS. Yellow alarm insertion is performed by the framer circuit on the T1 module.

Yellow Alarm in ESF Framing Mode

In ESF mode, the yellow alarm is carried in the ESF data link using a repetitive 'eight zeros - eight ones' pattern. If a far-end alarm occurs when the ESF data link is configured to carry the NMS control channel, the consequent yellow alarm overwrites the data link information. The NMS control channel is restored when the yellow alarm is cleared.

Trunk Conditioning

Trunk conditioning, per Bellcore requirements TR-NWT-000170, defines how consequent actions are handled in T1 networks. When an alarm condition is detected at a T1 interface, trunk conditioning occurs. During trunk conditioning, a trouble-word is inserted into each channel in the downstream path and a signalling trouble word is inserted into the signalling bits of each downstream channel. After 2.5 seconds, the signalling trouble word is replaced by a trouble-prime-word. All trouble words are configurable from the NMS. Should the downstream connection be to an E1 time slot, all trouble words should be set to 'all ones' via the NMS.

Consequent actions are configurable on a per-channel basis via the NMS. They may be carried on data only, on data and signalling, or they may be disabled entirely.

Signalling Freezing

Should a red alarm condition occur, then the signalling bits transmitted downstream are maintained in the state which existed before the alarm. This is known as Signalling Freezing, defined in TR-NWT-000170. The signalling state will not change until the alarm is cleared or trunk conditioning takes place. If consequent actions are set to Data and Signalling for a given channel, trouble word insertion on that channel occurs as described above.

Fault Masks

All interface alarms reporting on the GMM unit may be disabled on a per-interface basis via the NMS. If fault masking is on, then no faults are reported for that interface. Instead a Fault Masked alarm is generated. It is also possible to individually mask the AIS, yellow or BER alarms.

6.13.4.2 GMM Faults and Actions

The following acronyms will be used in the tables below:

Block number 0 = common faults, e.g. faults affecting the base unit or the protected interface
Block number 1,2 = interface 1 or 2
PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Affecting Fault
R = Red alarm LED
Y = Yellow alarm LED
RxAIS = AIS to the switch
TC = trunk conditioning (on a per-channel basis)
TxAIS = AIS to the line
Yellow = yellow alarm (RAI, FrFEA) to the line

Tx Signal Faults

Fault Condition	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
bus sync fault	0	PMA	S	Y	-	TxAIS	
missing IA activity	1, 2	PMA	S	R	-	TxAIS	

Rx Signal Faults

Signal and Frame Faults	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
missing module	1, 2	PMA	S	R	RxAIS	-	[a]
conflict in module type	1, 2	PMA	S	R	RxAIS	-	
HW fault in module	1, 2	PMA	S	R	-	-	[a]
no response to NNM messages	1, 2	PMA	S	R	RxAIS	-	
own NNM message received	1, 2	PMA	S	R	RxAIS	-	
wrong IDs in NNM message	1, 2	PMA	S	R	RxAIS	-	
loss of input signal (LOS)	1, 2	PMA	S	R	TC	Yellow	[b]
loss of input signal (LOS)	1, 2	DMA	S	R	TC	Yellow	[b]
loss of input signal (LOS)	1, 2	MEI	S	R	TC	Yellow	[b]
loss of frame on input signal (LOF)	1, 2	PMA	S	R	TC	Yellow	[b]
loss of frame on input signal (LOF)	1, 2	DMA	S	R	TC	Yellow	[b]
loss of frame on input signal (LOF)	1, 2	MEI	S	R	TC	Yellow	[b]
AIS on input signal	1, 2	PMA	S	Y	TC	Yellow	[b]
AIS on input signal	1, 2	DMA	S	Y	TC	Yellow	[b]
AIS on input signal	1, 2	MEI	S	Y	TC	Yellow	[b]
BER 10^{-3}	1, 2	MEI	-	Y	-	-	

a Fault is not implemented in the initial software releases. Check current releases for further information.

b The PCM faults (LOS, LOF, AIS and Yellow) are of configurable severity, hence their appearance three times in the fault table.

Far-End Alarms	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
yellow alarm (aka RAI, FrFEA)	1, 2	PMA	S	Y	TC	-	a
yellow alarm (aka RAI, FrFEA)	1, 2	DMA	S	Y	TC	-	a
yellow alarm (aka RAI, FrFEA)	1, 2	MEI	S	Y	TC	-	a

a Fault is not implemented in the initial software releases. Check current releases for further information.

Loops	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
interface loop back	1, 2	MEI	S	Y	-	TxAIS	
equipment loop back	1, 2	MEI	S	Y	-	TxAIS	
line loop back	1, 2	MEI	S	Y	RxAIS	-	
line loop back made by neighbour	1, 2	MEI	S	Y	RxAIS	-	
remote line loop back	1, 2	MEI	S	Y	-	-	
CSU line loop back	1, 2	MEI	S	Y	RxAIS	-	
payload loop back	1, 2	MEI	S	Y	RxAIS	-	

Common Logic Faults

Fault Condition	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
unpredicted fault	0,1,2	PMA	-	R	-	-	
reset	0	PMA	S	R	-	-	
power supply faults: +5V in subrack +5V in unit +12V in unit -10V in unit	 0 0 0 0	 PMA PMA PMA PMA	 - - - -	 R R R R	 - - - -	 - - - -	
start permission denied by SXU	0	PMA	S	R	-	TxAIS	a
RAM fault	0	PMA	S	R	-	-	
EPROM fault	0	PMA	S	R	-	-	
flash write error	0	PMA	-	R	-	-	
flash copy error	0	PMA	-	R	-	-	
flash erase error	0	PMA	-	R	-	-	
flash duplicate error	0	PMA	-	R	-	-	
flash shadow error	0	PMA	-	R	-	-	
flash checksum error	0	PMA	S	R	-	-	
missing settings	0	PMA	S	R	-	-	
EEPROM fault	0	PMA	S	R	-	-	
checksum error in downloaded SW	0	PMA	-	R	-	-	
SW in flash incompatible with EPROM	0	PMA	-	R	-	-	
HW fault in base unit	0	PMA	S	R	-	-	b

a Consequent action is not implemented in the initial software releases. Check current release notes for further information.

b Fault is not implemented in the initial software releases. Check current releases for further information.

1+1 Protection Switch Faults

Fault Conditions	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
loss of protected signal	0	PMA	S	R	-	-	[a]
protection switch forced	0	MEI	-	R	-	-	

a Signal actions depend on actions of the protected interfaces.

Miscellaneous Faults

Fault Condition	Block	Status	Svc	LED	Rx Signal	Tx Signal	Note
HDLC overlap with X-bus	1, 2	DMA		R	-	-	
fault masked/test	1, 2	MEI	S	Y	-	-	
G821 unavailable state	0,1,2	PMA	S	-	-	-	
G821 performance event	0,1,2	DMA	-	-	-	-	
TR820 unavailable state	1, 2	PMA	S	-	-	-	
TR820 performance event	1, 2	DMA	-	-	-	-	

6.13.5 Technical Specifications

Alarms

Alarms are detected in accordance with Bellcore TR-NWT-000170.

Loss of Signal

A LOS (Loss of Signal) defect is deemed to have occurred if 175 ± 75 consecutive zeros are detected on the receive T1 stream. Should the LOS defect remain present for 2.5 seconds, then the LOS alarm is declared. The LOS defect must be absent for 15 seconds before the LOS alarm is cleared.

Loss Of Frame

An OOF (Out of Frame) defect is deemed to have occurred if 2 out of 5 frame bits are in error. If the OOF defect remains for 2.5 seconds, then a LOF (Loss of Frame) alarm is declared. The LOF alarm is cleared when valid framing has been present for 15 seconds.

AIS (Blue Alarm)

If an 'all ones' pattern is received for 2.5 seconds, an AIS alarm is generated. This alarm may be detected in the presence of 10^{-3} bit errors. To clear the alarm, AIS must be absent at the interface for 15 seconds.

Yellow Alarm

Should a yellow alarm detected at the interface be present for 0.5 seconds, then a yellow alarm is declared. This alarm is cleared when the yellow alarm has been absent for 0.5 seconds.

Transfer Delays

When the GMM 253 is located in a Basic Node and its T1 interfaces are configured for even allocation, the transfer delay complies with Bellcore TR-NWT-000170.

Mean delay	< 0.5ms
Maximum delay	< 0.7ms

Mechanics

Weight	620 g
Dimensions	25 x 160 x 233 mm

Power from Battery

GMM unit + T1 interface module	5W

6.14 GMU and GMU-M SDH Interface Unit

6.14.1 General

GMU is an STM-1 interface unit for DXX Cluster Nodes and Basic Nodes. Its main function is to adapt the n x 64 kbit/s signals of the DXX node's cross-connect bus (X-Bus) into STM-1 or S34M frames using VC-12 and VC-2 containers. GMU-M is an STM-1 interface unit for DXX Basic and Midi Nodes.

GMU and GMU-M can also be used as spare parts of each other as shown in the following table:

Node and Control Unit	Recommended Unit	Other supported SDH Units	Spare Unit
Mini Node with XCG unit[a]	GMU-M	GMU	GMU-M or GMU
Basic Node with SCU unit[b]	GMU-M	GMU	GMU-M or GMU
Basic Node with SCU and HDLC-4CH (SCP) module	GMU-M	GMU	GMU-M or GMU
Cluster Node slave with SCU unit[b]	GMU	-	GMU
Cluster Node slave with SCU unit and HDLC-4CH (SCP) module	GMU	-	GMU

a XCG unit software version must be 2.1 or newer.

b GMU unit software version must be 1.4 or newer and there can only be one GMU or GMU-M in the inventory without HDLC-4CH (SCP) module, SCU unit software must be 8.4 or newer.

GMU and GMU-M consist of a base unit and two changeable interface modules. STM-1 electrical and optical modules and S34M electrical modules are provided. The S34M interface is synchronous and has a frame according to G.832[2]. GMU and GMU-M provide a SEC clock generator with accuracy and holdover characteristics as defined in G.81s.

GMU and GMU-M operate in terminal multiplexer, in terminal multiplexer 1+1 or in add-drop-multiplexer modes. One or two synchronous port modules can be equipped depending on the operating mode. In the add-drop-multiplexer mode GMU and GMU-M provide cross-connection of VC-12 and VC-2 allowing rearrangement of passing through virtual containers.

Network protection initially includes Multiplex Section 1+1 and lower-order Subnetwork Connection protection (SNCP).

GMU and GMU-M terminate the STM-1 Section Overhead (SOH) and the VC-4 trail. Most SOH and VC-4 Path Overhead channels can be cross connected in the DXX Basic Node's 64 kbit/s matrix and accessed via DXX interface units. GMU and GMU-M can terminate up to 32 VC-12 or 10 VC-2. Higher capacity containers can be created by VC-2 virtual concatenation.

Fig. 115 shows GMU or GMU-M with two synchronous ports in a Basic Node. DXX Interface units (IFU) collect n x 64 kbit/s and ATM traffic into GMU via the X-Bus. Control unit (SCU) communicates via the node control bus (VTP) to GMU. DC power supply in the GMU produces voltages from the battery supply.

2 For the valid date of any ITU-T/CCITT Recommendation please refer to Section Relevant Recommendations.

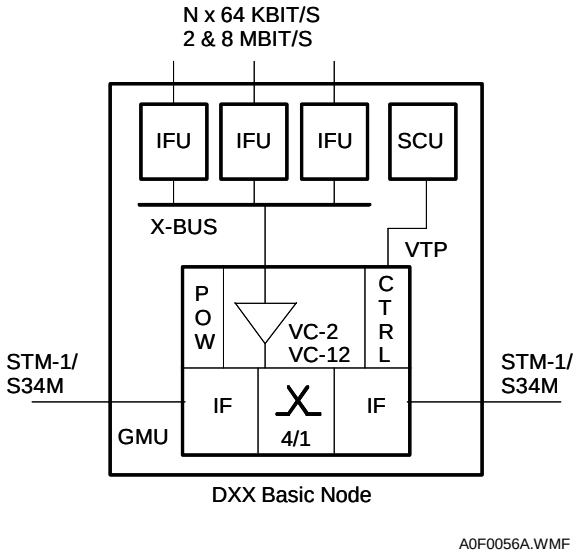


Fig. 115: GMU/GMU-M provide STM-1 or S34M ports for the DXX Node

6.14.1.1 GMU and GMU-M Mechanical Design

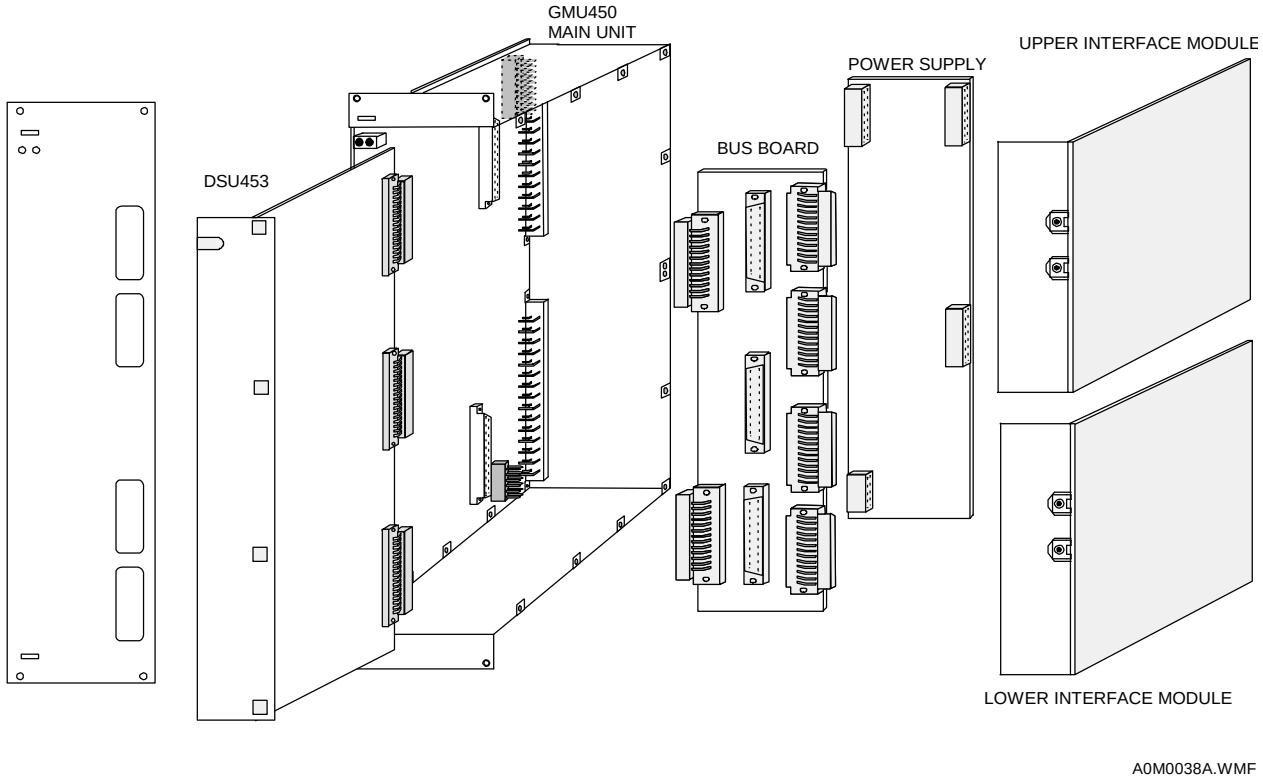


Fig. 116: Mechanical Structure of GMU and GMU-M

6.14.2 Operation

6.14.2.1 GMU and GMU-M Unit Functional Structure

GMU and GMU-M units consist of the GMU or GMU-M assembly, one or two interface modules and a power supply module.

GMU assembly consists of the following modules

Module Code	Function	Pcs. / GMU
GMU 450	GMU base unit	1
DSU 453	STM-1 interface base unit	1
RMU469	GMU Internal Bus Board	1
GMZ 460	GMU main processor program	1
GMZ 461	GMU ASIC processor program	1

GMU-M assembly consists of the following modules

Module Code	Function	Pcs. / GMU-M
GMU 700	GMU-M base unit	1
DSU 453	STM-1 interface base unit	1
RMU 469	GMU Internal Bus Board	1
GMZ 546	GMU-M main processor program	1
GMZ 547	GMU-M ASIC processor program	1

NOTE!

You cannot download GMU unit software into GMU-M, or GMU-M unit software to the GMU unit. If a compatible unit software version is not found from the unit's Flash and EPROM memories, the unit will not operate.

GMU 450, GMU base unit for two interfaces, has the following main functional blocks:

— Two control processors and peripheral circuits
— Core program memories
— Application SW memories
— X-BUS interface
— VTP control bus interface

GMU 450 contains two microprocessors. Unit management functions and HDLC links are handled by the main processor. Real-time ASIC control is dedicated to the ASIC-processor.

For the System SW 128 kbytes of EPROM memory is allocated. The application SW, GMZ460 and GMZ461 in GMU unit and GMZ546 and GMZ547 in GMU-M units are downloaded into a FLASH memory of 512 kbytes. Also the GMU and GMU-M internal calibration settings, serial numers etc. are included here.

32 kbytes of EEPROM is reserved for functional settings, like cross-connections and NMS settings.

GMZ 460, GMU main processor program, and GMZ546, GMU-M main processor program, handle the general functions of the GMU unit including communication with NMS and with other DXX units via the VTP-bus.

GMZ461, GMU ASIC processor program, and GMZ547, GMU-M ASIC main processor program, handle the ASIC-interface functions autonomously. It communicates with the main processor via the VTP-bus.

DSU 453, STM-1 interface base unit, is the VC processing board. The functionality is mainly divided between 4 ASICs. The main blocks are:

— TU-pointer processor
— 4/1 cross-connection
— VC-2 and VC-12 termination
— X-Bus frame buffers
— SEC oscillator

The Overhead Termination and Pointer Processing at AU4 -level as well as termination of Section Overhead (SOH) and higher-order path overheads is performed in the OTP ASIC, which is situated in every interface module of the GMU. The 8-bit data between the OTP and LAC ASIC is transferred using the SEC oscillator as a clock.

The TU-pointer processing and 4/1 cross-connection is realised in the LAC ASIC. The main function of it is to cross-connect two STM-1 signals and two 32x2Mbit/s X-Bus signals. The X-BUS data is received from (or transmitted to) the LTT ASIC which transmits the signals in TU-12/TU-2 -frames.

Basically, the LTT ASIC is an SDH Access Framer. In the receiving direction it terminates the VC-2/VC-12 and in transmitting direction functions as a TU Pointer Generator. The DSU453 has two LTTs.

The XBI ASIC is an interface between the DXX 1/0 cross-connect bus and the LTT.

As a local oscillator the DSU453 has an SDH Equipment Clock (SEC) at a frequency of 19.44 MHz.

GMU450, DSU453 and interface modules are coupled together using the RMU469 Internal Bus Board.

From the 48VDC power feed the GMU and GMU-M power supply, the PDF452, generates operating voltages of 3.3V, 5V, 12V and -10V. A 24V version PDF458 is also available.

6.14.2.2 GMU and GMU-M Operating Modes

Terminal Multiplexer (TM)

In the Terminal Multiplexer mode GMU or GMU-M are equipped with one STM-1 or S34M port. TM mode can be used in point-to-point links and full STM-1 capacity can not be filled from a Basic Node. With S34M ports, the link capacity can be fully used.

Terminal Multiplexer with 1+1 protection (TM1+1)

In the Terminal Multiplexer 1+1 mode GMU or GMU-M are equipped with two STM-1 or S34M ports for Multiplex Section 1+1 line protection. The same VC-4 is transmitted to both STM-1 ports. In receive direction the better VC-4 is selected. With S34M link, VC-12s are copied to both ports.

Add-Drop-Multiplexer (ADM)

In the Add-Drop-Multiplexer mode GMU or GMU-M units are equipped with two STM-1 or S34M ports (east and west direction). Any of the VC-12 and VC-2 virtual containers in the STM-1 can be added/dropped to the X-BUS.

Fig. 117 and Fig. 118 show GMU and GMU-M functional models with the ETSI symbols in the three modes with STM-1 and S34M ports.

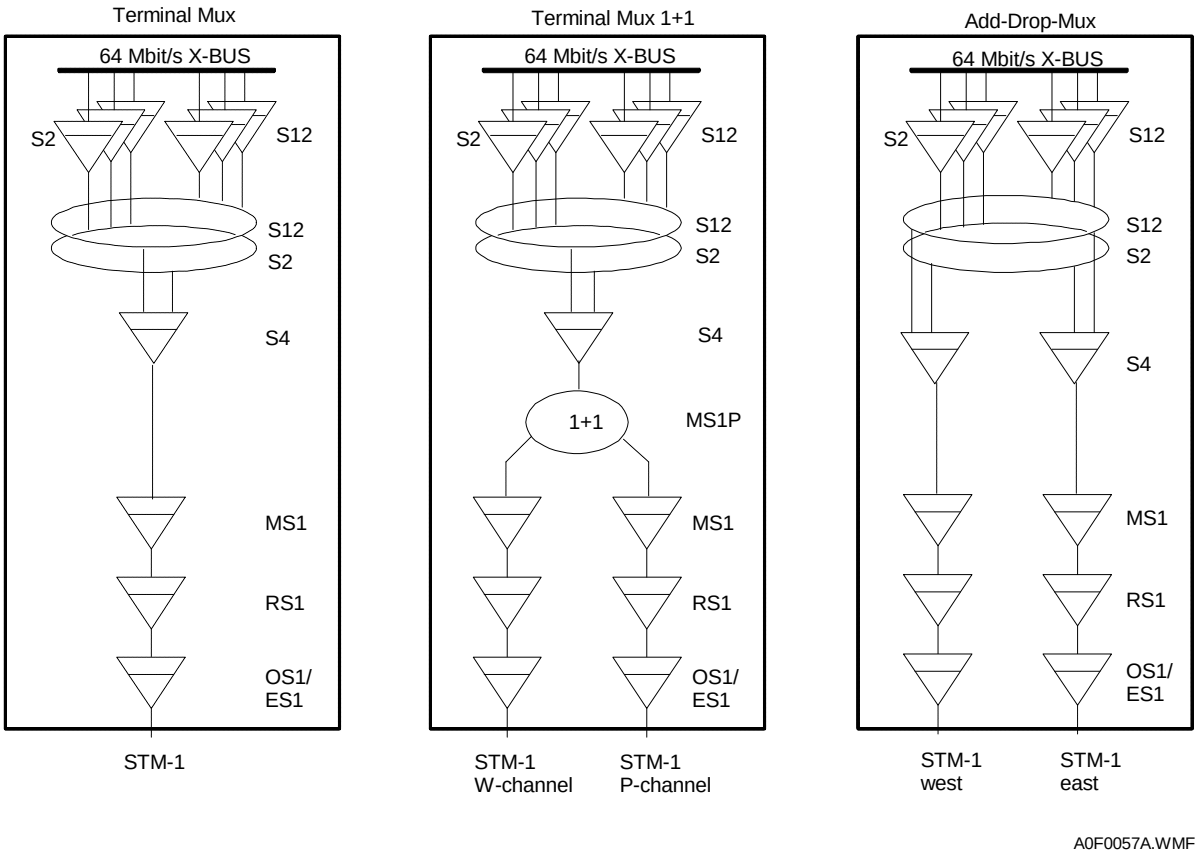


Fig. 117: GMU and GMU-M functional models in the three operating modes with STM-1 ports

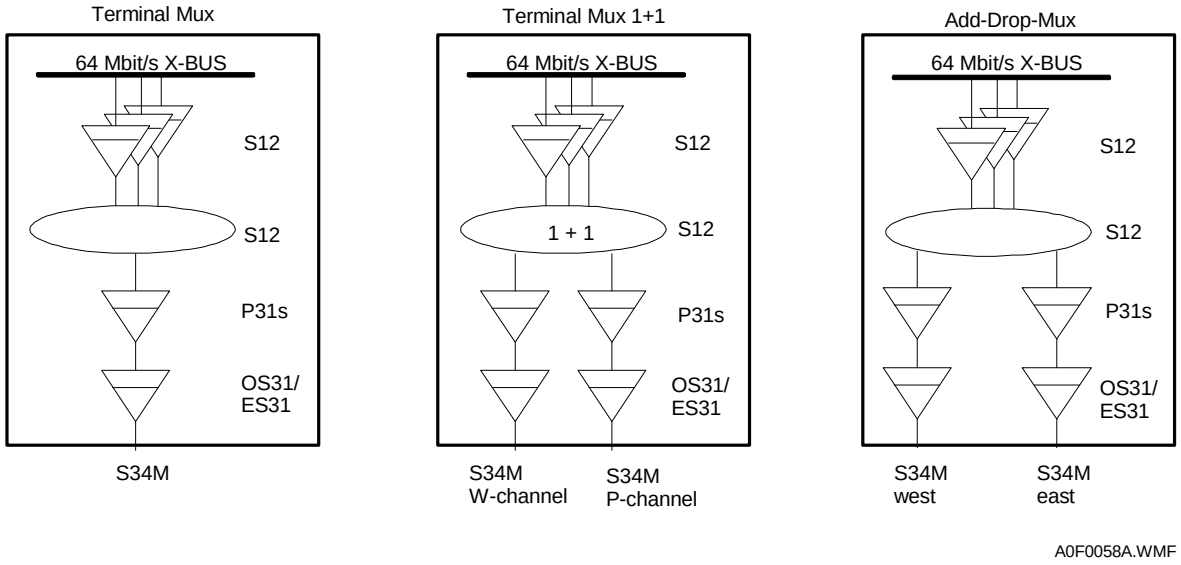


Fig. 118: GMU and GMU-M functional models in the three operating modes with S34M ports

6.14.2.3 GMU and GMU-M Capacity

GMU and GMU-M in the Basic or Midi Node

Half of the Basic or Midi Node capacity (64 Mbit/s) is usually used by trunks and half by tributaries. A Basic or Midi Node then can have up to 16 VC-12 or 5 VC-2 trunks corresponding to a total of about 32 Mbit/s. In order to fill the STM-1 capacity (63 VC-12), traffic is collected from several (four or more) Basic or Midi Nodes.

GMU in the Cluster Node

In a Cluster Node GMU can use the full capacity of the Slave Subrack (64 Mbit/s) and terminate up to 32 VC-12 or 10 VC-2 (if no other port units are furnished into the Slave Subrack). Two GMU ADMs are required to process the full STM-1. The GMUs are placed in separate Cluster Slave subracks and interconnected with an STM-1 electrical link. Fig. 119 shows a Cluster Node with two slave subracks containing GMUs and two Slave subracks with other IFUs. One of the STM-1 ports shown is optional and is used with network protection.

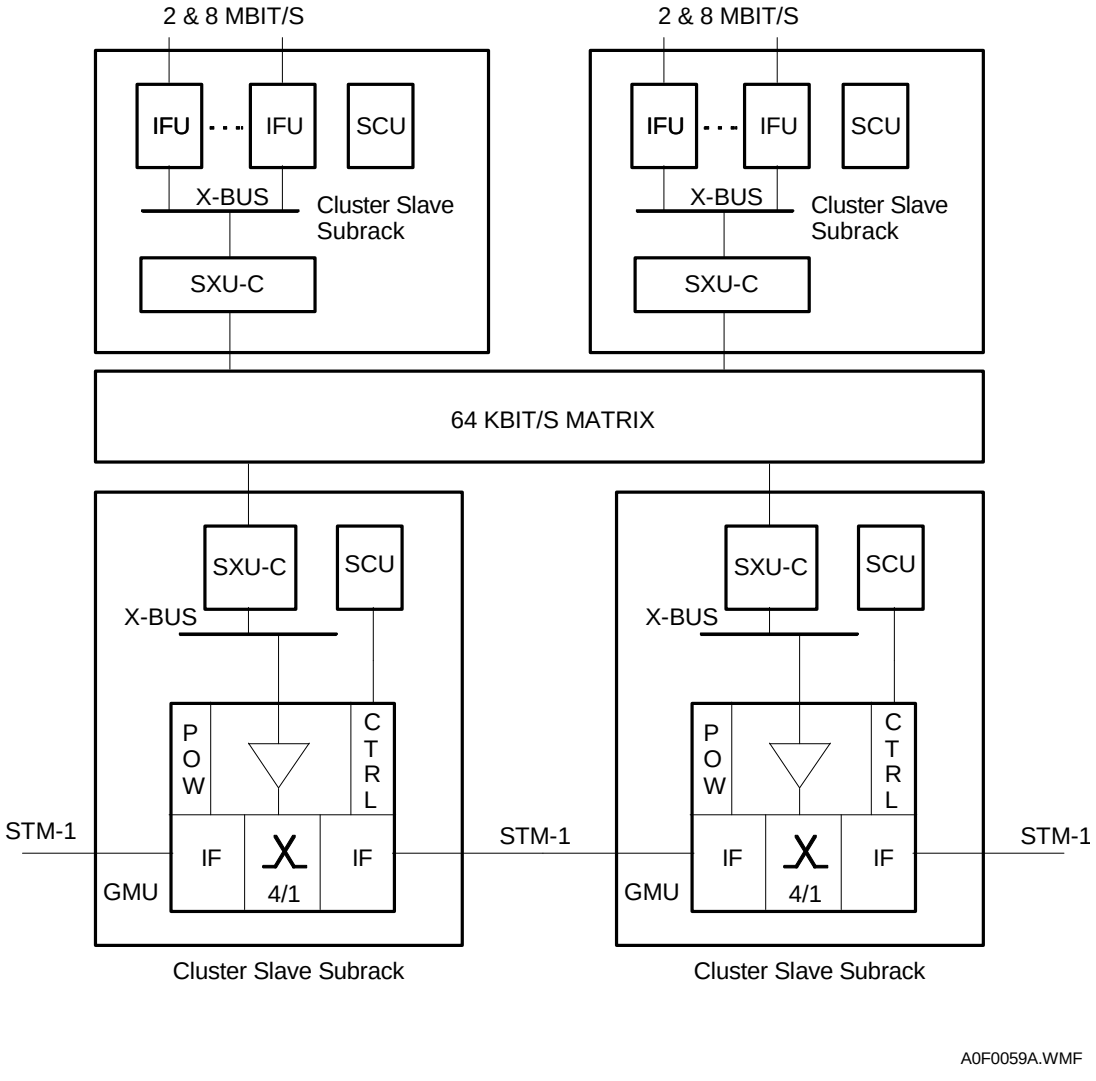


Fig. 119: Two GMUs in a Cluster Node

6.14.2.4 Mapping

DXX trunks

DXX trunk is a transparent link between two DXX nodes. The payload area of VC-12 and VC-2 is used for DXX trunks, to where the n x 64 kbit/s X-Bus signals are mapped.

Byte synchronous floating mapping used for VC-12 is similar to that defined in G.707 § 10.1.4.3 (Byte synchronous mapping of 31 x 64 kbit/s). For VC-2 a proprietary byte synchronous floating mapping, which is expanded from the VC-12 mapping, is used.

VC-12 User Access

GMU and GMU-M can interwork at VC-12 level with foreign equipment, which uses the appropriate VC-12 mapping; byte synchronous floating mapping without TS0 (G.704/G.706). Then the n x 64 kbit/s signals in TS1 to TS31 can be cross-connected in the DXX Node. Alternatively the VC-12 can have byte synchronous floating mapping with TS0, but then all 32 TS must be cross-connected transparently to a 2048 kbit/s port on a GMH unit.

6.14.2.5 Matrix

GMU and GMU-M contain a strictly non-blocking time-space cross connect matrix for VC-2 and VC-12. The matrix has capacity for the two STM-1 ports, the X-Bus port and a monitoring port. STM-1 timeslots for passing through VCs can be freely rearranged and timeslots for VCs terminated to the X-Bus can be freely selected. Uni- and bidirectional and multicast connections are possible.

6.14.2.6 Trail Termination

GMU and GMU-M can terminate 32 VC-12 or 10 VC-2 plus two VC-12 containers or any combination of these to the X-Bus. GMU and GMU-M always terminate the higher order VC-4. In total GMU and GMU-M contain 126 trail termination resources. The resources enable SNC/N protection monitoring. VC-12 and VC-2 share a termination resource pool. Every VC-2 termination reserves three termination functions. VC-12 with SNC/N protection also reserves three termination functions. VC-2 with SNC/N protection reserves nine termination functions.

6.14.2.7 X-Bus Ports

GMU and GMU-M's tributary interfaces are all directed to the node's internal X-Bus. The user selects a VC-12 or a VC-2 termination in the short buffer mode or in the long buffer mode. This creates X-Bus ports, to which cross-connections can be made. Additionally, two SOH and two VC-4 POH ports are implemented.

In the short buffer mode delay is minimized and only the TS-bytes can be used. X-Bus capacity is reserved for all TS, even if cross connections are not made. Unused timeslots are automatically filled with an all '0's pattern.

In the long buffer mode longer delay is allowed. X-BUS TS are not reserved until cross-connected. This allows bus overbooking with ports containing partly filled payloads.

One particular timeslot can carry Channel Associated Signalling (CAS) for 30 other timeslots, if enabled.

The VC-12 payload has 32 timeslots (TS0 to TS31) and two R-bytes (R0, R1). The VC-2 payload consists of 96 timeslots (TS0 to TS95) and ten R-bytes (R1A-R3A, R1B-R3B, R0C-R3C).

X-Bus ports in GMU and GMU-M

		Short buffer mode		Long buffer mode	
Port type	**Number of ports**	**Timeslots/port**	**Capacity/port, kbit/s**	**Timeslots/port**	**Capacity/port, kbit/s**
VC-2	10	96	6144	96+10	6784
VC-12	32	32	2048	32+2	2176
SOH	2	-	-	81	5184 [a]
POH	2	-	-	4	256 [a]

a Some of the capacity is reserved for the standardized use of SOH/POH

The total capacity cannot exceed the X-Bus capacity of 1043 timeslots in Basic or Midi Nodes and 1051 timeslots in a Cluster Nodes.

6.14.2.8 Virtual Concatenation

Virtual concatenation of VC-2 (VC-2-mc) is defined in G.707. In GMU and GMU-M VC-2-mc is used in order to increase trunk bandwidth to be able to transfer 8 448 kbit/s signals or to enhance trunk utilization. Several VC-2 containers are combined maintaining payload integrity. In the transport network VC-2 pointers are processed as for separate VC-2s. The VC-2s must be kept in a single VC-4 in order to limit delay spreading between the VC-2s. GMU and GMU-M allow delay spreading of up to 250 ms in the concatenated group. When SNC protection is used for VC-2-mc in the network, the VC-2s must be switched as a group. The allowed number of network nodes on the trail depends on the TU pointer processor delay variation in the nodes. This characteristic is not standardized and is vendor dependent.

Up to 10 VC-2s can be concatenated in a single group. The number of VC-2 groups can be up to 5. Additionally proprietary VC-12-mc concatenation is possible with up to 32 VC-12 in a group. The maximum number of VC-12 groups is 16.

6.14.2.9 Unused Containers

Unequipped signal (VC-UNEQ) is transmitted to unused VCs if the user does not activate a termination resource. VC-UNEQ can be transmitted to VC-2 and VC-12 for the full STM-1 capacity. VC-UNEQ has a valid pointer and parity. Otherwise signal content is zero.

6.14.2.10 Performance Monitoring

Performance monitoring (PM) is according to G.826. PM provides 15 minute and 24 hour values of Errored Seconds (ES), Severely Errored Seconds (SES) and Background Block Error (BBE) for near end and far end termination functions.

MS1, VC-4, VC-2 and VC-12 trail terminations have the following performance parameters. RS1 does not have the far end parameters.

N_ES	near end errored second
F_ES	far end errored second
N_SES	near end severely errored second
F_SES	far end severely errored second
N_BBE	near end background block errors
F_BBE	far end background block errors
UAS	unavailable seconds

The protected MS1 trail is similar to the MS1 trail.

Also the following performance parameters are monitored.

PJE	AU-4 pointer justification events
OFS	out of frame second
PSC	protection switch count
PSD	protection switch duration

OS1 trail termination has the following parameters:

— laser bias and transmit power level

6.14.2.11 Loops

An equipment loop (tx signal looped back to rx) can be activated for the aggregate STM-1 / S34M signal. A line loop can be activated for selected VC-12s and VC-2s.

6.14.2.12 Network and Line Protection

Protection modes defined in ETS 300 417-1-1, DTR/TM-3025 and DTR/TM-3042 are applied. Protection types and hardware implementations are described without details of APS protocols.

Protection modes

Protection type	Level	Characteristics
Linear multiplex section 1+1	STM1	Dual/Single-ended
Linear multiplex section 1+1	S34M	Single-ended
Subnetwork connection (SNC/N) 1+1	VC2, VC12	Single-ended
Subnetwork connection (SNC/I) 1+1	VC2, VC12	Single-ended

Multiplex Section (MS) 1+1 Protection

MS 1+1 protection can be used with STM-1 and S34M interfaces in point-to-point networks in Basic Nodes, Midi Nodes and Cluster Nodes. ADM with MS 1+1 is not supported. Single-ended and dual-ended switching in revertive and non-revertive modes can be selected. In single-ended mode a receiver in one end operates independently of the other end. In dual-ended mode the switch operation is co-ordinated in the two ends with the APS protocol. In revertive operation the default link is reselected after the fault clearance.

The VC-4 container is copied to both STM-1 ports. The protection switch operates on detection of loss of signal, loss of frame or Multiplex Section AIS within 50 ms. Also block errors (DEG defect from B2) affect the protection switch.

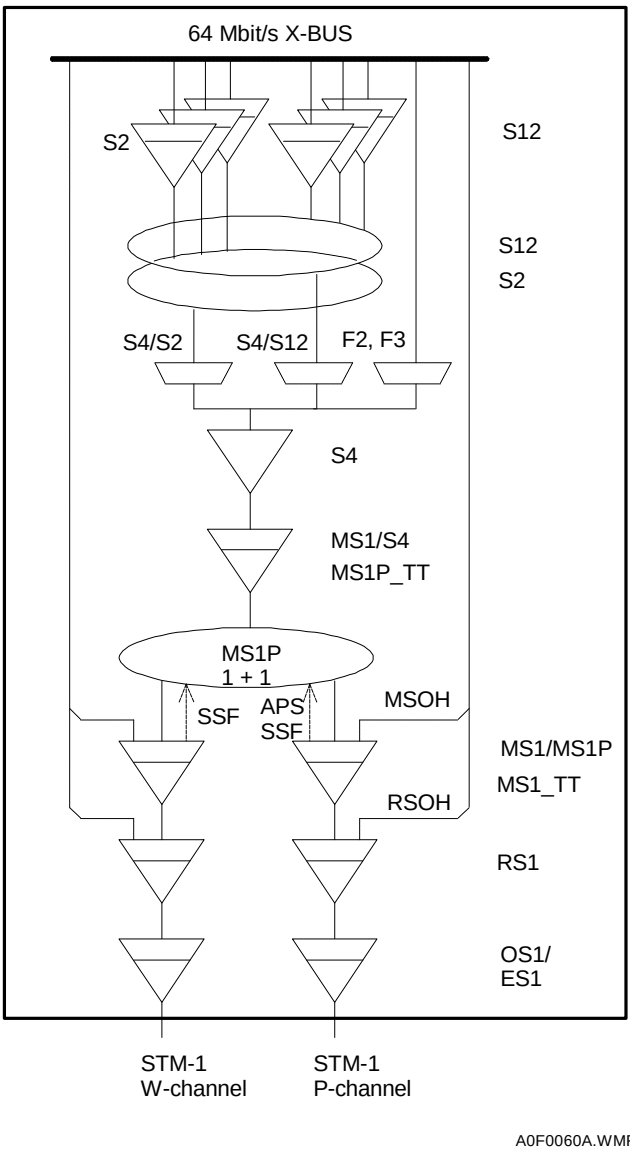


Fig. 120: MS 1+1 Detailed Functional Model

Subnetwork Connection/Non-intrusive Protection (SNC/N)

SNC/N 1+1 protection can be applied for VC-12 and VC-2. Any VCs from the two aggregate links can be selected as the protection pair. The number of protected VCs can be up to 10 VC-2 or 32 VC-12. Switch operation is single-ended. Revertive and non-revertive modes can be selected. SNC/N protection switch operates on VC-level defect and on block error defect criteria.

In the transmit direction the VC is broadcast to two ports. In the receive direction GMU and GMU-M use three termination resources for each protected VC to monitor the status of the two incoming VCs and to terminate the protected VC. A maximum of 96 terminations is consumed by 32 VC-12s with SNC/N. The protection switch operates within 50 ms in case of a single VC failure. A holdover time of 0 to 10 s can be set in steps of 100 ms.

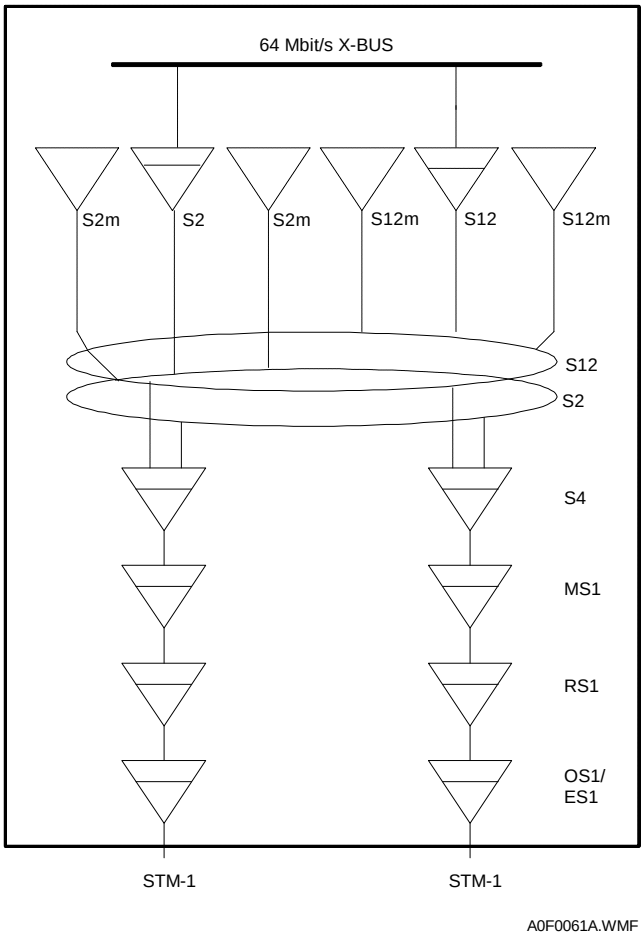


Fig. 121: SNC/N 1+1 in GMU adn GMU-M ADM

Subnetwork Connection Inherent 1+1 Protection (SNC/I)

SNC/I 1+1 protection is similar to the SNC/N protection except that the received VC is selected based on defects TU-AIS, loss of TU pointer and loss of TU-multiframe. The VC/POH is not monitored.

6.14.2.13 Synchronization

SDH networks are synchronized from a Primary Reference Clock (PRC, G.811) provided by the network operator. The reference clock is transferred in the SDH network with STM-N signals or distributed with a separate synchronization network.

DXX Node Clock is generated in the Basic Node's SXU or in the Cluster Node's CXU-M. In normal state the node clock is locked to a network reference and the GMU and GMU-M lock its STM-1 output frequency to the Node Clock. The synchronization signals between SXU/CXU-M and GMU and GMU-M are transferred in VC-4 POH / K3.

A fallback list of the following clock sources can be entered:

— STM-1/west in GMU and GMU-M
— STM-1/east in GMU and GMU-M
— Internal clock of GMU and GMU-M
— 2048 kbit/s (G.704) port in a GMH unit
— 2048 kHz (G.703) synchronization interface in SXU/CXU-M

Use of the 2048 kbit/s and 2048 kHz ports is restricted to high quality references as defined in G.813.

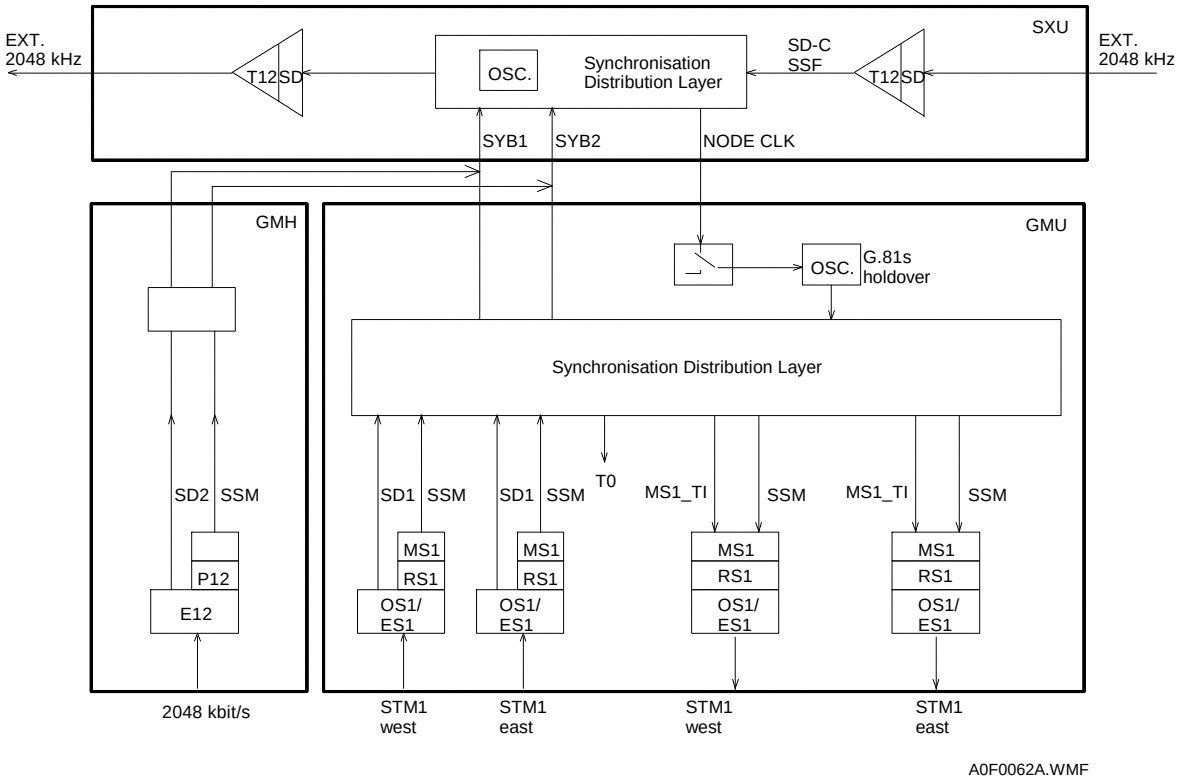


Fig. 122: Basic Node Synchronization

If the reference with the highest quality and priority fails, the one with the next highest quality is selected from the fallback list. If all reference clocks should fail, GMU and GMU-M's local oscillator provides holdover clock.

The local oscillator is an SDH Equipment Clock (SEC) generator defined by DE/TM3017-5 and G.813.

Main Characteristics of SEC

Frequency accuracy	± 4.6 ppm
Pull-in range	> ± 5 ppm
Holdover mode accuracy	0.05 ppm initially (prETS 300 462-5 graph)

Reference clock is distributed in the network according to the network topology. In a ring the direction of clock source must change when the alternative clock source is chosen. Synchronization Status messages (SSM) in S1 byte carry clock quality information in a ring. SSM can be used in other network topologies also.

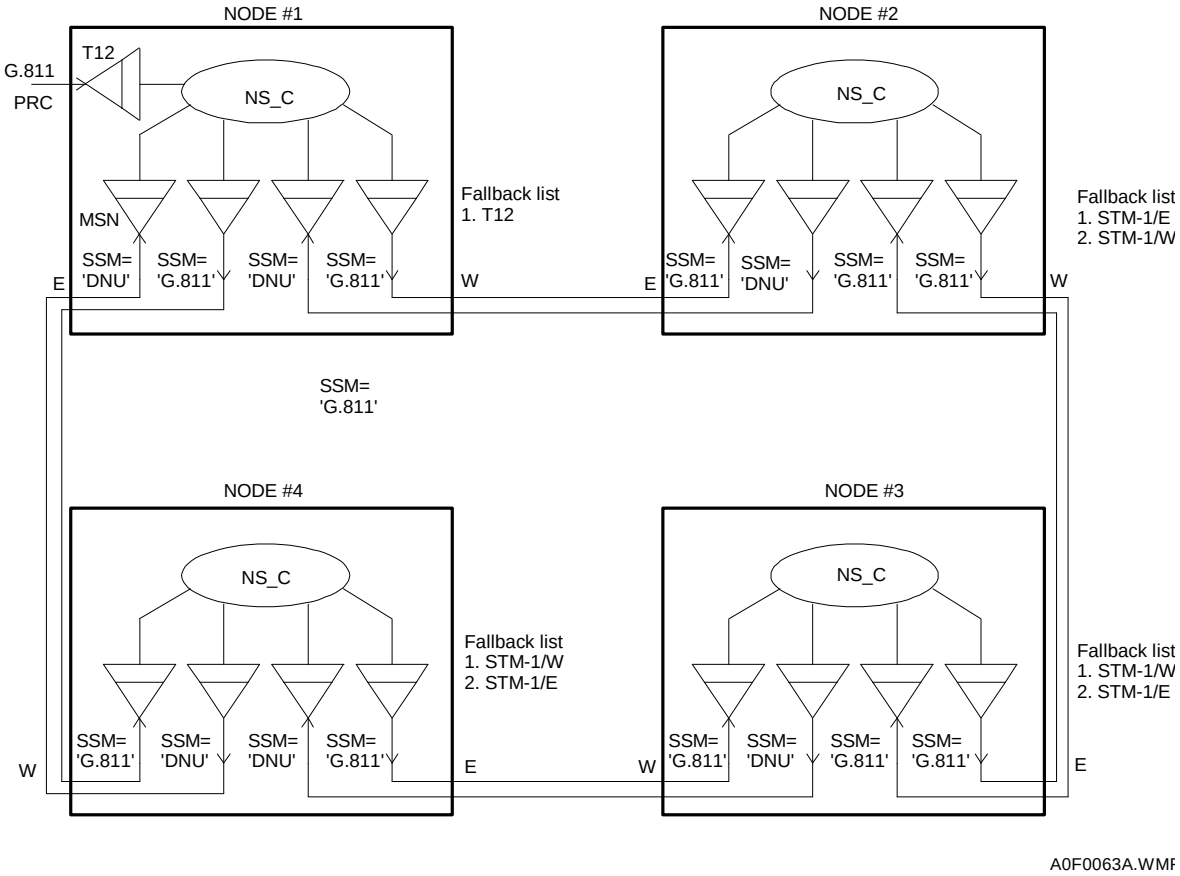


Fig. 123: An Example of Clock Distribution in a STM-1 Ring

Fig. 123 shows an example of four nodes in a ring in the normal operating state with possible fallback lists and the corresponding SSM codes. Node #1 receives PRC from the G.703 port and distributes the clock to the other nodes via STM-1 as shown.

If for example the link from Node #1 to Node #4 fails, Node #4 enters a holdover state. Node #4 changes the SSM sent to Node #3, so that Node #3 becomes aware of the holdover state. Node #3 then switches to the second reference on the fallback list. After that Node #4 switches to the second reference on the fallback list and synchronization in the ring is restored.

6.14.2.14 DXX Network Management Control Channels

GMU and GMUM are controlled by the DXX Network Management System (NMS). GMU and GMU-M can terminate two NMS Control channels (64 kbit/s HDLC). Any of the following bytes in the synchronous ports can be used to carry control messages:

STM-1 East/West	SOH	D1 to D12, E1,E2,F1, NU1 to NU6, R1 to R6,U1 to U26, Z12, Z13, Z21, Z22
STM-1 East/West	VC-4 POH	F2, Z3, N1
STM-1 East/West	any C-2	Rn
STM-1 East/West	any C-12	Rn
S34M East/West	Overhead	NR, F, DC1 to DC3 (proprietary)
S34M East/West	any C-12	Rn

If more than two control channels are required, the optional SCP module of SCU unit can be used. The SCP module can terminate four additional channels, which can be cross-connected to GMU and GMU-M to any of the bytes listed above.

GMU and GMU-M cannot terminate the TMN standard Q3 Management Control Channels (DCCR and DCCM), but they can be cross connected through GMU and GMU-M as described in the previous section.

An example of the NMS communication network is shown in Fig. 124. In access networks, where DCCM channel is available, MSOH byte D4 is primarily used. Between access networks, which are connected in the transport network by VC-2 or VC-12, NMS control channel is carried in a payload byte in a VC-2 or VC-12.

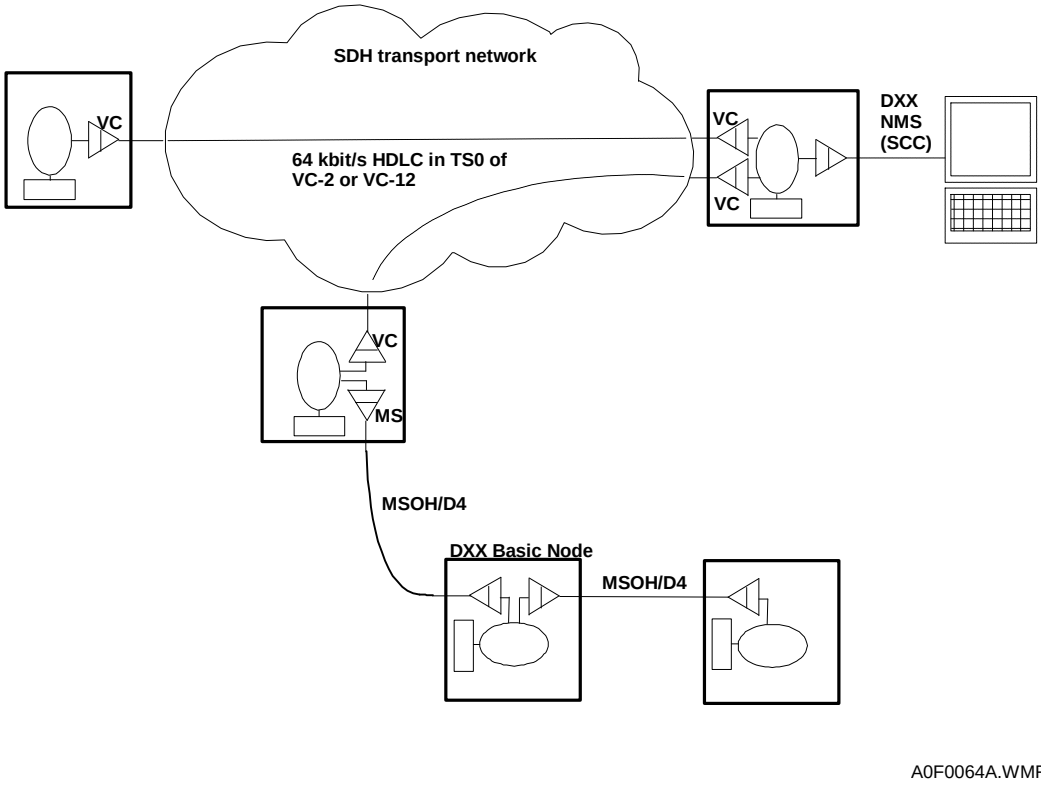


Fig. 124: An Example of NMS Communication Channels

NMS control channels in a DXX node are presented in Fig. 125, which shows SCU, SCP, GMH and GMU or GMU-M units and management link connections and terminations. Within the DXX Node units communicate via the local VTP-bus.

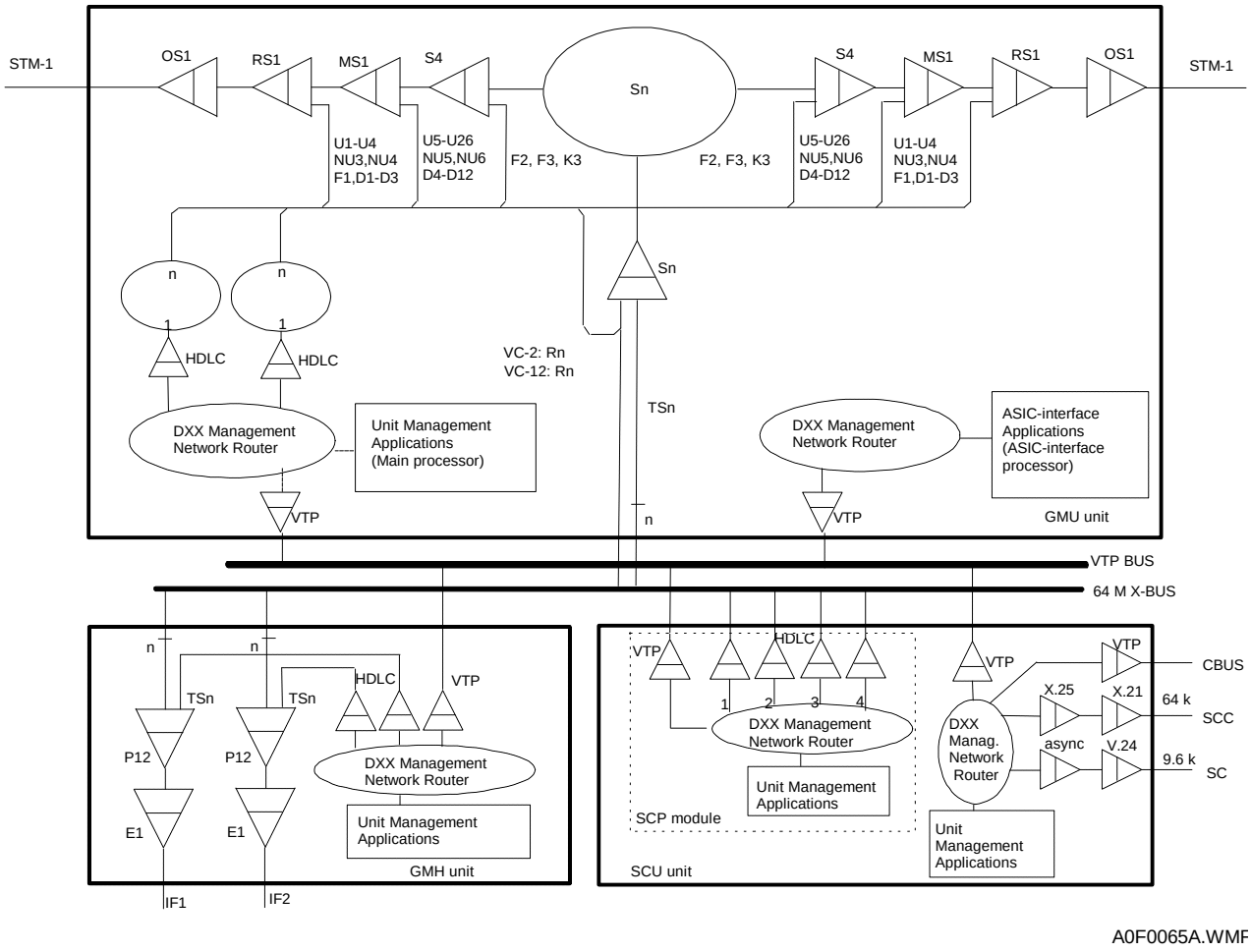


Fig. 125: Management Communication in a DXX Node with GMU or GMU-M

6.14.2.15 Node Requirements

For installation of GMU and GMU-M into a Basic, Midi or a Cluster Node, hardware and software of other DXX units must have the following or later version.

SCU Node control unit equipped with

— SCZ 280, SCU 210 software module, V8.3
— SCP 211 (HDLC-4CH) Control Channel Expansion Module, V3.0
— SCZ 281, SCP 211 software module, V3.0

In a Basic Node SXU-A or SXU-B Cross-connect unit equipped with

— SXZ 282, SXU software module V6.6

In a Cluster Node SXU-C Cross-connect unit equipped with

— SXZ 289, SXU-C software module V2.7

In a Cluster Node CXU-M Master cross-connect unit equipped with

— SXZ 288, CXU-M software module, V2.7

NMS release 9.0 is required.

GMU-M and GMU are shown as GMU units in the NMS. In other words, GMU-M in a node is shown as GMU unit and the unit software can be used to identify the unit to be GMU-M unit.

6.14.3 Interface Modules for GMU and GMU-M units

6.14.3.1 General

The interface modules available for GMU and GMU-M units:

— STM-1-SH-13
— STM-1-LH-13
— STM-1-E
— SYN-34-E

GMU and GMU-M can be furnished with one or two interface modules. Every module contains one standard interface. GMU and GMU-M must be removed from the subrack for insertion or removal of an interface module.

Mode	Number of interface modules
TM	1
TM1+1	2
ADM	2

Name	Module Code	Function	Pcs. / GMU
STM-1-SH-13	ODH 451	Optical STM-1 interface module (S-1.1)	0...2
STM-1-LH-13	ODH 454	Optical STM-1 interface module (L-1.1)	0...2
STM-1-E	GDH 455	Electrical STM-1 module	0...2
SYN-34-E	GDH 456	Electrical S34M interface module	0...2

Every interface module contains the following main blocks:

1. Optical/electrical interface
2. Clock recovery
3. STM-1 and VC4 or S34M termination
4. Transmit clock multiplication

Power Supply Module

Module Code	Function	Pcs. / GMU
PDF 452	Power supply module 48 V	0...1
PDF458	Power supply module 24 V	0...1

PDF 452 is the DC/DC conversion module for battery voltage of 48 V (30 to 60 V). Output voltages are 3.3 V, 5 V, 12 V and -12 V.

PDF458, a DC/DC conversion module is intended for battery voltage of 24V (19 to 32V). Output voltages are as in PDF452.

6.14.4 Faults

6.14.4.1 Terminology

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Alarm
R = Red alarm LED
Y = Yellow alarm LED
RxAIS = AIS insertion to Rx signal
RDI = Remote Defect Indicator
MFrFEA = Multiframe level far-end alarm (FR0/TS16/Bit6)

6.14.4.2 GMU and GMU-M Faults and Actions

Common Logic Faults (Block CommUnit)

Fault Condition	Status	LED	Rx signal	Tx signal	Note
"Reset (GMZ460) or (GMZ461)" There has been a unit reset (detected always after the power-up of the unit).	PMA, S	R	Bus if off	Off	[a]
"VB1: +5 V (BUS1) " The voltage is below the threshold limit (about 4.6 V depending on the calibration and the A/D resolution).	PMA	R	-	-	[b]
"Power +12 V" The voltage is below the threshold limit (about 11.3 V depending on the calibration and the A/D resolution).	PMA	R	-	-	[b]
"Power -12 V" The voltage is above the threshold limit (about -11.3 V depending on the calibration and the A/D resolution).	PMA	R	-	-	[b]
"Power +3.3 V (GMZ460) " The voltage is above the threshold limit (limit depends on the calibration and the A/D resolution).	PMA	R	-	-	[b]
"Protected bus voltages" Protected bus voltages are above the threshold limit (limit depends on the calibration and the A/D resolution).	PMA	R	-	-	[b]
CPU memory faults (There are separate fault for GMZ460 and GMZ461) RAM fault EPROM fault FLASH faults	PMA, S	R	-	-	-
Incompatible EPROM/FLASH SW	PMA, S	R	-	-	-
Check sum err in downloaded SW	PMA, S	R	-	-	-
"SW unpredicted" This fault condition should never occur (or not yet supported).	PMA, S	R	-	-	-
"Missing Settings" One of the setting structures has been corrupted in the non-volatile memory.	PMA, S	R	-	-	-
“ Settings corrupted” Functional settings of GMU are corrupted	PMA	R	-	-	-

Common Logic Faults (Block CommUnit)

Fault Condition	Status	LED	Rx signal	Tx signal	Note
"CRC err.LAC RAM 1/2/3/4" CRC error detected at one of the ASIC's ram memories.	PMA, S	R	-	-	-
"Start permission denied" Most likely the unit does not belong to the node configuration.	PMA, S	R	Bus IF off	Idle pattern in the payload	-
"System clock missing" 19.44 MHz clock of the GMU is missing.	PMA, S	R	-	-	-
"Node clock missing" 16.896 MHz node clock missing. A typical reason for this fault is that SXU is missing.	PMA, S	R	-	-	-
"F/MSYNC problem in X-bus" The fault is activated if X-bus synchronization pulse transmitted by the SXU is missing. A typical reason for this fault is that SXU is missing. If only one GMU unit has this fault although there are other GMU units in the subrack then the fault is most likely in the GMU unit.	PMA, S	R	-	-	-
"16/20MHz clks not locked" 19.44 MHz of the GMU clock not locked with 16.896 MHz clock of the node.	DMA	R	-	-	-
"Backup unit (SCP) fault" Extended backup unit not responding. Probably it is missing or not in inventory.	PMA	Y	-	-	-
"Osc. phase transient suppression fail" Tx phase transient over limits.	MEI	Y	-	-	-
"Clk. freq. outside of holdover range" Node clock cannot be measured by the GMU for the holdover mode.	DMA	R	-	-	-
"IA alarm from IA mon" The IA addresses do not work correctly.	PMA, S	R	-	-	-
"Improper control unit" GMU-M does not work in a Cluster Node	PMA	R	Bus IF off	Idle pattern in the payload	-
"Hdlc/x-bus in same TS" The fault is activated if the HDLC control channel bit(s) are also used by the cross-connection bus. The HDLC control channel is located to a cross-connect TS. Control channel data overdrives cross-connection data.	DMA	R	-	-	-
"No extended backup unit address" Control unit returns no address of the extended backup unit. Capacity of the extended backup unit may have run out (especially when not using the SCP unit)	PMA	R	-	-	-

a Fault message (with delta event) appears when the unit starts to operate.

b Rx signal action depends on the status of each TTP.

Neighbour Node Monitoring Faults (Block NNM1, NNM2)

Fault Condition	Status	LED	Rx signal	Tx signal
"No response (NNM) " The control channel of the interface is used and the neighbour node supervision option of the interface is on and no NNM (Neighbour Node Monitoring) message has been received from the interface within 8 seconds.	PMA, S	R	-	-
"Wrong id in NNM msg" The control channel of the interface is used and the neighbour supervision option of the interface is on and the received NNM message contains unexpected neighbour identification data.	PMA,S	R	-	-

Neighbour Node Monitoring Faults (Block NNM1, NNM2)

Fault Condition	Status	LED	Rx signal	Tx signal
"Own NNM msg received" The control channel of the interface is used and the neighbour supervision option of the interface is on and the received NNM message contains same identification data as the NNM message sent to the interface.	PMA, S	R	-	-

Interface Module Faults (Block IFMOD-1, IFMOD-2)

Fault Condition	Status	LED	Rx signal	Tx signal
"If module missing" The interface module defined in the settings is missing.	PMA,S	R	-	-
"Incorr. if.module" There is a conflict between the installed module and the settings.	PMA,S	R	-	-
"LO transmitt clk" Loss of the 155.52 MHz transmit clock when using STM-1 interface module.	PMA,S	R	-	-
"LO ph. locking for 68.368MHz (34M) " Loss of phase locking for 68.368MHz when using S34M interface module. The 34.368 MHz transmit clock cannot be generated.	PMA, S	R	-	-
EEPROM faults	PMA, S	R	-	-
"Tx power limit exceeded" Transmit power of the optical interface module exceeds its limit.	DMA	R	-	-

GMZ460/GMZ461 Faults (Block SW-GMZ460, SW-GMZ461)

Fault Condition	Status	LED	Rx signal	Tx signal
"Chsum err in dnl program" The downloaded software has been corrupted.	PMA, S	R	-	-
"Incomp.SW (GMZ460:eprom/flash) " The fault is activated if there is downloaded software in flash but the revision is wrong (for example if EPROM SW is r5.5 and downloaded SW is r6.1).	PMA, S	R	-	-
"Setup data mismatch (between units) " Information stored to setup is self-contradictory.	PMA	R	-	-
"Initialization error " Initialication of application SW unsuccessful (after the power-up of the unit).	PMA, S	R	-	-

Electrical STM1 IF1/IF2 Faults (Block STMIF2-eSPITTP, STMIF2-eSPITTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"Faults masked" The fault is activated when interface Fault mask setting is on	MEI	Y	-	-
"LOS" Loss of signal. Loss of signal defect is declared when a supervised signal hasn't had any transitions for a period of time or the signal indicating degradation of level in received signal is activated.	PMA, S	R	RxAIS	-
"ES Equipment loop" ES loop is active. Electrical section TX to RX loop activate.	MEI, S	Y	-	-

Optical STM1 IF1/IF2 Faults (Block STMIF2-oSPITTP, STMIF2-oSPITTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"Faults masked" The fault is activated when interface Fault mask setting is on	MEI	Y	-	-

Optical STM1 IF1/IF2 Faults (Block STMIF2-oSPITTP, STMIF2-oSPITTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"LOS" Loss of signal. Loss of signal defect is declared when a supervised signal hasn't had any transitions for a period of time or the signal indicating degradation of level in received signal is activated.	PMA, S	R	RxAIS	-
"OS Equipment loop" OS loop is active.	MEI,S	Y	-	-

Electrical 34M IF1/IF2 Faults (Block 34MIF1eSPITTP, 34MIF2eSPITTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"Faults masked"	MEI	Y	-	-
"LOS"	PMA, S	R	RxAIS	-
"E34M Equipment loop" E34M loop is active.	MEI, S	Y	-	-

RSTTP STM1 IF1/IF2 Faults (Block STMIF1rsTTP, STMIF2rsTTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"Faults masked" The fault is activated when interface Fault mask setting is on	MEI	Y	-	-
"SSF" Server signal fail. Defect in above layer set SSF to below layer (example defect in regeration section set SSF active in multiplex section).	PMA, S	R	RxAIS	-
"LOF" See CCITT G.706 Loss of frame alignment. Loss of frame. Frame alignment is done according to requirements presented in DE/TM-1015-1 and G.783.	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is enabled..	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is disabled..	MEI	Y	-	-
"DEG" Signal degrade. Once every second, block errors shall be compared with limit value. If errors count Š limit the one second shall be declared BAD, otherwise it shall be declared GOOD. The Signal Degrade defect (dDEG) shall be detected if M consecutive BAD seconds have occurred. The Signal Degrade defect (dDEG) shall be cleared if M consecutive GOOD seconds have occurred. M value range 2…9.	DMA	R	-	-
"UNAVAIL" Performance monitoring unavailable state (G.774.01).	DMA		-	-
"QOS" Quality of signal. 24 hours period. At least one of SES, BBE or ES limit exceeded. Cleared when period changes.	DMA		-	-
"QOSTR" Quality of signal. 15 minutes period. At least one of limits ES, BBE , SES has been exceeded. Cleared when found a period where none of the ES, BBE or SES limits has been exceeded. Note that ES and BBE have upper/lower limit so that upper must be exeeded to get a fault and lower is used as a limit when fault is cleared	DMA		-	-
"RS Line loop" RS loop is active. Regeration section RX to TX loop activate.	MEI, S	Y	-	-

MSTTP STM1 IF1/IF2 Faults (Block STMIF1msTTP, STMIF2msTTP)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"SSF"	PMA, S	R	RxAIS	RDI
"AIS" Alarm indication signal. In S34M interface AIS defect is detected according to DE/TM-01015-2-1.	MEI, S	Y	RxAIS	RDI
"DEG"	DMA	R	-	-
"RDI" Remote defect indicator 5 consecutive equal new values of the RxRDI.	MEI	Y	-	-
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-
"MS Line loop" MS loop is active.	MEI, S	Y	-	-

VC4TTP STM1 IF1/IF2 Faults (Block STMIF1vc4TTP, STMIF2vc4TTP)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"SSF"	PMA, S	R	RxAIS	RDI
"SLM" Signal label mismatch. Received signal label not valid.	PMA. S	R	RxAIS	RDI
"UNEQ" Received signal label at UNEQ state.	PMA. S	R	RxAIS	RDI
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is enabled..	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is disabled..	MEI	Y	-	-
"DEG"	DMA	R	-	-
"RDI"	MEI	Y	-	-
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-
"LOM" Loss of multiframe alignment. The multiframe indication byte H4 is interpreted according to ITU-T G.783 recommendations	PMA, S	R	RxAIS	-
"S4D Line loop" S4D loop is active.	MEI, S	Y	-	-

PS34TTP IF1/IF2 Faults (Block 34MIF1-psTTP, 34MIF2-psTTP)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"SSF"	PMA, S	R	RxAIS	RDI
"LOF"	PMA, S	R	RxAIS	RDI
"SLM".	PMA. S	R	RxAIS	RDI
"UNEQ"	PMA. S	R	RxAIS	RDI

PS34TTP IF1/IF2 Faults (Block 34MIF1-psTTP, 34MIF2-psTTP)

Fault Condition	Status	LED	Rx signal	Tx signal
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is enabled..	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is disabled..	MEI	Y	-	-
"DEG"	DMA	R	-	-
"RDI"	MEI	Y	-	-
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-
"LOM"	PMA, S	R	RxAIS	-
"PS34M Line loop" PS34M loop is active.	MEI, S	Y	-	-

VC2TTP 1…42 Faults (Block VC2-1 .. VC2-42)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"SSF"	PMA, S	R	RxAIS	RDI
"SLM"	PMA, S	R	RxAIS	RDI
"UNEQ"	PMA, S	R	RxAIS	RDI
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is enabled..	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is disabled..	MEI	Y	-	-
"DEG"	DMA	R	-	-
"RDI"	MEI	Y	-	-
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-
"MRDI groupA " When three consecutive equal new values of RxFEA is received it is accepted to the AcFEA. Multiframe remote defect indicator in signalling group A. Note: Same fault to groups B and C also available.	MEI, S	Y	-	-
"MLOF groupA " The multiframe alignment is lost when two consecutive wrong FSW values or all ‘0’ multiframe is found. The next signalling byte with four zeros in bits 1..4 is considered to be the correct FSW. To avoid a false alingment it is required that the previous signalling byte was not all ‘0’. Multiframe loss of frame in signalling group A. Note: Same fault to groups B and C also available.	PMA, S	R	RxAIS/ SigTS	MFrFEA
"MAIS groupA" Multiframe Alarm indication signal in signalling group A. The signalling AIS is detected when one signalling multiframe is all ‘1’ or contains only one ‘0’. Note: Same fault to groups B and C also available.	MEI, S	Y	RxAIS/ SigTS	MFrFEA
"Vc2 loop" Vc2 loop to line is active.	MEI, S	Y	-	-

VC12TTP 1…126 Faults (Block VC12-1…VC12-126)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"SSF"	PMA, S	R	RxAIS	RDI
"SLM"	PMA, S	R	RxAIS	RDI
"UNEQ"	PMA, S	R	RxAIS	RDI
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is enabled..	PMA, S	R	RxAIS	-
"TIM" Received trace identifier does not match with expected one, if attribute timaAisEnabled is disabled..	MEI	Y	-	-
"DEG"	DMA	R	-	-
"RDI"	MEI	Y	-	-
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-
"MRDI "	MEI, S	Y	-	-
"MLOF"	PMA, S	R	RxAIS/ SigTS	MFrFEA
"MAIS"	MEIS	Y	RxAIS/ SigTS	MFrFEA
"Vc12 loop" Vc12 loop to line is active.	MEI, S	Y	-	-

AU4CTP STM1 IF1/IF2 Faults (Block STMIF1-au4CTP, STMIF2-au4CTP)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"AIS"	MEI, S	Y	RxAIS	-
"LOP" Loss of pointer. The AU/TU-pointer is interpreted according to ETSI DE/TM-105-1.	PMA, S	R	RxAIS	-

TU2CTP STM1 IF1/IF2 Faults (Block tu12CTP-1 .. tu12CTP-126)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"AIS"	MEI, S	Y	RxAIS	-
"LOP"	PMA.S	R	RxAIS	-

TU12CTP STM1 IF1/IF2 Faults (Block tu12CTP-1 .. tu12CTP-126)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-
"AIS"	MEI, S	Y	RxAIS	-
"LOP"	PMA.S	R	RxAIS	-

PROTECTED TTP (MS OR PS34M) Faults (Block MSP-1)

Fault Condition	Status	LED	Rx signal	Tx signal
" Faults masked "	MEI	Y	-	-

PROTECTED TTP (MS OR PS34M) Faults (Block MSP-1)

Fault Condition	Status	LED	Rx signal	Tx signal
"UNAVAIL"	DMA		-	-
"QOS"	DMA		-	-
"QOSTR"	DMA		-	-

PROTECTION GROUP (MS OR PS34M) Faults (Block MSPG-1)

Fault Condition	Status	LED	Rx signal	Tx signal
"Group Failed" Both working and protecting channels failed when using MS 1+1 or SNC protection.	PM, ,S	R	-	-
"Group DEG" Block errors indicated read from MS/PS34M 1+1 protected TTP.	DMA	R	-	-
"SSF (working) " Protected channel has a serious fault (MS/PS34M 1+1 or SNC protection).	DMA	R	-	-
"SSF (protecting) " Protecting channel has a serious fault (MS/PS34M 1+1 or SNC protection).	DMA	R	-	-
"FOP" Failure of protocol when using MS 1+1 protection: -Protection switching time not within 50 ms. -Request active, but no answer from far end. - One end is in 1+1 mode and the other in 1:1.	DMA	R	-	-

SNC PROTECTION GROUP (MS OR PS34M) Faults (Block SNCG-1 .. SNCG-32)

Fault Condition	Status	LED	Rx signal	Tx signal
"Group Failed"	PMA, S	R	-	-
"SSF (working) " (MS/PS34M 1+1 or SNC protection).	DMA	R	-	-
"SSF (protecting) "	DMA	R	-	-

6.14.5 GMU Front Panel

GMU and GMU-M front panel contains two leds, red and yellow indicating PMA and MEI alarms. There is also optical SC connectors for the STM-1 ports or electrical SMB connectors for STM-1/S34M ports.

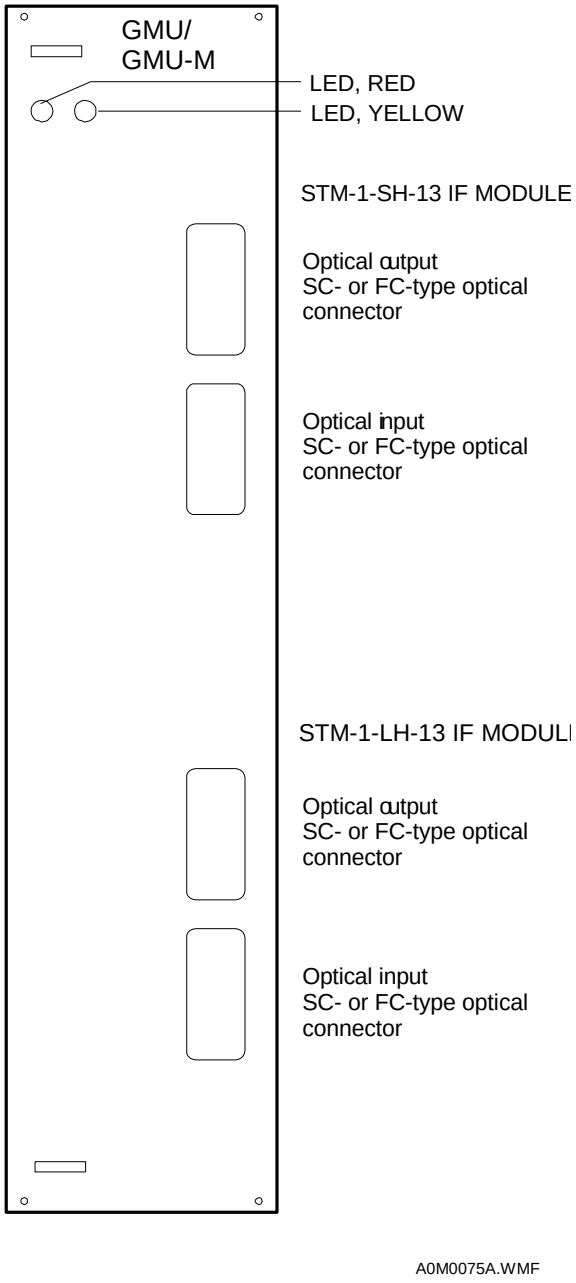


Fig. 126: Front panel for GMU and GMU-M with STM-1-SH-13 and STM-1-LH-13

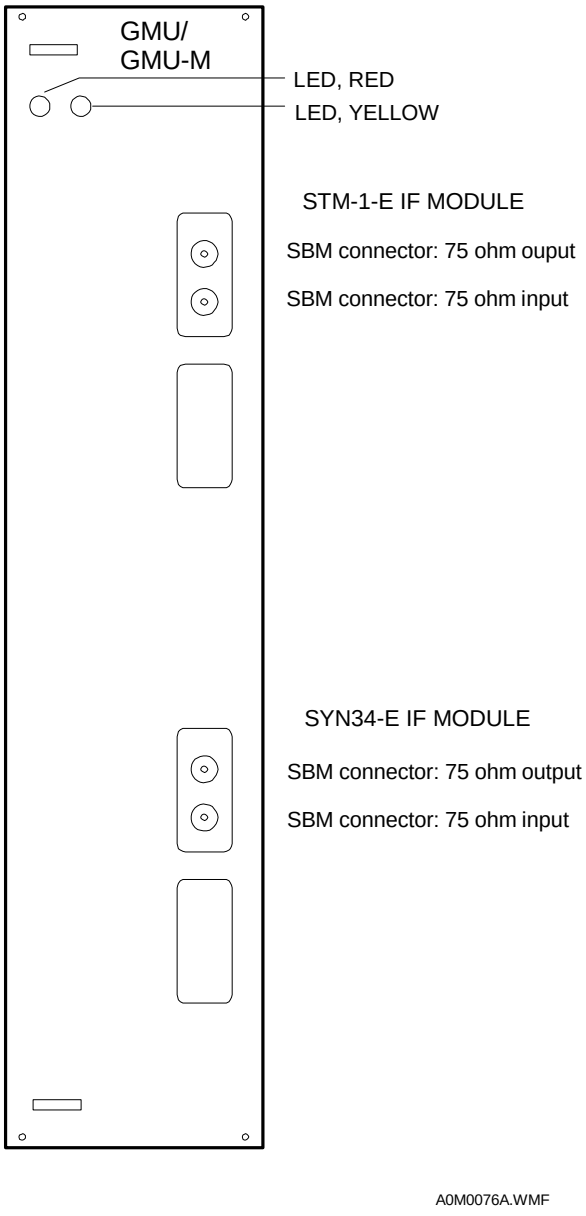


Fig. 127: Front panel for GMU and GMU-M with STM-1-E and SYN34-E interface module

6.14.6 Technical Specifications

GMU and GMU-M have three operating modes

— terminal multiplexer (TM)
— terminal multiplexer with MS 1+1 protection (TM1+1)
— add-drop-multiplexer (ADM)

Trunk Interfaces

— STM-1 electrical, G.703
— STM-1 optical short-haul, G.957 (S-1.1)
— STM-1 optical long-haul, G.957 (L-1.1)
— 34 Mbit/s electrical, G.703

STM-1 Electrical Interface

Bit rate	155.52 Mbit/s
Input tolerance	±20ppm
Code	CMI
Nominal impedance	75 ohm
Pulse shape	G.703 figures 24 and 25
Maximum input attenuation	12.7 dB at 77.76 MHz ($\sqrt{f}$)
Jitter tolerance	G.825 § 4.1
Connector type	SMB (unbalanced 75 Ohm)

STM-1 Optical Interface Short-Haul (S-1.1)

Bit rate	155.52 Mbit/s
Input tolerance	±20ppm
Code	NRZ
Pulse shape	G. 957 fig. 2
Transmission path	Standard single-mode fibre (G.652 , G.957)
Optical transmitter	LASER multi-longitudinal mode transmitter
Operating wavelength range	1261…1360 nm
Maximum spectral RMS width	7.7 nm
Mean launched power	
-minimum	-15 dBm
-maximum	-8 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	PIN-diode
Receiver sensitivity (BER 1E-10)	-28 dBm
Receiver overload	-8 dBm
Connector type	SC

STM-1 Optical Interface Long-Haul (L-1.1)

Bit rate	155.52 Mbit/s
Input tolerance	±20ppm
Code	NRZ
Pulse shape	G. 957 fig. 2
Transmission path	Standard single-mode fibre (G.652,G.957)
Optical transmitter	LASER multi-longitudinal mode transmitter
Operating wavelength range	1280…1335 nm
Maximum spectral RMS width	4 nm
Mean launched power	
-minimum	-5 dBm
-maximum	0 dBm
Minimum extinction ratio	10 dB
Optical receiver	PIN-diode
Receiver sensitivity (BER 1E-10)	-34 dBm
Receiver overload	-10 dBm
Connector type	SC

S34M Electrical Interface

Bit rate	34.368 Mbit/s
Input tolerance	±20ppm
Code	HDB3
Nominal impedance	75 ohm
Pulse shape	G.703 figure 17
Jitter tolerance	G.823 § 3.1.1
Connector type	SMB (unbalanced 75 Ohm)
Frame structure	G.832

Matrix 4/1

Matrix type	4-port
	T-S, strictly non blocking
Cross connection level	VC-2, VC-12
Connection types	unidirectional
	bi-directional
	loop
Connection capacity	4 x STM-1 port equivalent (two trunk ports, a tributary port and a monitoring port)
Delay	VC-12 from STM1 port to STM1 port less than 50 µs

Termination and Mapping

Frame structures	STM-1, G.707
	34 Mbit/s, G.832
Trail termination	VC-4 (east and west)
	P31s (G.832) (east and west)
	VC-2 x 10
	VC-2-mc (m = 2…10)
	VC-12 x 32
	VC-12-mc (m = 2…32)
Mapping	n x 64 kbit/s byte synchronous floating
SOH access	most SOH channels can be cross connected and accessed from other DXX interface units.
Concatenation	virtual concatenation of VC-2 and VC-12

Other Characteristics

Clock generator	Short term as in G.813 Long Term accuracy ±4.6 ppm
Clock source	STM-1, 2048 kbit/s, 2048 kHz
Line protection	Linear Multiplex Section 1+1
	Subnetwork Connection Non-intrusive 1+1 for VC-2, VC-12
Power supply	48 V DC with PDF452 24 V DC with PDF458
Power consumption	25 W
Unit size	76 x 160 x 233 mm (w x d x h)
Unit width	15 T

6.14.6.1 Relevant SDH Standards

ETSI Standards:

ETS 300 147	SDH multiplexing structure, Jan 1995
ETS 300 417-1-1	Generic functional requirements for SDH transmission equipment
	Generic processes and performance, Feb. 1995
DE/TM-1015	Generic functional requirements for SDH transmission equipment
	part 2 Physical section layer functions, March 95
	part 3 STM-N regenerator and multiplex section layer functions, May 95
	part 4 SDH path layer functions, June 95
	part 6 Synchronization distribution layer functions, June 95
DE/TM-3017	Generic requirements for synchronous networks
	Part 1 Definitions of synchronization terminology, Oct. 94
	Part 2 Synchronization network architecture, Mar 95
	Part 3 The control of jitter and wander within synchronization networks, Sep. 95
	Part 5 Timing characteristics of slave clocks suitable for operation in SDH eq., May 95
DE/TM-3042	SDH Network Protection Schemes: APS Protocols and operation, Aug. 95

ETSI Technical Reports

DTR/TM-3025 SDH Network Protection Schemes: Types and characteristics, Sep. 95

ITU-T recommendations

G.703	Physical/electrical characteristics of hierarchical digital interfaces, 91
G.707	Network node interface for the SDH, Oct. 95
G.775	Loss of signal (LOS) and Alarm Indication Signal (AIS) defect detection and clearance criteria, Oct. 93
G.781	Structure of recommendations for SDH, Jan 94
G.782	Types and general characteristics of SDH equipment, Jan 94
G.783	Characteristics of SDH equipment functional blocks, Jan 94
G.803	Architectures of transport networks based on the SDH, Mar 93
G.81s (813)	Timing requirements at the outputs of slave clocks suitable for SDH operation on international digital links, July 95
G.825	The control of jitter and wander within digital networks which are based on the SDH hierarchy, Mar 93
G.826	Error performance parameters and objectives for international constant bit rate digital paths at or above the primary rate, Nov. 93
G.832	Transport of SDH elements on PDH networks, Nov. 94
G.841	Types and characteristics of SDH protection architectures, May 95

6.15 ISD-LT/ISD-NT Transparent Basic Rate ISDN U-Interface Unit

6.15.1 General

ISD-LT and ISD-NT are 10-T wide interface units in a DXX node. The units give a possibility to use the DXX network as so called “transparent” link in a third party ISDN network. One unit holds four 160 kbit/s bit rate U-interfaces for connecting ISDN NT1 or DXX STU-160 network terminating units to the DXX network.

The ISD-LT unit consists of a 10T UBU base unit, a unit power supply module, an ISD-LT power supply module, an LT-type ISDN transparent module and a Baseband 160 kbit/s module.

The ISD-NT unit consists of a 10T UBU base unit, unit power supply module, an NT-type ISDN transparent module and a Baseband 160 kbit/s module.

The U-interface bit rate is 160 kbit/s where the user bit rate is 144 kbit/s (2B+D channels). The cross-connection within the DXX network can be done in a 2 Mbit frame. All data in a 160 kbit frame is transferred through the DXX network. 2B+D channels are transferred transparently and the overhead bits of the frame are transferred “semitransparently” inside a proprietary 8 kbit/s C-channel.

The cross-connect capacity of interface depends on the interface mode. In the ISD-NT unit it is always 152 kbit/s. In an ISD-LT unit it is 152 kbit/s in TE mode and 136 kbit/s in DXX mode.

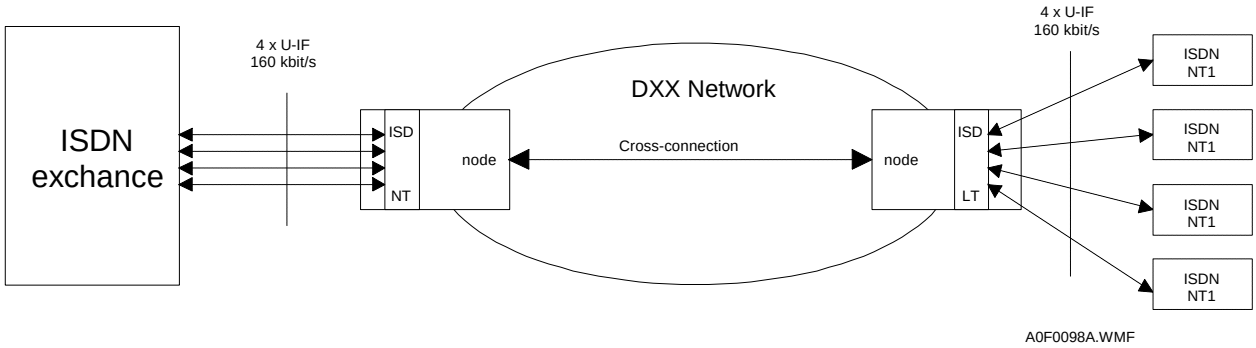


Fig. 128: ISD unit application in ISDN network

6.15.2 Operation of ISD-LT/ISD-NT Interface Unit

6.15.2.1 Mechanical Design

The mechanical design of the UBU base unit is based on standard DXX system mechanics. The unit can occupy any card slot in the subrack; however, general recommendations for subrack equipping should be followed.

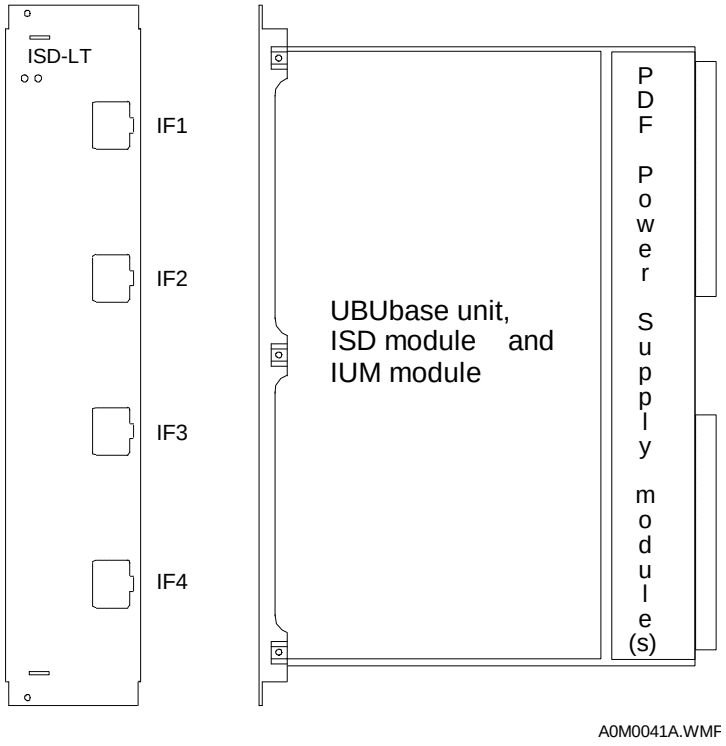


Fig. 129: ISD-LT/ISD-NT Mechanical Structure

The unit front panel houses alarm LEDs and four 8-pin modular user interface connectors.

There are two module locations on the UBU, the left one in an ISD unit is for an ISD transparent module and the right one is for an IUM interface module. The ISD module is physically and functionally between the base unit and the IUM module.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

6.15.2.2 Functional Structure

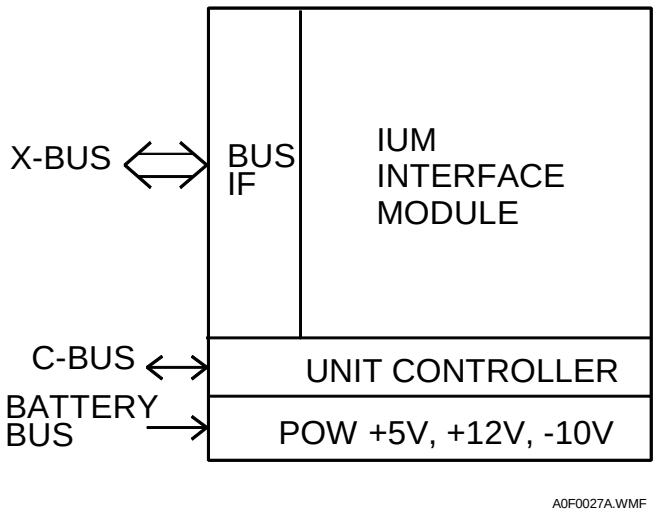


Fig. 130: Functional Structure of IUM-5T

The main functional blocks of the UBU unit include a power supply, a processor with its peripheral circuits, various interfaces for the interface module and an X-bus interface.

The power supply generates operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to the control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor may generate HDLC messages and process HDLC messages received from channels located on the interface module.

The interface module converts physical interface signals to/from signals designed for the unit's digital circuits.

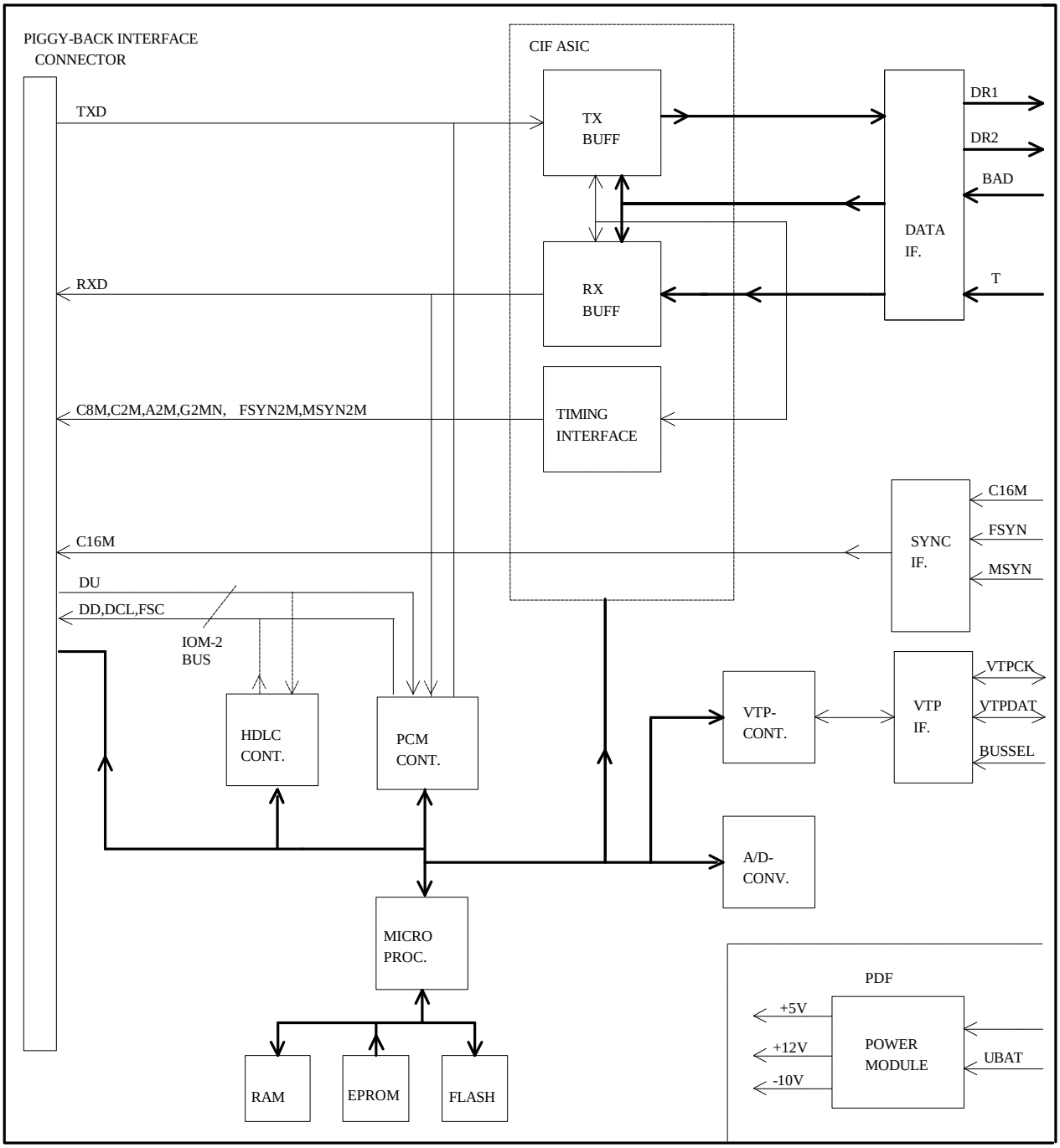
The transmit buffers of the channels are used to store data received from the cross-connect via the X-bus which means that there is always a time slot available for transmit by the Tx-frame block. The transmit buffers also synchronize the phase of the transmitted data with the phase of the X-bus.

The receiving buffers of the channels store incoming data so that required time slots are always available to the cross-connect unit.

Most of the blocks between the interface connector and the DXX bus are realized with CIF ASIC.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

6.15.2.3 Block Diagram



A0F0026A.WMF

Fig. 131: Block Diagram of Base Unit

6.15.2.4 Power Supply

The base unit and modules receive their operating voltage from the power supply module PDF 488. This module can be replaced as a whole and is plugged into the unit with connectors. The module is fixed with screws in the place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides operating voltages +5V, +12V and -10V. The module receives also a +5V bus voltage which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset-circuit, and low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D-converter. An alarm is generated if a voltage exceeds its limits.

The ISD-LT unit includes also the PDF 524 power supply module which generates the voltage of -130V for ISD-LT module. This voltage is separated from logic ground and is regulated dropped down in module separately forto each interface to the level controlled by NMS.

PDF 524 Power Supply module

A DC/DC unit power supply module PDF524 provides the voltages of -130V and +5V for interfaces on interface module ISD494 in ISD-LT unit. The power supply module gets the DXX battery voltage via the base unit and converts the output voltages for the module.

The output voltages are separated from input and logic ground. The nominal DC input voltage is 48V, 24V input is not supported.

6.15.2.5 Unit Controller

The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM memory. Part of the application programs are stored in a non-volatile FLASH memory, thus enabling the update of these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in case of power interruption, the unit is automatically reset to the conditions prevailing prior to the interruption without specific parameterization. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC links.

6.15.2.6 Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus whenever there is no other traffic on the bus. When a unit is transmitting, it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

6.15.2.7 A/D-Converter

The unit includes a multi-channel analogue-to-digital converter (A/D) which monitors the operating voltages as well as the control voltages from the interface module connector. The control voltage is application-dependent.

6.15.2.8 X-bus Interface

The main signals of the X-bus interface are:

Signal	Signal description
C16M	Internal timing signal for the node
FSYN, MSYN	Frame and multiframe alignment signals
DR10 - 17	8-bit-wide data bus UBU towards SXU
DR20 - 27	8-bit-wide duplicate of the data bus UBU towards SXU
T0 - 7	8-bit-wide data bus SXU towards UBU
BAD0 - 7	8-bit-wide addressing bus SXU to UBU

The X-bus interface transmits and receives one byte of data each time an interface of the unit is addressed by the BAD0 - 7 bus. For each 125–µs bus frame the interface can be addressed one or more times depending on the XB capacity (N x 64 kbit/s). A channel below bit rate 64 kbit/s is transferred between the UBU and the cross-connection unit SXU using one byte per frame (64 kbit/s) and utilizing one or more of the 8-data bits, 8 kbit/s each, of the byte. The SXU maps only the used bits to the connection.

The bus functions are monitored also by the interface units. When an interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm in case it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing, the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

In the DXX system the bus frame repetition frequency is always 8 kHz. Several consecutive bus frames are combined into one bus multiframe. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

6.15.2.9 Loops

The operator can activate three loop types on a unit. Use of loops is relevant only in the ISD-LT unit in DXX mode. The loops are:

— interface loop: data coming from the X-bus is looped back on the module in a U interface chip
— equipment loop: data coming from the X-bus is looped back on the base unit in a PCM controller
— line loop: data coming from the line via a module is looped back on the base unit in a PCM controller

Each channel can be looped separately.

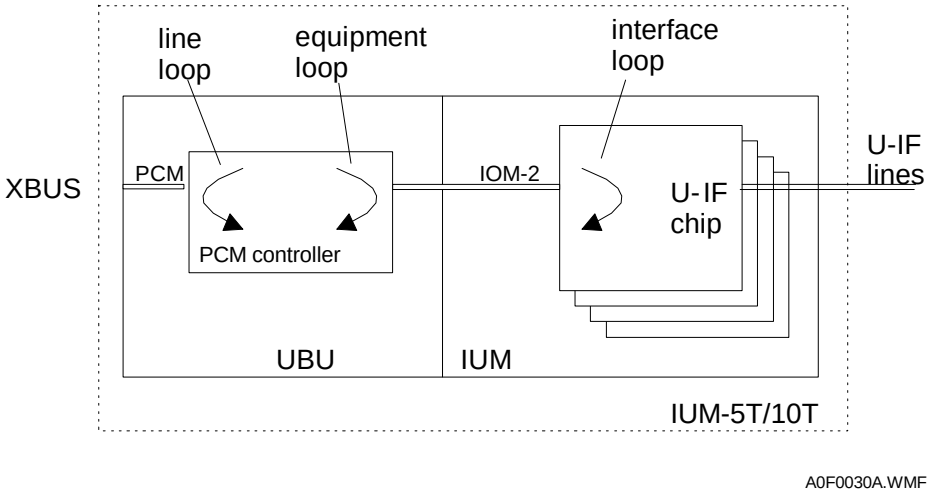


Fig. 132: Loops on a Unit

6.15.2.10 Performance Counters

The unit can support circuit performance monitoring separately for each interface. The performance signal quality monitoring is according to G.821. Performance data is collected in three ways:

- The unit collects the G.821 data for 24-hour periods starting at 00:00 hours. The 24-hour data is available during the next day for automatic transfer to the DXX performance database.
- If activated, the unit also calculates performance data for 15-minute periods. If the signal impairments during a 15-minute period exceed the limit selected by the user, the data is transferred to the performance database.
- A third set of performance counters is available for the network operator. The operator can start and terminate error monitoring at any time and gain performance data for periods that can be selected from seconds to days or months. The results are shown as error counts and as G.821 parameters.

Error Counters

Using SW and HW counters the unit is typically able to count

- number of frame losses (frame from the interface side, C1)
- number of frame word errors (frame from the interface side, C1)
- number of CRC block errors
- buffer slips and adjustments

G.821 Statistics

The error counts are transformed into CCITT G.821 parameters (see Relevant Recommendations).

- total time (seconds)
- unavailable time (seconds)
- errored seconds
- severely errored seconds
- degraded minutes

6.15.3 Modules for ISD-LT/ISD-NT Interface Unit

6.15.3.1 General

A PCM controller maps the PCM data coming from the X-bus to an IOM-2 frame for interface module. Each chip on the module handles its own time slot in the IOM-2 frame. This IOM-2 bus is fed through c-channel controller circuit in ISD module before it goes to IUM module.

The processor bus is connected to piggy-back interface connectors. Through this bus it is possible to detect the module parameters stored in an EEPROM memory on the module.

An HDLC controller maps the HDLC data between a microprocessor interface and the IOM-2 bus. The data is handled by the microprosessor and transferred through the control bus between the other units of the subrack.

The Modules for ISD-LT/ISD-NT Interface Units:

— ISD

6.15.4 Fault Conditions in ISD-LT/ISD-NT Interface Units

6.15.4.1 Signal Description

The interface blocks on the ISD unit are numbered from 1. The common parts are of block 0. The signals and directions are identified as follows:

Ref. Point	Signal Description
UI1	Input signal at the receive part of the interface
UI2	Output signal at the transmit part of the interface
C1	XB output signal towards the X-bus interface
C2	XB input signal from the X-bus interface, net signal

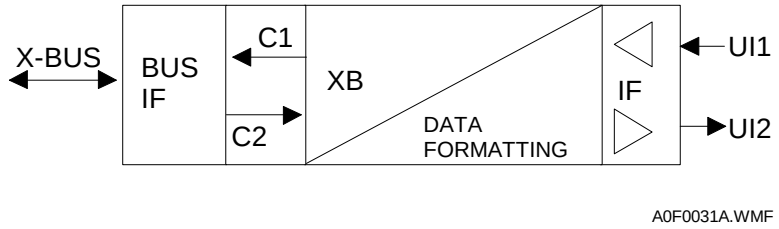


Fig. 133: Naming of Signal Reference Points

The following table contains all faults that can be monitored in an ISD-LT/ISD-NT unit, as well as the required reaction of the unit to each fault. The first number in parentheses after the fault condition name is for GPT (general problem type) and the second for SPT (specific problem type). In the LED column, R or Y means that the red or yellow LED is on. UI2 refers to the signal that the unit transmits through the interface; C1 refers to the signal that the unit sends towards the cross-connection bus in the event of a fault (hyphen means as normal as possible). The actions determined in the UI2 and C1 columns are carried out by hardware; software intervention is not required.

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Affecting Fault
R = red alarm led
Y = yellow alarm led
AIS = signal substituted by AIS

Faults in Block 0 Base Unit

Fault Condition	Status	LED	UI2	C1
unpredicted fault (1,1)	PMA	R	-	-
software error (1,20)	PMA	R	-	-
reset (2,2)	PMA, S	R	off	off
setup structure corrupted (3,19)	PMA, S	R	-	-
power supply faults: +5 V in subrack (4,3) +5 V in unit (4,4) +12 V in unit (4,5) -10 V in unit (4,6)	 PMA PMA PMA PMA	 R R R R	 - - - -	 - - - -
RAM fault (5,11)	PMA, S	R	-	-
EPROM fault (5,12)	PMA, S	R	-	-
flash write error (5,13)	PMA, S	R	-	-
flash copy error (5,14)	PMA, S	R	-	-
flash erase error (5,15)	PMA, S	R	-	-
flash duplicate error (5,16)	PMA, S	R	-	-
flash shadow error (5,17)	PMA, S	R	-	-
flash checksum error (5,18)	PMA, S	R	-	-
missing module 1 (10,22)	PMA, S	R	-	-
missing module 2 (10,23)	PMA, S	R	-	off
conflict in module type 1 (10,24)	PMA, S	R	-	off
conflict in module type 2 (10,25)	PMA, SR	R-	-	off
ASIC fault in base unit (32,30)	PMA, S	R	-	-
fault in XILINX1 (32,31)	PMA, S	R	off	off
fault in XILINX2 (32,32)	PMA, S	R	off	off
start permission (i.e. cross-connection permission) denied by SXU (36,8)	PMA, S	R	-	-
bus sync fault (38,7)	PMA, S	R	AIS	AIS
missing IA activity (40,33)	PMA, S	R	AIS	AIS
software in flash incompatible with EPROM (55,9)	PMA, S	R	-	-
checksum error in downloaded software (55,10)	PMA, S	R	-	-
HW fault in base unit (62,34)	PMA, S	R	-	-
HW strapping conflict with SW (62,35)	MEI	R	-	-
HW fault in module 1 (62,36)	PMA, S	R	-	-
HW fault in module 2 (62,37)	PMA, S	R	-	-
setup conflict (69,38)	DMA	R	-	-

Faults in Blocks 1 to 4, U Interfaces

Fault Condition	Status	LED	UI2	C1
loss of input signal (12,39)	PMA, S	R	-	AIS
bit error rate 10^{-3} (13,41)	DMA	R	-	-
CRC errors from far-end (22,42)	DMA	Y	-	-
loops (27,46)	MEI, S	Y	-	-
unit test loop on (27,26)	MEI, S	Y	-	-
no response to neighbour node message (29,27)	PMA,S	R	-	AIS
own neighbour node message received (29,28)	PMA,S	R	-	AIS
unexpected neighbour node message (29,29)	PMA,S	R	-	AIS
input buffer slip (30,48)	DMA	R	-	-
unavailable state in terms of G.821 (48,51)	PMA, S	-	-	-
NTU power fault (57,53)	PMA, S	R	-	-
fault masks (58,54)	MEI	Y	-	-
performance event (60,55)	DMA	-	-	-
activation failure (56,57)	PMA	R	-	-
U interface power fault (57,58)				

Faults in Blocks 5 to 8 (the end-to-end monitoring over DXX network for IFs 1to 4)

Fault Condition	Status	LED	UI2	C1
bit error rate 10E-3 (13,41)	DMA	R	-	-
unavailable state by G.821 (48,51)	PMA, S	-	-	-
performance event (60,55)	DMA	-	-	-
out of frame (24,59)	PMA, S	R	-	-
fault masks (58,54)	MEI	Y	-	-

6.15.5 Technical Specifications for ISD-LT/ISD-NT Interface Unit

6.15.5.1 Normative General Standards

General features

Number of channels	4
Channel capacity available to NTU user	2B+D + overhead, 160kbit/s, “semitransparently through DXX Network”

Line interface

Line rate	160 kbit/s (2B + D)
Symbol rate	80 kBaud
Signal encoding	2B1Q
Impedance	135 Ω
Line connection	2-wire full duplex
Frame structure	ETR 080
Line monitoring in DXX mode	1. Dying gasp monitoring 2. Carrier detection 3. Bit error rate (calculated from CRC)
Line power feeding	Five voltage levels: OFF, 60V, 68V, 95V, 100V, 110V Max. feeding current is 25 mA

Performance

Exceeds ETSI ISDN U-interface (ETR 080 1993) performance requirements for 2-pair 2B1Q-systems line rate 160 kbit/s.

Max. cable attenuation	better than 40 dB at 40 kHz
Max cable length	about 8 km (0.5 mm/40 nF/km cable , no noise) about 5 km (0.4 mm/46 nF cable, no noise) (guidelines only: actual length depends on cable characteristics)

Diagnostics

Loops	Interface-loop, data is looped back to XBUS on interface module Equipment loop, data is looped back to XBUS on base unit Line loop, data is looped back to line on base unit The use of loops are is relevant generallybasically in ISD-LT DXX mode only
Operation	ETR080, G.960, G.961
Statistics	G.821

6.15.5.2 Power Requirements

DC Supply

Input voltage when

— equipped with 48V PDF: 30…72 Vdc

Total power consumption

Input power (+20% tolerance included)

— ISD-LT: 11 W (without line load)
— ISD-NT: 5,6 W

6.15.5.3 Mechanics

Physical dimensions

Width: 50mm

Depth: 160 mm

Height: 244 mm

Weight: 900 g

6.16 PMP Server Unit

6.16.1 General

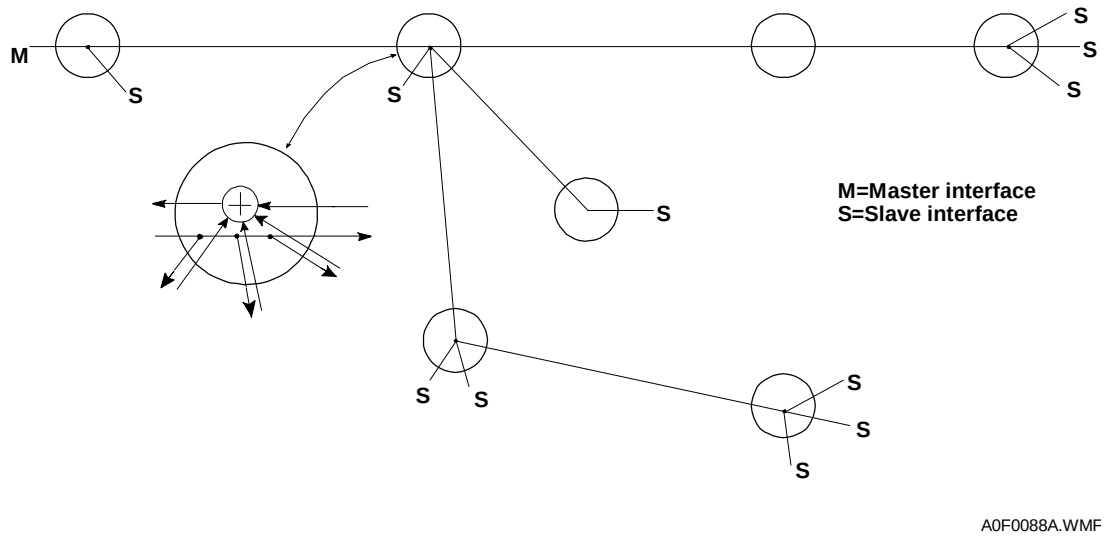


Fig. 134: A Point-to-Multipoint Connection

6.16.1.1 PMP Data Circuits in DXX Networks

A PMP circuit comprises one or several PMP servers and point-to-point subcircuits interconnecting the PMP servers and tying slave and master interfaces to bridge ports. Whenever required, the PMP bridge of a GCH or VCM unit may be activated, whereafter the unit is called a **PMP Server**. A PMP server holds one and only one PMP data bridge with one master port and several slave ports. The master port is connected to the master computer or to a slave port of an another DXX PMP bridge in direction towards the master computer. A slave port is connected to a slave DTE or to a master port of an another DXX PMP bridge in direction towards the slaves.

A DXX node may simultaneously hold PMP servers for several PMP circuits.

6.16.2 Operation

6.16.2.1 Ports of a PMP Server

There are single unit PMP servers and multi unit PMP cluster servers comprising up to eight VCM or GCH server units.

Single Unit Server

The PMP bridge function operates at the user bit rate. The bridge splits each user interface of the unit into two ports, a local port (interface) and a network port (port) for connections to remote interfaces or bridges. One bridge port is master port and all other slave ports. The unused slave ports can be switched off. The master port may be a local interface (local master) or a network port (remote master). The number of ports of a PMP server is:

Server	**Local Ports**		**Network Ports**	
Unit	Master	Slave	Master	Slave
GCH	1	1	-	2
GCH	-	2	1	1
VCM	1	3	-	4
VCM	-	4	1	3

The local ports of GCH servers may interface SBM 64E, SBM 384E or SBM 768E NTU's. The local ports of VCM are of type V.24, V.35, V.36 or X.21. If a local port of the server is used as master, the server is called an entry server. An entry server cannot be clustered.

PMP Clusters

The port capacity of a PMP bridge may be increased considerably by combining 2…8 PMP servers to a PMP cluster. The master ports (a network port) of the server are connected in parallel. The combined master port is cross connected to a remote master interface or to a slave port of the next bridge. Any mix of GCH and VCM servers may be combined into a server cluster. Local communication channels, controlling activation of the master ports, are automatically established between the member units of a PMP cluster.

Server	**Local Ports**		**Network Ports**	
Unit	Master	Slave	Master	Slave
GCH	-	N*2	1	N*1
VCM	-	N*4	1	N*3

6.16.2.2 Control Signals

The signal of the master port is broadcasted to all slave ports of a PMP circuit. The summing functions of the PMP servers conveys replies from the slaves to the master. The summing function may be 105 controlled or uncontrolled. In 105 controlled mode, only one slave is connected to the master at a time and transmission errors in passive slave branches do not disturb the traffic on the active branch. In uncontrolled mode, transmission errors in any slave branch will disturb the traffic.

At bit rates below 64 kbit/s the 105 signal is transferred within the V.110/X.30 frame. At higher bit rates is used a V.13 simulated carried. SBM 64/384/768 NTU's utilise V.13 simulated carrier att all bit rates. At rates below 64 kbit/s the V.13 of a NTU is converted to V.110/X.30 at the GCH access unit. V.13 carrier from NTU's routed via GMH will be converted to 105 at the PMP server port.

6.16.2.3 Bridge Delays

The delay of a PMP bridge is negligible. However, the 105 signal is sampled once for 8 data bits at V.110 rates (V.110S or X.30 framing), 105 turn-on delay is 8 data bits at V.13 simulated carrier and the unit change over delay in a PMP cluster is 0,5 ms.

At rates using X.30 framing (600 bit/s, 1.2…38.4 kbit/s, 48 kbit/s), 105 sampling is related to the octet timing enabling data transfer from slave ports to the master port without time skewing between data and control signals. 105/106 delay is required only to compensate for PMP cluster delay (0,5 ms/cluster) and V.13 turn-on delay for NTU tails (8 bits).

At all other rates the 105/106 delay shall be at minimum one V.13 turn-on delay for each PMP bridge (8 bits) increased by the PMP cluster delays (0,5 ms).

6.16.2.4 106 Delay

The 106 delay at slave access ports shall be dimensioned to bridge the turn on delays of the bridges between the access interface (SBM 64E/384E, VCM etc) and the master port.

At all rates using X.30/V.110S framing the 105 signal may lag the corresponding data by 0…8 bits per bridge. However, the lag is 0…4 bits at 2,4 kbit/s and 0…2 bits at rate 1,2 kbit/s.

At n*64 kbit/s and m*8 kbit/s rates (excluding 48 and 56 kbit/s) the control signal (V.13) propagates with the same rate as the data signal. However, a PMP bridge cannot activate the data port before 109 has been detected, which will cause a delay of 8 data bits for each bridge.

NTU Tails

All E-type NTU's use V.13 simulated carrier, which shall, at V.110/X.30 data rates, be converted to V.110 control signal in the GCH unit or at the PMP bridge port closest to the NTU. The conversion generates a conversion delay of 8 bits and 0…8 bits V110S/X.30 of sampling delay.

106 Delays

Bit Rate kbit/s	105 Transfer Mode	per PMP Bridge	106 Delay per Code Conversion, ms	Other Rates kbit/s
1,2	X.30	0…1,7 ms	6,7…8,4	
2,4	X.30	0…1,7 ms	3,3…5	
4,8	X.30	0…1,7 ms	1,7…3,4	
9,6	X.30	0…0,9 ms	0,9…1,7	
19,2	X.30	0…0,5 ms	0,5…0,9	
38,4	X.30	0…0,2 ms	0,2…0,4	
48	X.30	0…0,2 ms	0,2…0,4	
3	V.110S	0…2,7 ms	2,7…5,4	3.2, 3.6
6	V.110S	0…1,3 ms	1,3…2,7	6.4, 7.2
12	V.110S	0…0,7 ms	0,7…1,3	12.8, 14.4
24	V.110S	0…0,3 ms	0,3…0,7	25.6, 28.8
56	V.13	0…0,2 ms	-	
64	V.13	130 µs	-	
128	V.13	63 µs	-	
256	V.13	32 µs	-	
512	V.13	16 µs	-	
1024	V.13	8 µs	-	

6.16.2.5 PMP Circuit Delay

The total delay of a PMP connection include transport delays consisting of path delay, transit node delay, access delay, bridge delay (data buffer delay of bridge ports) and 106 delay.

Delay components in slave to master direction:

— Delay/km: 5 µs/km; 5 ms/1000 km
— Delay/transit node: 0,4…0,8 ms
— Delay/access node: 0,3 ms

Interfacing and Bridge Delays

Bit Rate kbit/s	Delay ms
≤ 4.8	4
6.0…9,6	2
12…19,2	1
24…38,4	0,5
48	0,4
64	0,8
128	0,5
256	0,5
≤ 512	0,5

6.16.2.6 Example of a PMP Circuit

Below is presented an example of a PMP circuit topology. The symbols used in the figures are explained in the following figure.

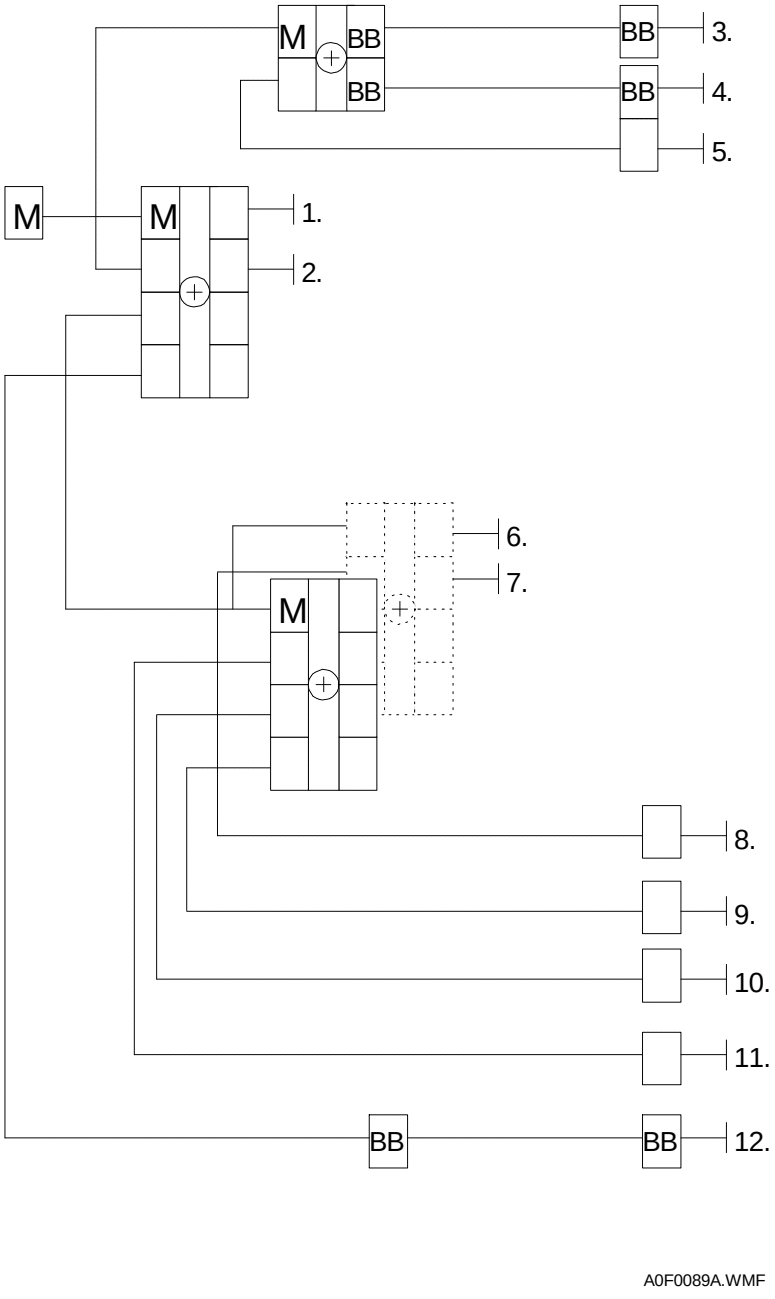


Fig. 135: Example of PMP circuit topology

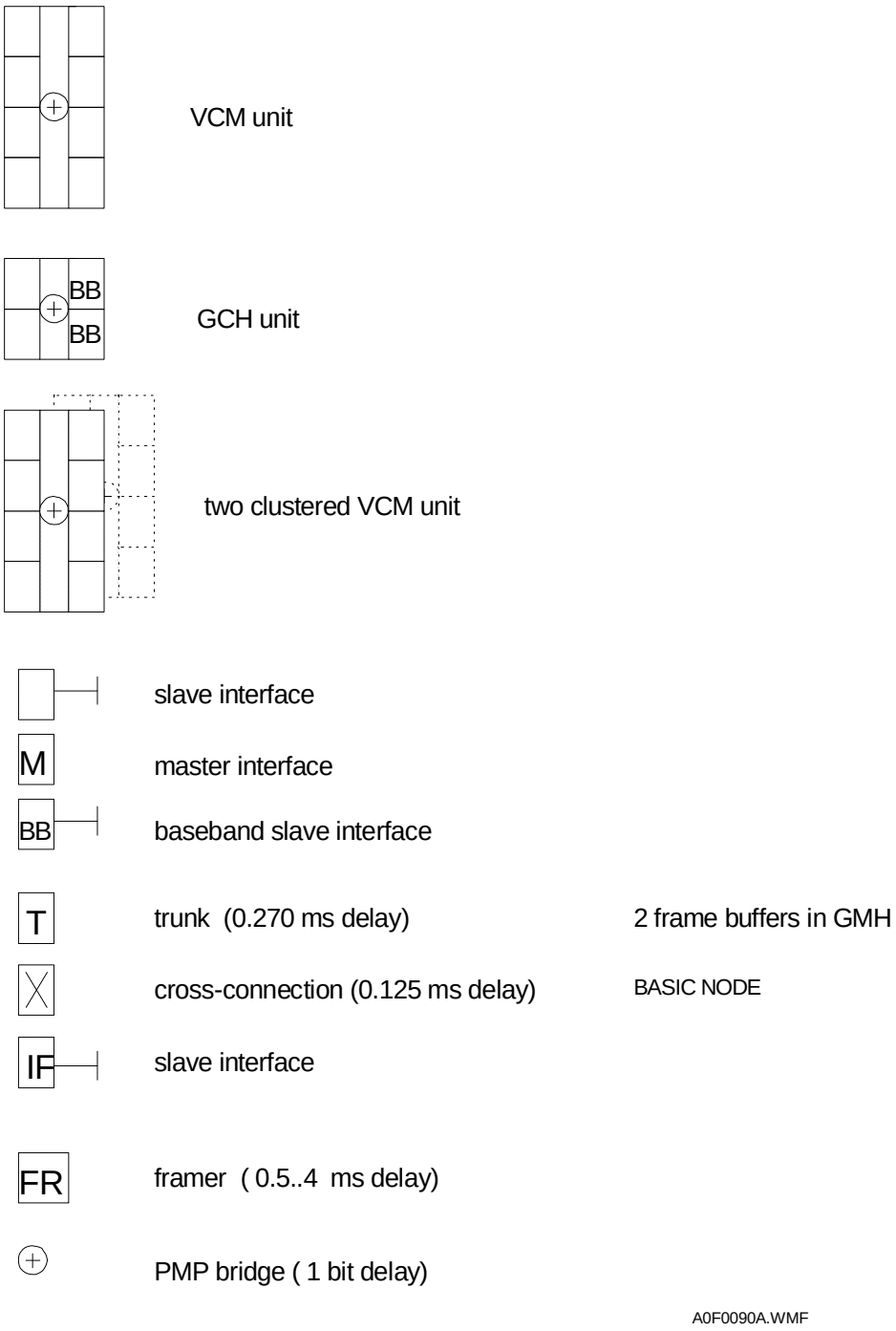


Fig. 136: Explanation to symbols

This topology is "drawn out" in master to slave direction in Fig. 137, Fig. 138 and Fig. 139 and in slave to master direction in Fig. 140, Fig. 141 and Fig. 142. In these figures a data delay is shown in both directions and required 106 delay in slave to master direction.

6.16.2.7 Master to Slave Direction

Because the data from master to slave is broadcasted, there is only one pair of framers between master and slaves. Because normally the framers are the main delay source of the circuit, the delays of each master to slave data paths are close to the others.

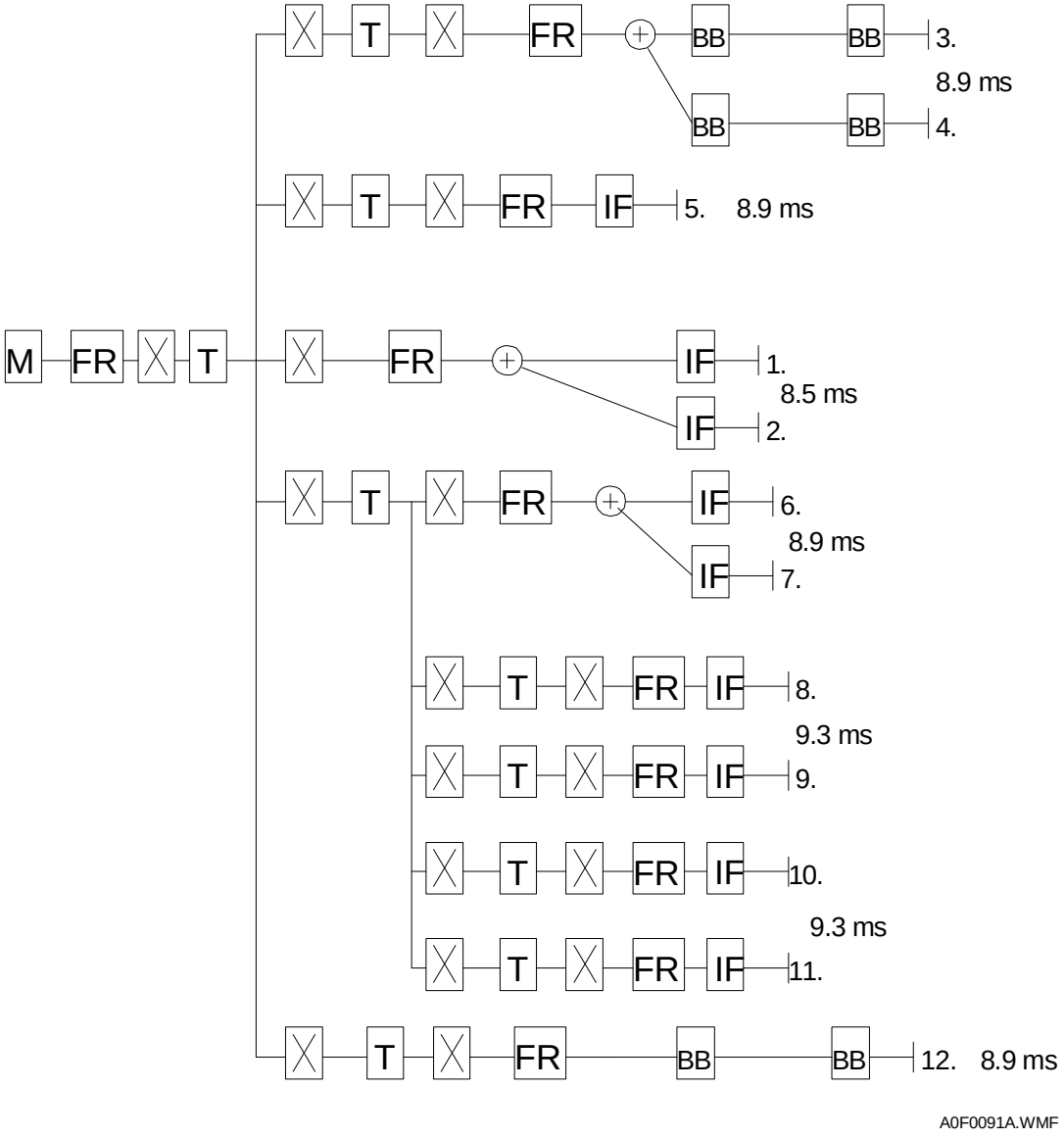


Fig. 137: Master to slave direction at 4,8 kbit/s

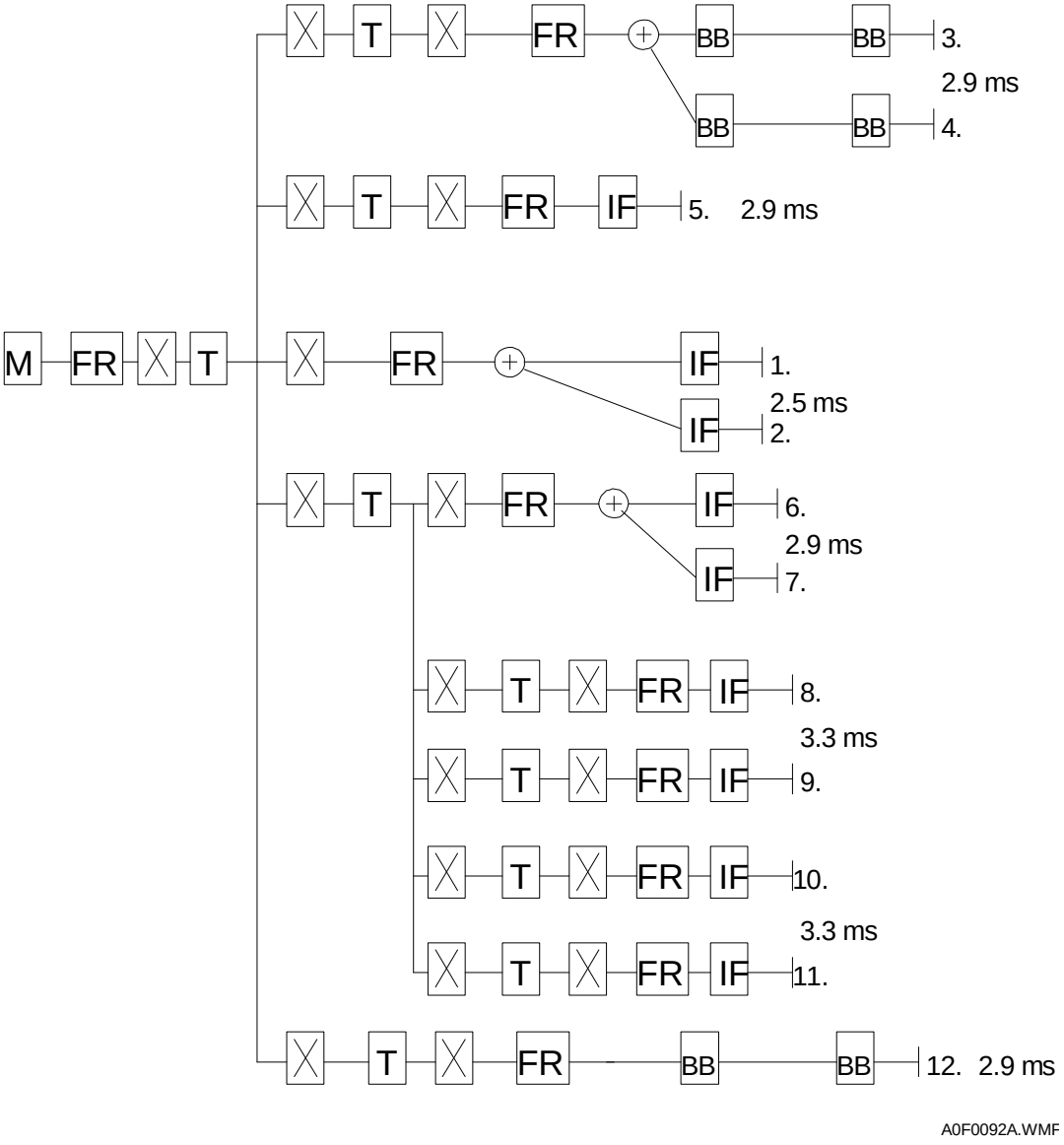


Fig. 138: Master to slave direction at 19,2 kbit/s

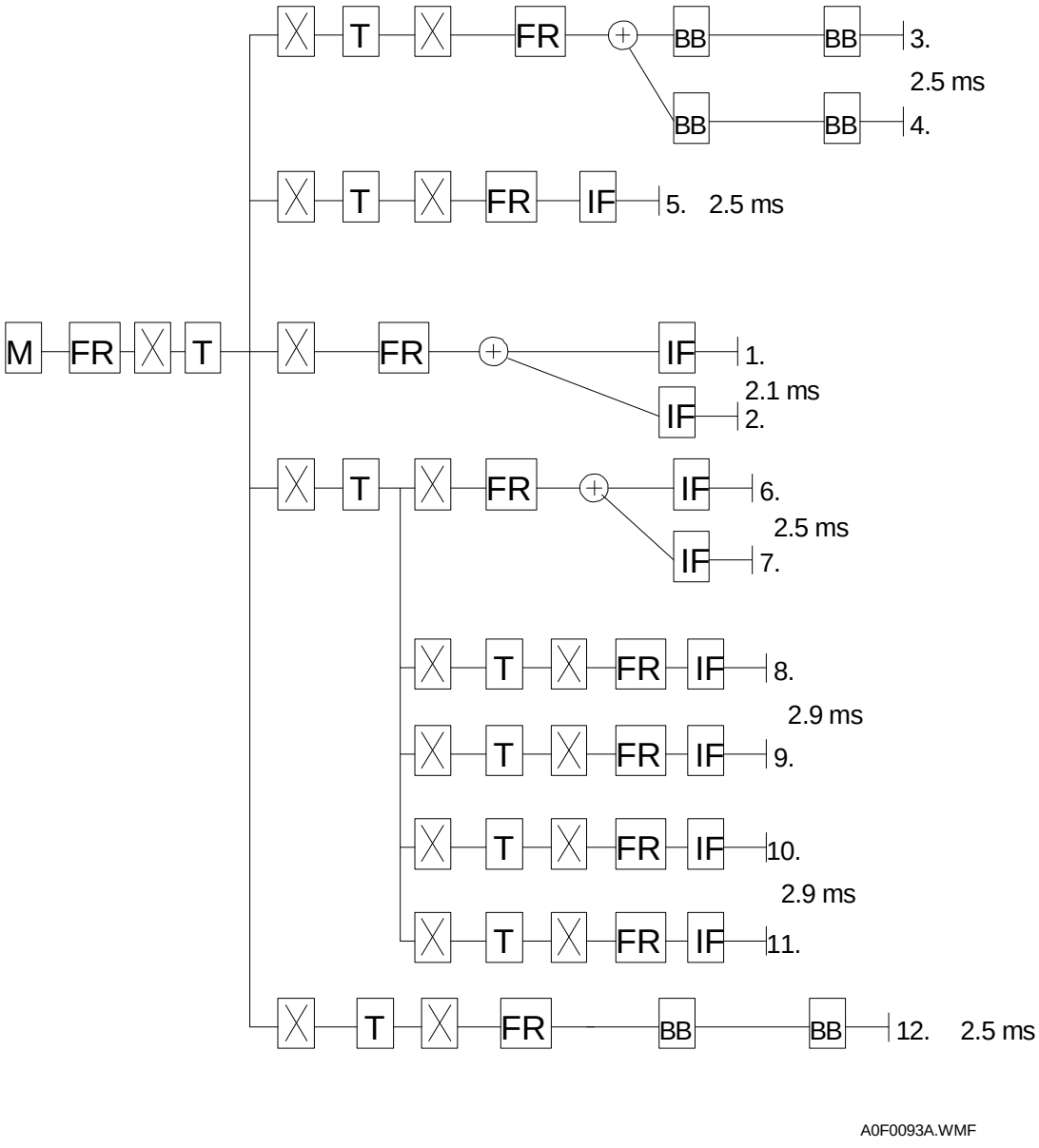


Fig. 139: Master to slave direction at 64 kbit/s

6.16.2.8 Slave to Master Direction

There is a different number of framers between each slave and master, so the delays differ from others. Slaves 1 and 2 have the smallest data delay (2 framers) and slaves 5, 8, 9, 10, 11 have the greatest data delay (6 framers). The delay of the slaves 3, 4, 6, 7 and 12 (4 framers) is between these two.

Slaves 8, 9, 10 and 11 need more 106 delay, because there is a PMP cluster between master and slave. (Note that slaves 6 and 7 are local interfaces of the PMP cluster and they need no extra 106 delays).

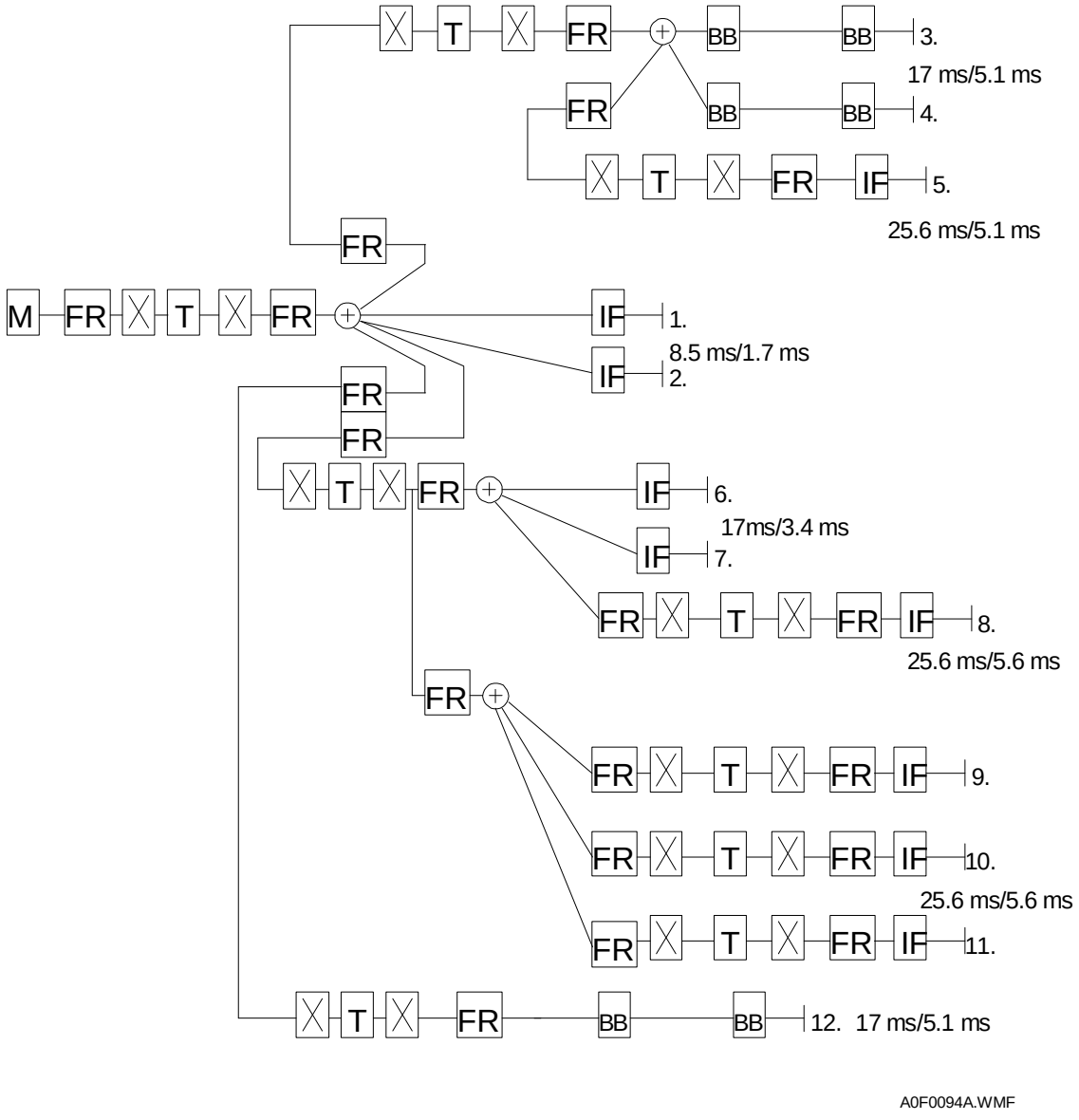


Fig. 140: Slave to master direction at 4,8 kbit7s

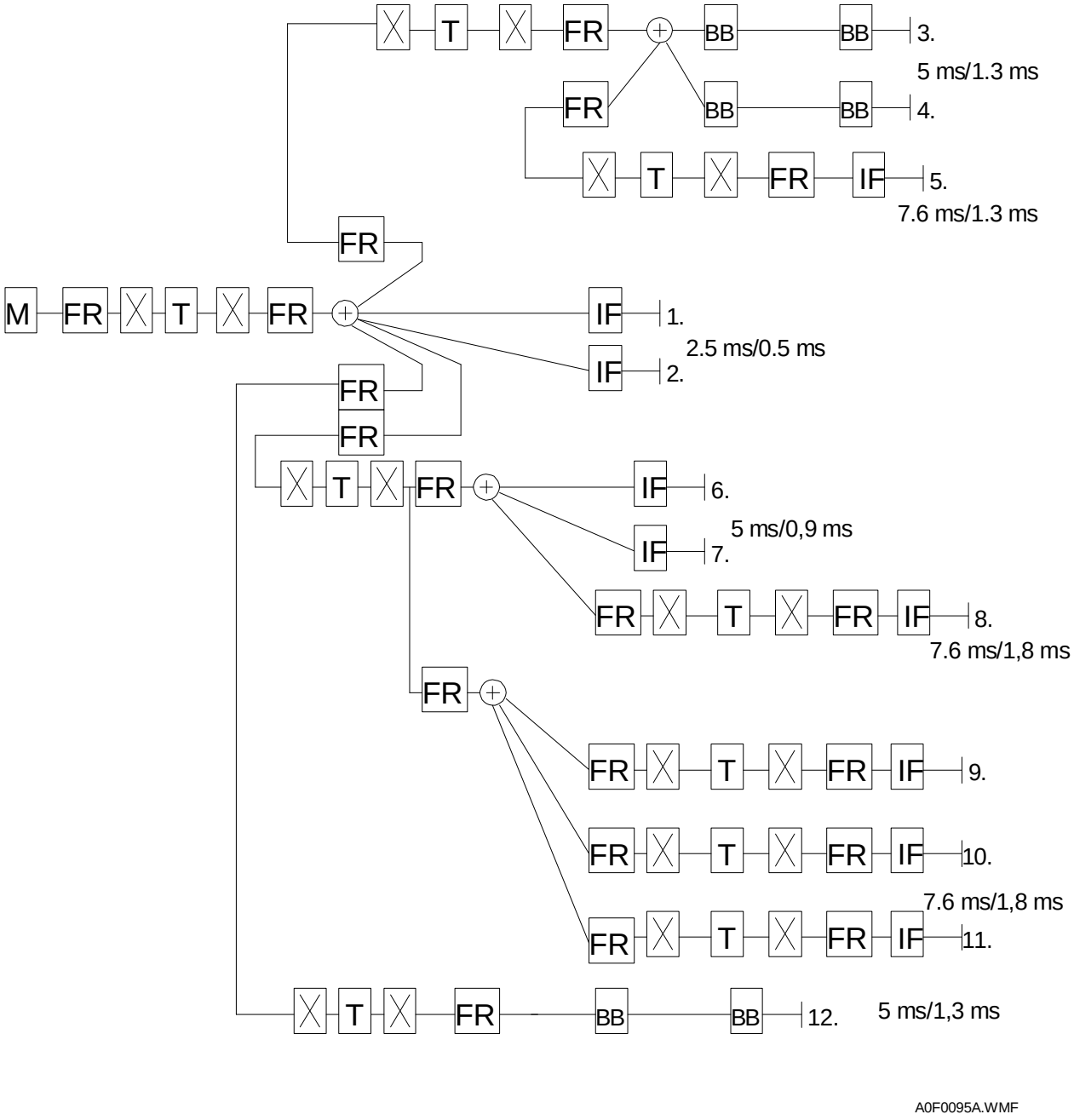


Fig. 141: Slave to master direction at 19,2 kbit/s

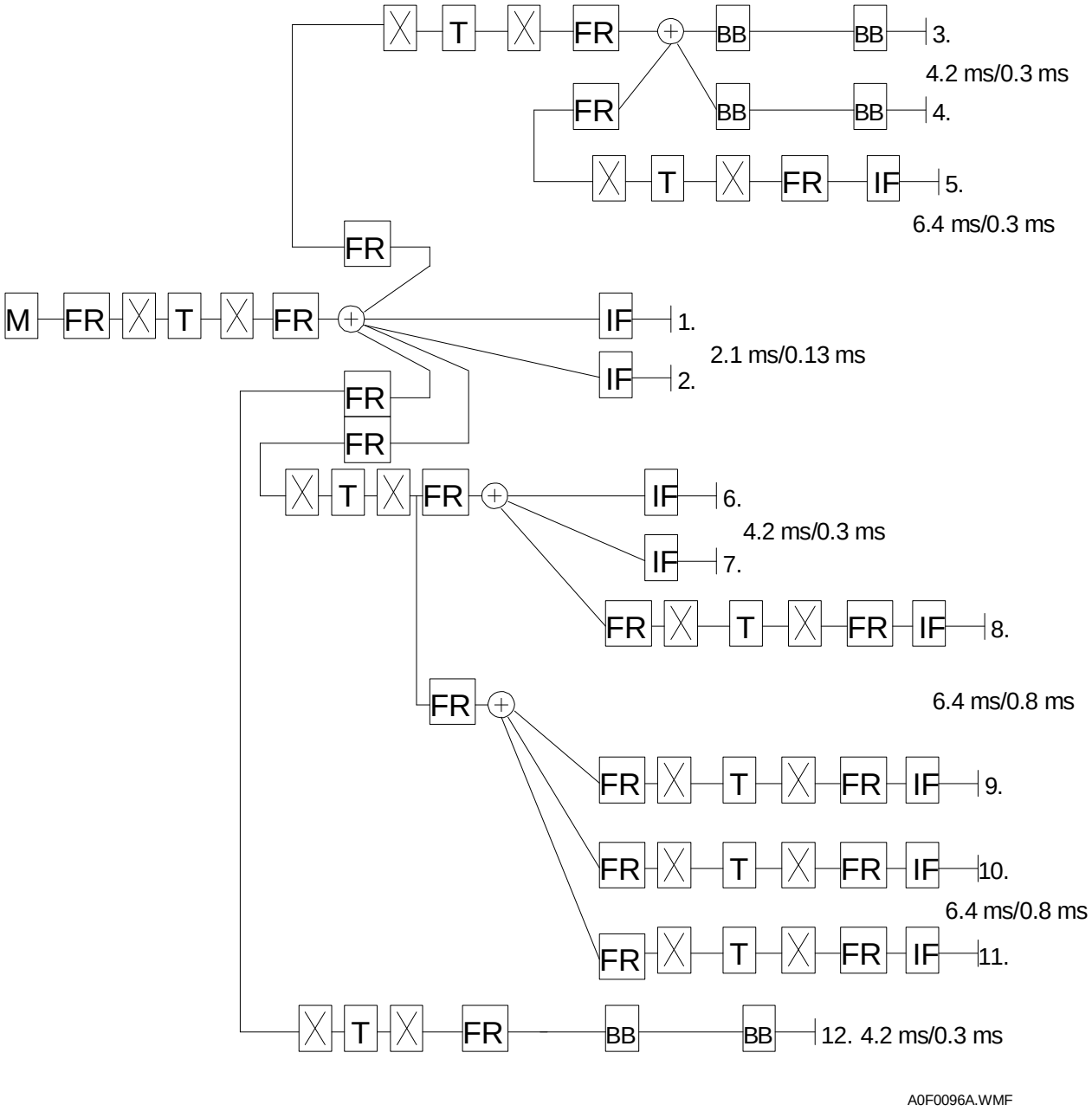


Fig. 142: Slave to master direction at 64 kbit/s

6.17 QMH G.704 Framed Interface Unit

6.17.1 General

The QMH unit processes framed signals at 2048 kbit/s. The unit includes four transmission channels to carry data and also to provide an internal communication link of the DXX system. Transmission channel interfaces may be G.703 interfaces.The frame structure is in accordance with G.704. footnote: For the valid date of any ITU-T/CCITT Recommendation please refer to Chapter 6 section on Relevant Recommendations.

Compared to GMH, QMH has the same features at 2048kbit/s speed, except no measurement point and 1+1 protection is available for interfaces 1 and 2 only. One module comprising of four interfaces can be assembled.

6.17.1.1 Mechanical Design

The mechanical design of the QMH unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; the general recommendations for subrack equipping should, however, be followed.

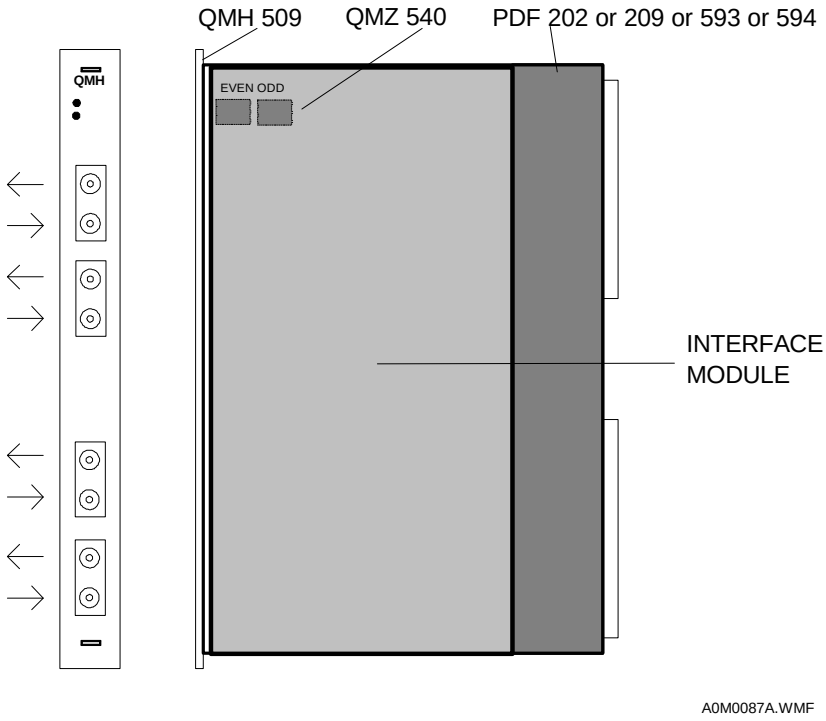


Fig. 143: QMH Unit Equipped with G703-75-Q

The minimum configuration of the QMH unit consists of a unit power supply PDF 202 (-48V) or PDF 209 (-24V) or PDF 593 (-48V) or PDF 594 (-24V) program memory QMZ 540 and a QMH unit interface module for all four channels.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

6.17.1.2 Functional Structure

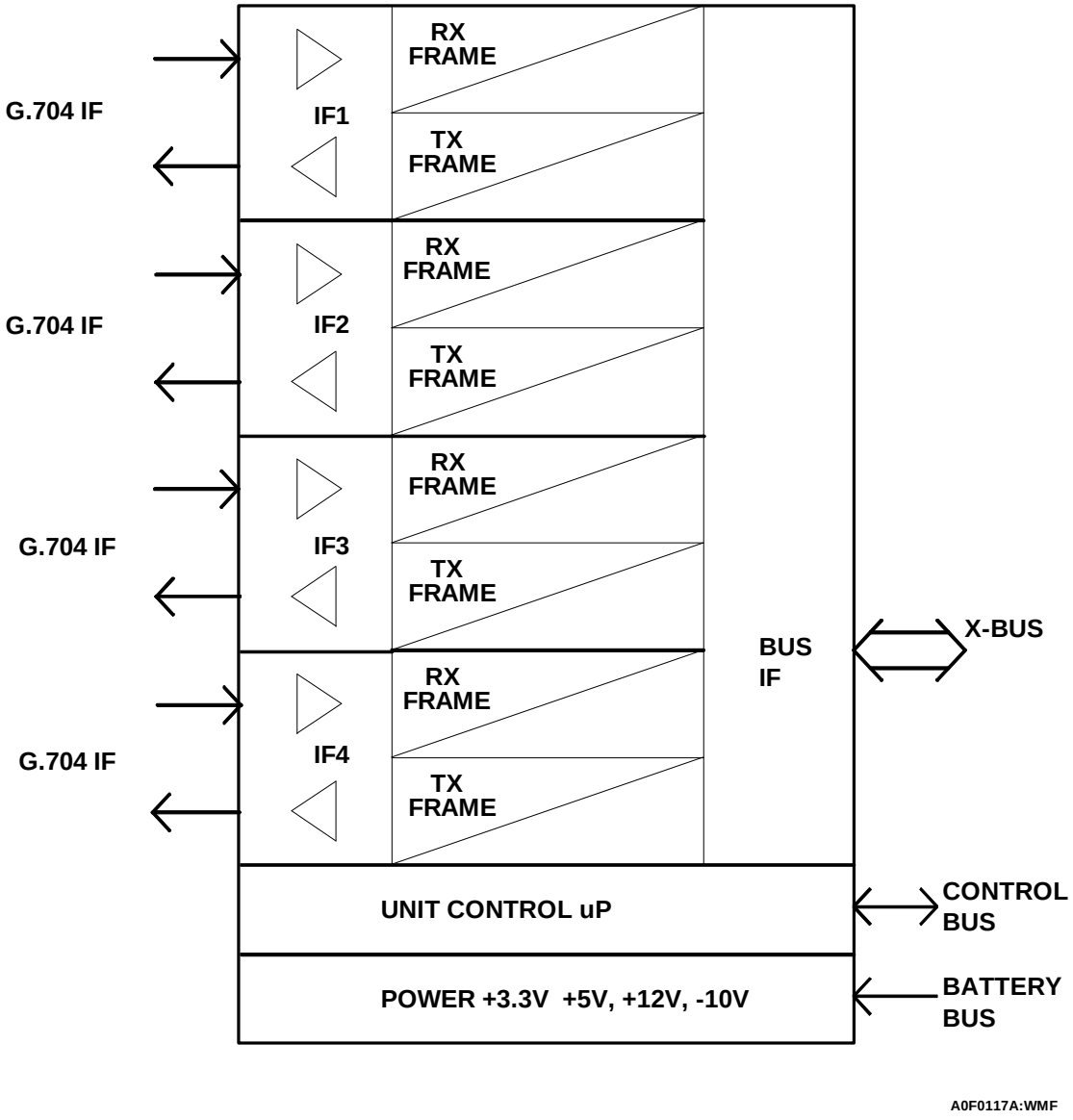


Fig. 144: Functional Structure of the QMH Unit

The main functional blocks of the QMH unit include the power supply, the processor and its peripheral circuits, line interfaces for four channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for all channels.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analog line signals to/from signals suited for the unit's digital circuits. In the transmitting direction data pulses are created in a form suitable for transmitting in the required format. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx frame and Rx frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC check sum, and by generating the HDLC channel at a required position within the frame, with the aid of the processor. In the receiving direction the Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the Rx-frame block can extract the data transmission time slots, check the CRC check sum, and recover and supply the HDLC channel to the processor. The frame structure at 2048 kbit/s speed is in accordance with G.704. If required, it is also possible to remove the framing and have the channel to operate in a transparent mode.

The transmit buffers of the channels are used to store data received from the cross-connect through the X-bus, so that there is always a time slot available for transmit by the Tx frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that the required time slots are always available to the cross-connect unit. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation slips are desired to occur as seldom as possible.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

6.17.2 Operation

6.17.2.1 Unit Operation

Power Supply

A unit receives its operating voltage from the power supply module PDF 202, PDF 209, PDF 593 or PDF 594. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. PDF 202 or PDF 209 provides the operating voltages +5V, +12V and -10V. PDF 593 or PDF 594 provides the operating voltages +3, +5V, +12V and -10V. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

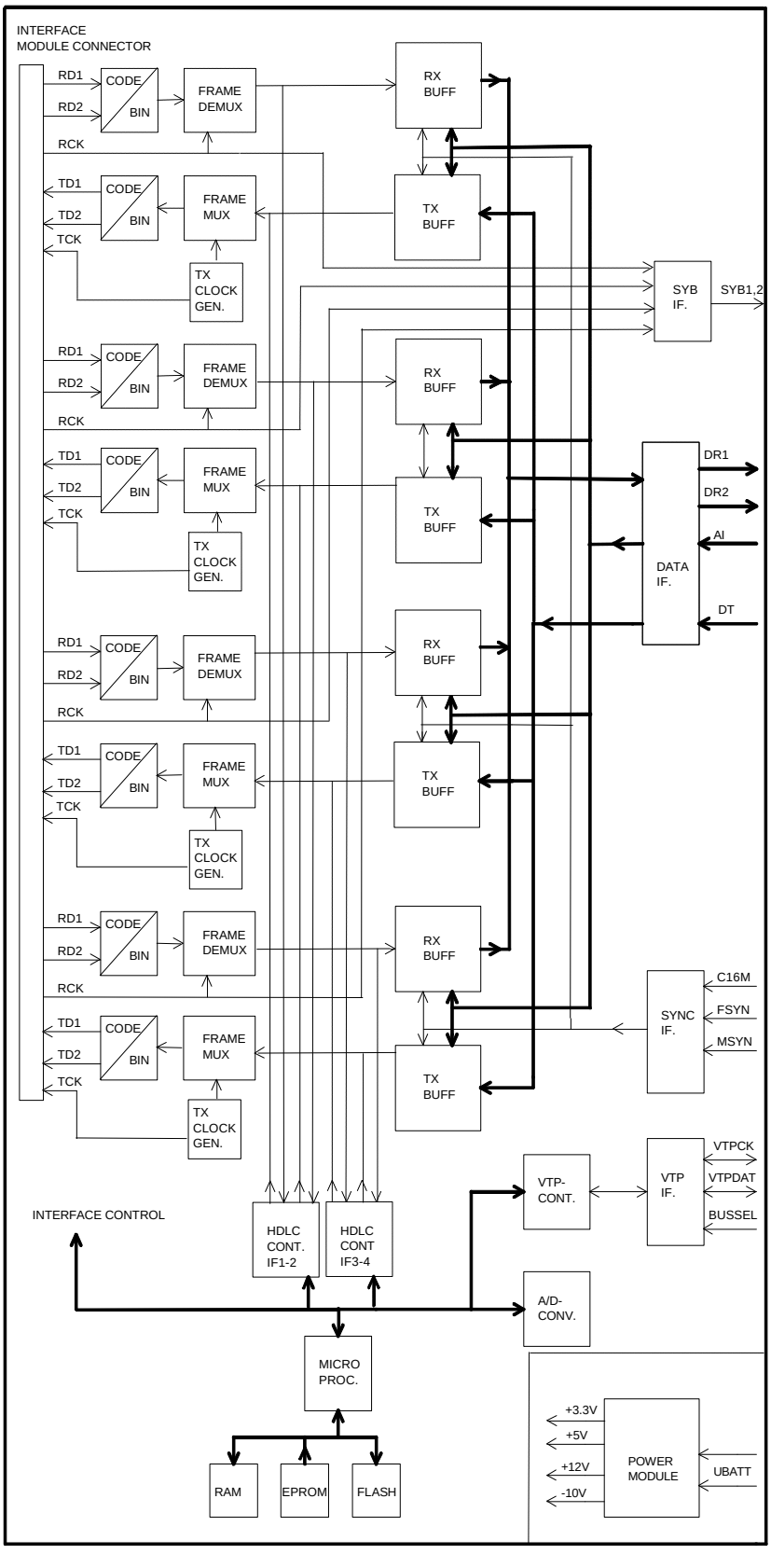


Fig. 145: Functional Block Diagram of the QMH Unit

Processor

The unit is controlled with an 80C186 microprocessor. The program is stored on the board in an interchangeable EPROM memory identified as QMZ 540. A part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM memory of the processor operates as a working storage containing i.e. error counters and data buffers for the HDLC-links and the frame control bus.

Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

A/D Converter

The unit includes a multichannel analog to digital converter (A/D) which monitors the operating voltages and also the control voltage from the interface module connectors.

Module Interfaces

A unit is connected to a transmission line through interface modules. The interface modules contain the analog components required for the interface and also the analog components needed to generate input and output clocks. The signals between the unit and the interface module are digital signals which are converted to the transmission line level in the module. Line code is coded/decoded in the unit.

The processor bus is connected to interface module connectors. Through this bus it is possible to detect the module type and to read data regarding the module status, regarding a missing incoming signal, for example. Parameters which define the module functions, e.g.looping commands, can be selected through the bus.

In the receiving direction the interface module regenerates the coded signal received from the transmission line and transforms the signal to the digital level. The module monitors the level of the received signal; if it is too low or completely missing, the module sets an AIS signal to the unit and at the same time it activates a missing signal alarm through the processor bus.

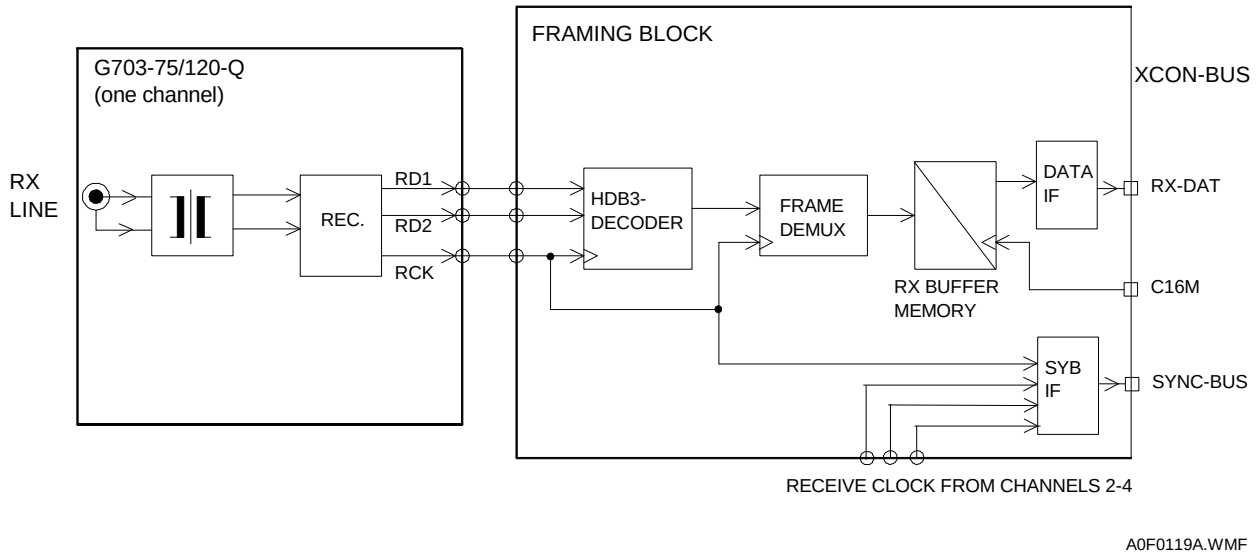


Fig. 146: Data and Clock Processing in the Receiving Direction

The receiving direction clock is recovered from the data in the interface module. The clock is supplied to the unit, which uses it to decode the line code and to demultiplex the frame. If there is no received signal, the interface module replaces the received clock with the transmitted clock.

The received clock from all channels is connected to the SYB interface, where the processor can select a desired clock for either SYB-bus to be used as the frame synchronization signal. The clock to the SYB-bus is disconnected if there is a received signal failure.

The unit generates the frame structure for the data in the transmitting direction. The line code of the data is generated in the unit for G.703 interfaces. The coded digital data is connected to the interface module, where it is converted to a line level signal.

Transmitting direction clock is phase-locked to the C16M frame clock received from the X-bus.

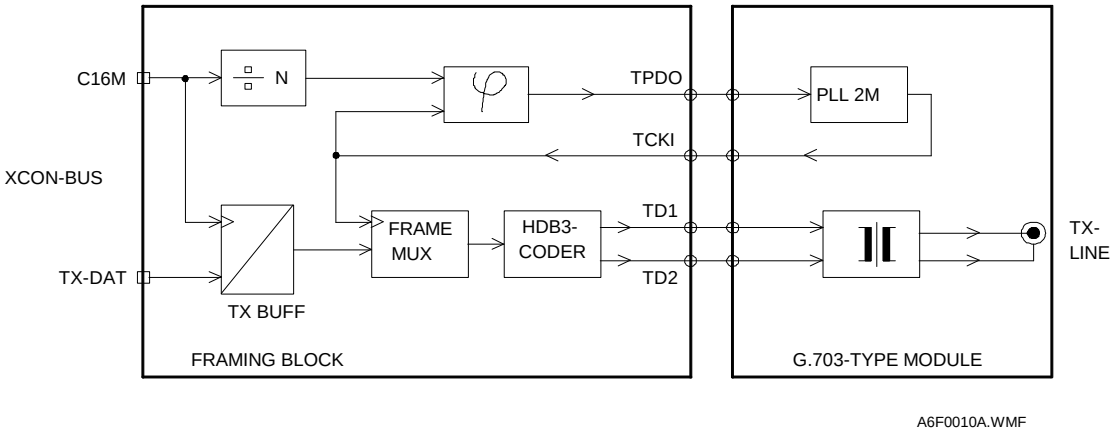


Fig. 147: Transmitting Direction Clock and Data Generation at 2048 kbit/s

The transmitting direction clock for 2048 kbit/s is generated by the phase-locked crystal oscillator of the interface module. The oscillator is locked to the C16M clock of the bus, which is used to create the frame and to generate the output pulses in the coder.

Even if the C16M clock is missing, the output signal is generated with the aid of the clock signal from the interface module crystal oscillator. The phase-locked oscillator will then adjust to its nominal frequency and time slot data in the frame is set to AIS.

6.17.2.2 X-Bus Interface

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with the data bus DR2. The cross-connect unit decides with the aid of the BUS test which bus to use, and this information is supplied to other units through the control bus. From the cross-connect unit the QMH unit receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are monitored also by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure. In the DXX system the frame repetition frequency is always 8 kHz. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. Signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronization by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a HDLC controller connected to framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronization words and the transmitted data channels the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

6.17.2.3 2048 kbit/s Frame Structure

The DXX system utilises a frame structure for 2048 kbit/s according to G.704. The first time slot of a frame, ts0, contains the Frame Synchronization Word (FSW). The bits of this frame synchronization word have a different meaning in odd and even frames. Even frames contain the frame alignment signal and odd frames specify one bit of this word as a frame alignment signal, one bit as the frame far-end alarm bit and five special bits. Four of these five special bits are recommended to be used by the internal HDLC channel of the DXX system. The function of these bits is defined in the user interface through the QMH Parameterization window. However, if CRC check is used, then the first bit in time slot ts0 of every frame is used by the CRC check and cannot be defined for other purposes in the user interface.

The first bit of 16 consecutive time slots ts0 form a CRC multiframe consisting of 16 frames. This multiframe has six frame synchronization bits, eight bits for the CRC check sum, and two bits used to transmit far-end block error information. The period of 16 frames is divided into two subgroups, each consisting of eight frames. A check sum is separately calculated for both subgroups and sent during the next subgroup. The receiving end performs the CRC check, and if a faulty block is detected, then information about this is sent to the far-end by setting the corresponding block error bit to state 0 during one multiframe.

When CAS Channel Associated Signalling is used time slots ts1ºts15 and ts17ºts31 are reserved for payload data transmission. Each data time slot has a corresponding 4-bit signalling word, which is transmitted in time slot ts16 of a multiframe. The bits in time slot ts16 can be utilised by other functions if no signalling capacity is required by a data time slot.

The length of a multiframe is 16 frames. Within the multiframe the first ts16 time slot (in the first frame) is used to transmit the multiframe synchronization word (four bits in the 0 state), the multiframe far-end alarm and three special bits. The function of the special bits can be defined through the user interface. It is recommended to set these bits in state 1 when they are not used. The ts16 time slots of the other frames carry signalling data for two time slots each, four bits for each data time slot. For example, ts16/Fr1 carries signalling data for the time slots ts1 and ts17.

An HDLC channel can be placed in any free time slot where it can occupy a required number of bits. A time slot bit can carry 8 kbit/s of data, and thus the total capacity of the 8 bits in a time slot is 8 x 8 = 64 kbit/s. It is, however, recommended to locate the HDLC channel in the bits B5, B6, B7 and B8 of the time slot ts0. Due to the frame alternation the time slot TS0 capacity is only 4 kbit/s per bit, and these four bits together provide a 16 kbit/s transmission channel. If the HDLC channel is located in bit B1 of time slot ts0, replacing the CRC check, then no other bits can be used to form the HDLC channel.

Frame Multiplexing and Demultiplexing at 2048 kbit/s

A frame to be transmitted is multiplexed in the Frame Mux and clocked by the Tx clock. The data to be transmitted is received through the X-bus into a transmit buffer, from which the Frame Mux fetches data, one time slot at a time, controlled by the bus frame clock. The time slot ts0 can also be received via the transmit buffer from the bus, but usually the frame alignment signal is generated in the Mux. The other bits for the ts0 are read into the transmitted frame from positions defined through the user interface. E.g. the HDLC channel data is received from the HDLC controller in serial form and clocked by the Tx clock. The data for the first frame in the signalling multiframe is generated in the Mux and the time slot signalling data is received via the transmit buffer from the X-bus. Before the frame is transmitted, a CRC check sum is calculated and the CRC multiframe structure is placed into the first bit of time slot ts0.

The receiver will search for the frame alignment signal in the received decoded signal. When the alignment is found at the correct position in consecutive frames, the receiver is synchronized and the frame demultiplexed. The frame alignment search is performed in accordance with a state diagram which should ensure that the receiver will be correctly synchronized even on noisy connections.

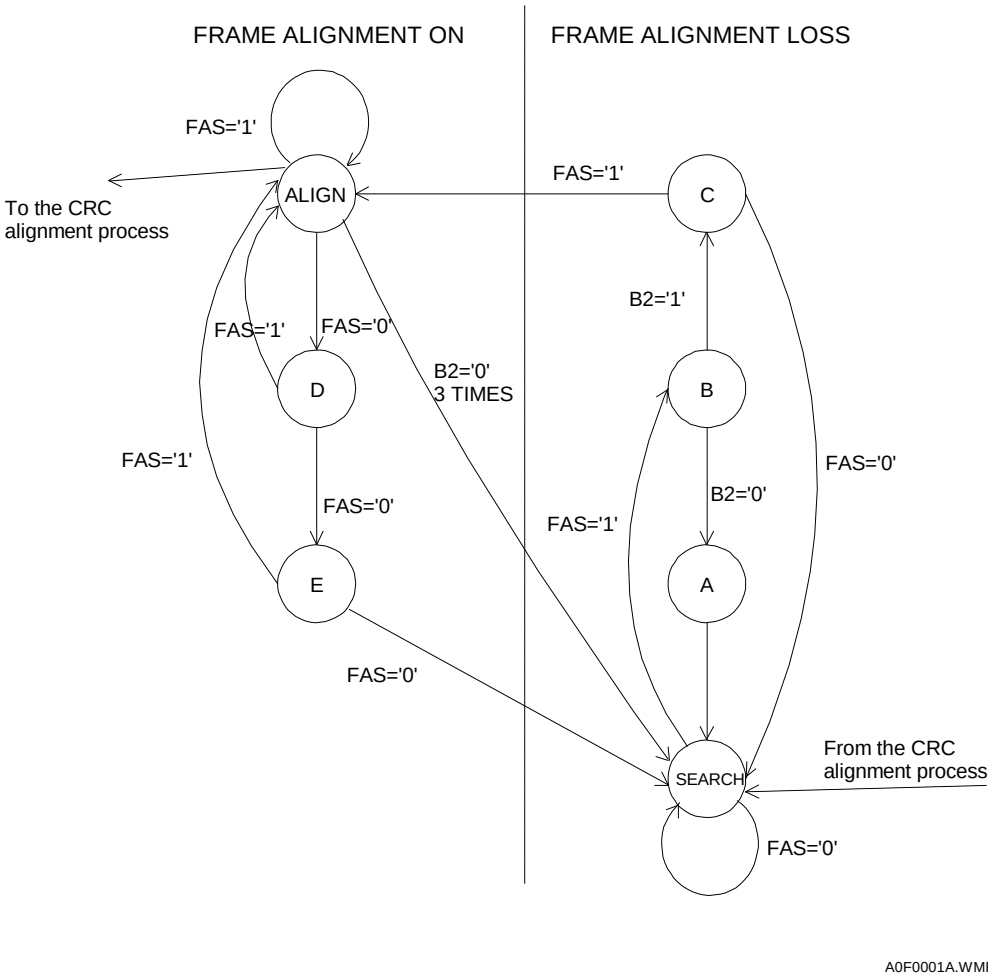


Fig. 148: Frame Alignment State Diagram at 2048 kbit/s)

The right-hand side of figure 0-8 shows the states in the search mode: the frame alignment alarm is activated and the data to the X-bus is set to AIS. On the left-hand side the receiver is synchronized to a received frame and the alarm is inactive. In the search mode the correct frame synchronization word must

be found, thereafter the time slot ts0 in the next frame must have the bit B2 in state 1, then the frame synchronization word again has to be in the correct position in the next frame, and only then the frame is synchronized. If any of these conditions is not fulfilled, the search is repeated from the beginning. When the frame is synchronized, the frame alarm is inactivated and at the same time the AIS is removed from the data supplied to the X-bus.

When the frame alignment is found, the receiver monitors the received frame synchronization words. The frame alignment is considered lost if a corrupted frame synchronization word is received in three consecutive frames. In this case the frame synchronization alarm is activated and a new frame alignment search is started. The receiver monitors also the state of bit B2 in time slot ts0 of odd frames. The frame alignment is considered lost if the bit B2 is 0 in three consecutive frames

The number of faulty frame synchronization words is also counted in the receiver in order to calculate the error rate of the connection. Normally, the error rate limit is set to 10E-3. If the error rate exceeds this value, the reception is inhibited and the receiver sets AIS as data to the X-bus and activates the error rate alarm. The error rate is not calculated when the frame alignment is lost.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are less than three bits in state 0 during two frames and a corresponding alarm is activated. The far-end alarm bit is extracted from time slot ts0 in a received frame. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates the functions defined in the alarm table.

In receiver fault situations - if the error rate is too high or if the frame alignment is lost, for instance - the receiver transfers corresponding information to the transmitter which then activates the far-end alarm bit in the transmitted time slot ts0.

The CRC check is used to increase the reliability of frame alignment and to prevent alignment on words only simulating the frame synchronization word. The receiver is synchronized to the first word found to be identical with the frame synchronization word. If this detected word is sent by some data equipment in a data slot and if this word remains the same for a longer period, the receiver can falsely synchronize to this simulating synchronization word. This situation is detected with the CRC check.

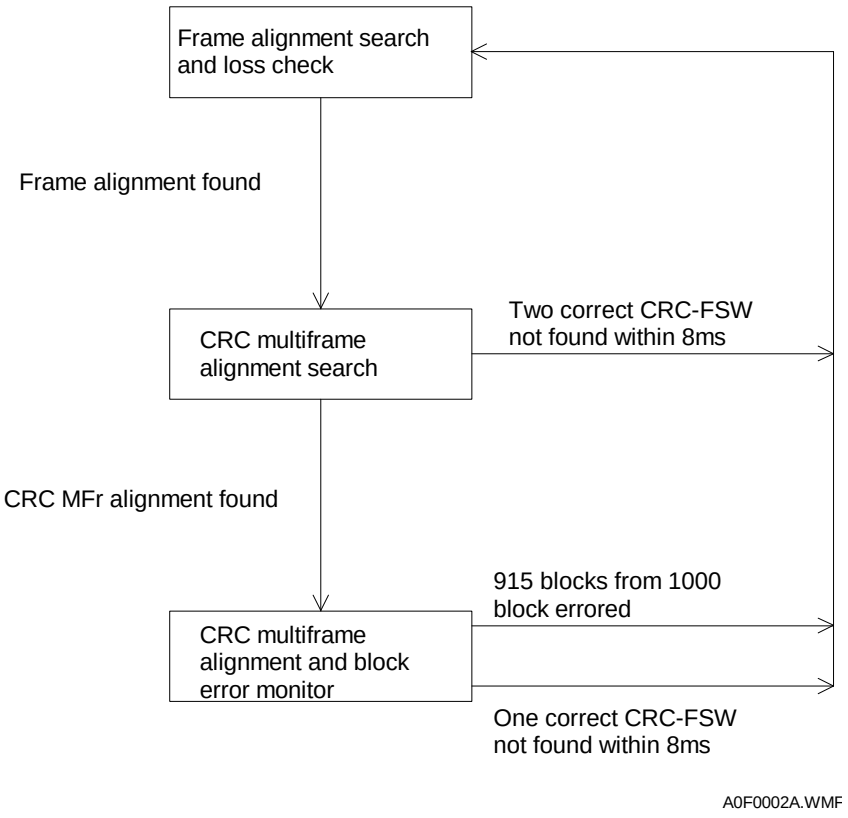


Fig. 149: CRC Multiframe Alignment State Diagram at 2048 kbit/s)

The CRC multiframe alignment state diagram is shown in the figure above. The state at the top contains the 2048 kbit/s frame alignment state diagram. When frame alignment is found, the receiver starts the search for the CRC multiframe alignment signal. The CRC multiframe alignment is found when the receiver finds two correct CRC multiframe alignment signals in the correct position within a period of 8 ms. Then the CRC error count is started. If two CRC multiframe alignment signals are not found within the period of 8 ms, then also a new frame alignment search is started and a frame synchronization alarm is activated.

The receiver starts to count CRC block errors when the CRC multiframe alignment is found. The frame alignment search is started and an alarm is activated if there are more than 914 faulty blocks out of 1000 blocks. The CRC multiframe synchronization words are also monitored: if no correct CRC multiframe synchronization word is found within 8 ms, then a new frame alignment search is started.

The signalling multiframe consists of the time slots ts16 of 16 consecutive frames. The first four bits of time slot ts16 in the first frame form the multiframe synchronization word. These bits are all zeroes (0). The other time slots ts16 contain signalling information for the data time slots.

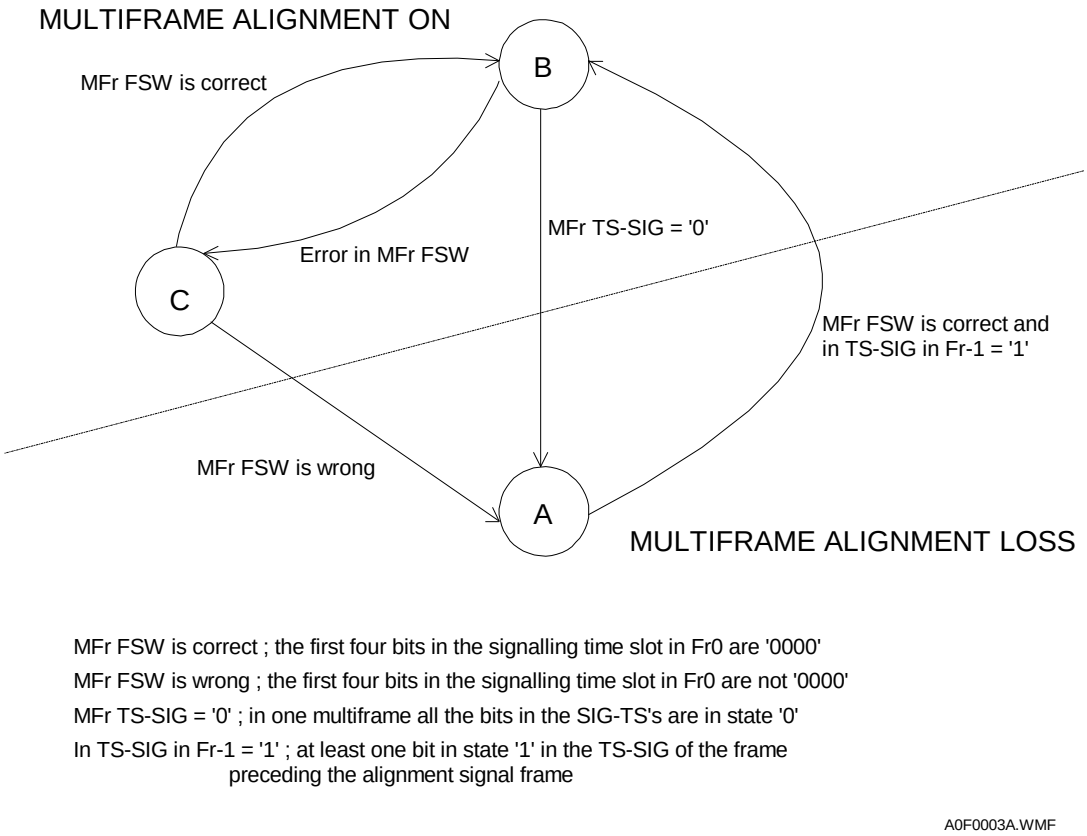


Fig. 150: Signalling Multiframe Alignment State Diagram

The signalling multiframe alignment signal search begins when the frame alignment is found. When the first four bits of time slot ts16 are found to be zeroes (0), this is considered to be the multiframe synchronization word. However, in order to avoid a false alignment it is required that the prior time slot ts16 had at least one bit in state 1. The AIS is removed from the signalling information to the X-bus and the multiframe alarm sent to the far-end is inactivated when the alignment is found.

The multiframe synchronization word monitoring function is started when the multiframe is synchronized. If errors are found in two consecutive synchronization words, the multiframe alignment is considered to be lost. In the synchronized state the contents of all time slots ts16 are monitored, and if all time slots ts16 in one multiframe contain only zeroes (0) the multiframe alignment is considered to be lost. A corresponding alarm is activated if the alignment is lost, the signalling data to the X-bus is set to AIS and the transmitted far-end alarm is activated (ts16/B6).

The far-end alarm is extracted from the received signalling multiframe synchronization time slot. The alarm state is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates an alarm. Through the user interface it is possible to define that the alarm state also puts the signalling data to the X-bus to AIS. In such case the frame far-end alarm bit will also put the signalling data directed to the X-bus to AIS.

If the signalling multiframe synchronization is lost, the received signalling time slot data is monitored in order to detect an AIS. A signal is considered to be AIS if the signalling time slot during one multiframe contains only one bit or no bits in state 0.

6.17.2.4 Buffers

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus, it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control that write and read operations do not simultaneously address the same time slot. In the QMH unit there are two ways to avoid such conflict situations:

1. The transmit buffer length is set to two frames. Then the frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one frame or 125 ms.

2. The read and write operations are performed on the same frame area, but the transmitted frame is synchronized to the bus frame clock and data is written to the buffer in a defined sequence and at a regular speed so that a read/write conflict is effectively prevented. In this case there is only a small frame delay, but the data must be evenly distributed in time slots on the X-bus. The bus has a limited capacity for even distribution: it is reserved for 2048 kbit/s and 8448 kbit/s connections, and it is recommended to use this capacity for trunk lines.

Through the user interface the Rx Buffer can be set to the 2 Fr alternative. In this case the transmit buffer is set to the short form which provides a short delay. The other alternatives create a two-frame buffer.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the cross-connect unit requests data from the interface units through the X-bus, it also specifies the time slot concerned. Usually, the phase of the received frame does not coincide with the frame phase of the X-bus; on the other hand, the receiver writes time slot data into the Rx buffer clocked by the received frame. Therefore the Rx buffer has to control that the read and write operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the QMH unit the centring is made by changing the read address, the change being always one frame or a multiple of a frame. The centring causes a certain number of frames to be lost or re-transmitted; the number is proportional to the distance which the read address is moved. Through the user interface it is possible to select four different lengths for the receiving buffer, in order to meet different requirements, such as a minimum delay or the ability to tolerate large speed fluctuations.

Centring is required when the equipment is powered up, when a received signal contains disturbances, or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

Operating Modes of Buffers			
Rx Buffer	**Rx delay**	**Tx length**	**Tx delay**
2 Fr	0º2 Fr	1 Fr	approx. 0 Fr
4 Fr	1º3 Fr	2 Fr	1 Fr
8 Fr	1º7 Fr	2 Fr	1 Fr
8 Fr Split trunk	2º6 Fr	2 Fr	1 Fr
64 Fr	1º63 Fr	2 Fr	1 Fr

2 Fr Rx Buffer

The length of the receiving buffer is two frames, which provides a minimum connection delay.

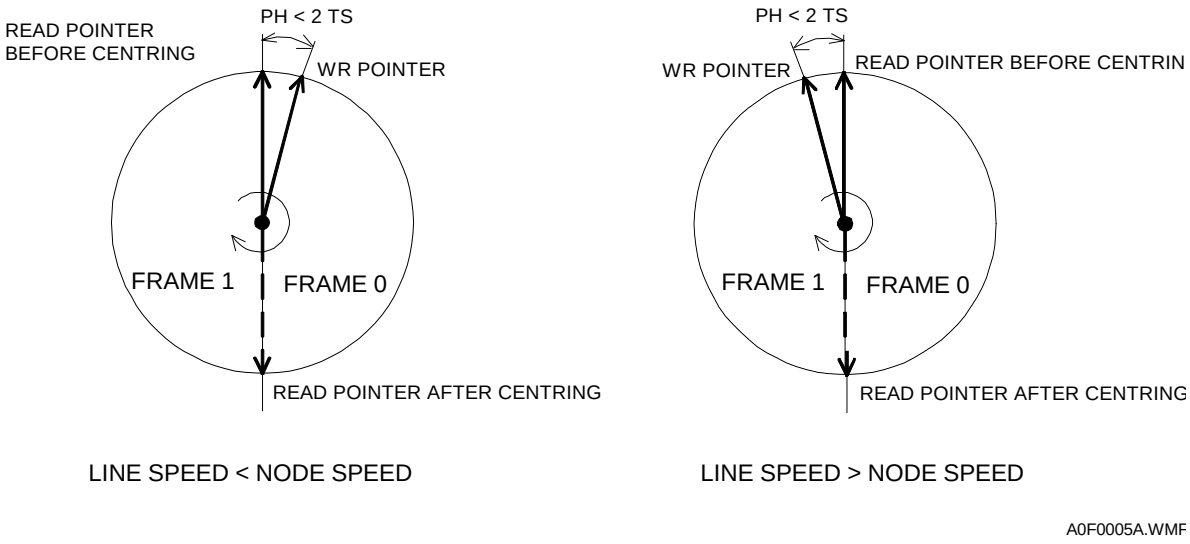


Fig. 151: Centring in an Rx Buffer of Two Frames

In a short buffer the minimum allowed distance between the read and write addresses is one time slot. The distance is checked at intervals of two frames when the read address moves to a new frame. If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. This means that one frame is either lost or repeated once. In a plesiochronous system the distance from the centred position to the position where a new centring occurs is one frame as in figureabove, and the interval between the centring situations is at 2048 kbit/s 240/df, where df is the frequency difference between the signal received from the line and the receiving frequency generated by the X-bus clock frequency.

The short buffer can be used for 2048 kbit/s connection, and then an even distribution is used on the X-bus. This is recommended for trunk lines in order to keep the transmission delays as short as possible.

4 Fr Rx Buffer

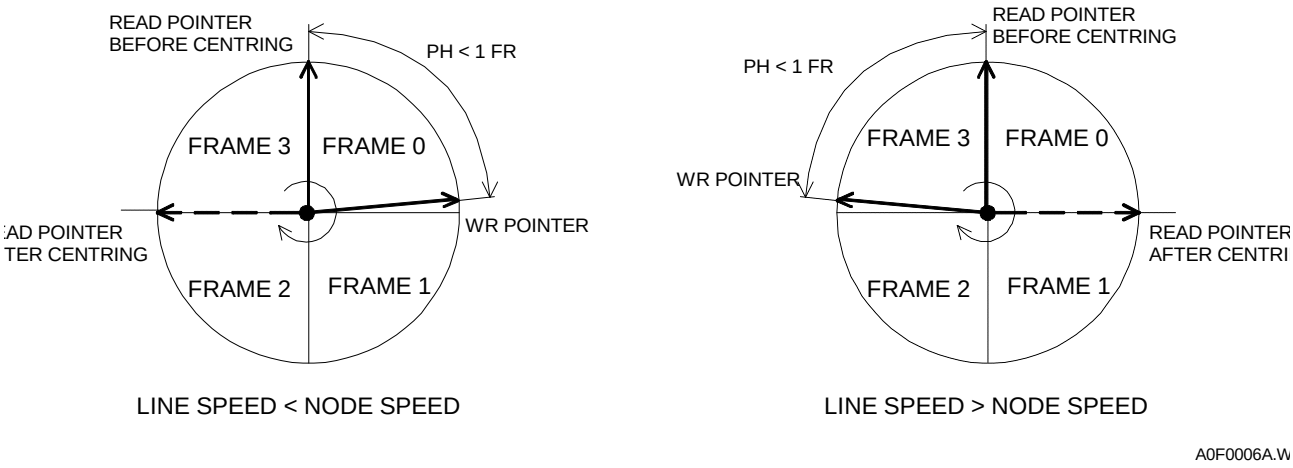


Fig. 152: Centring in an Rx Buffer of Four Frames

The minimum allowed distance between the read and write addresses is one frame. The distance is checked at intervals of four frames when the read address moves to frame Fr0 (from the frame Fr3). If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. The address jump direction depends on the direction from which the write address was closing in on the read address. Centring means here that one frame is either lost or repeated once. In a plesiochronous system with a four-frame Rx buffer the interval between centring situations is at 2048 kbit/s 256/df. It is recommended that the 4 Fr buffer is used for framed user interfaces.

8 Fr Rx Buffer

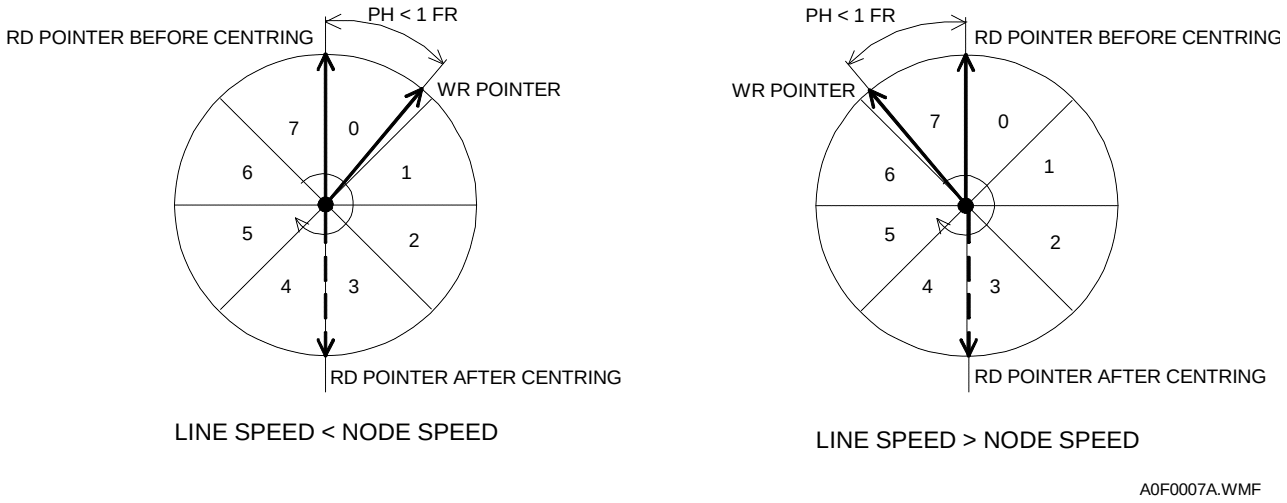


Fig. 153: Centring in an Rx Buffer of Eight Frames

The allowed distance between read and write addresses in an Rx buffer of eight frames is one frame. If a shorter distance is detected by the check, then the read address is moved to a new position four frames farther away. In this case centring means that four frames are either lost or repeated once. The eight frames buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure is used.

The 8 Fr buffer is the only possibility for Split Trunks. The centring for Split Trunks is defined so that the minimum allowed distance between the read and write addresses is two frames. In other respects the centring is equal to the 8-frame buffer's basic mode.

In a plesiochronous system the interval between centring situations is:

at 2048 kbit/s Split Trunk	512/df
at 2048 kbit/s	1024/df

A buffer with a length of eight frames is used for Split Trunk operation. It may also be used for other applications, in particular if unusually large fluctuations have to be handled correctly or if the frame alternation has to be intact also after the centring.

64 Fr Rx Buffer

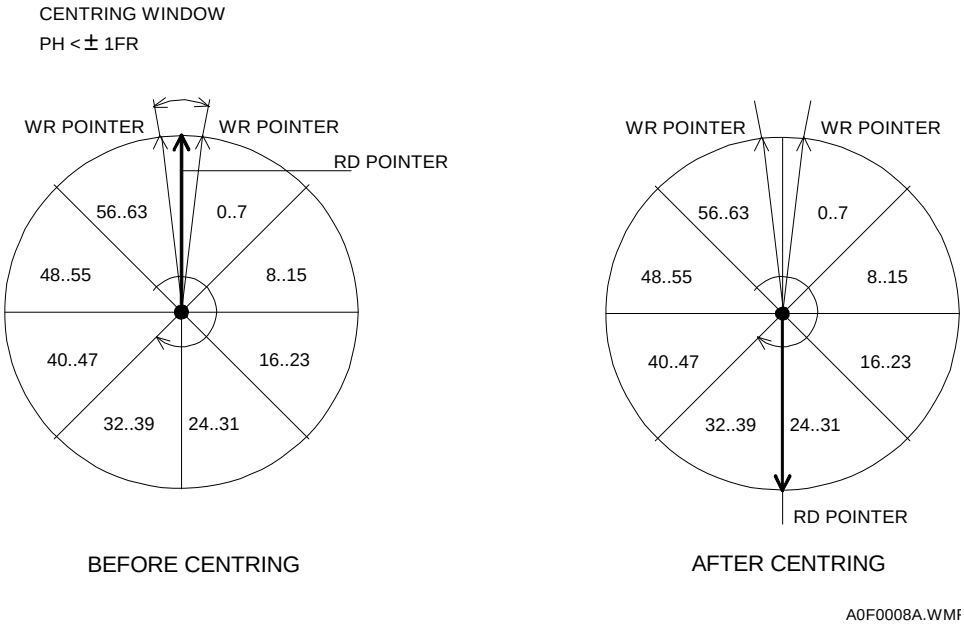


Fig. 154: Centring in an Rx Buffer of 64 Frames

In an Rx buffer of 64 frames a new centring is triggered if the distance between the read and write addresses is less than one frame. Centring means now that 32 frames are either lost or repeated once. The long buffer leads to a delay of up to 63 frames and thus this buffer mode is recommended for special purposes only. The slip distance is very large in a plesiochronous system and the buffer is well suited for large frequency fluctuations.

In a plesiochronous system the interval between centring situations is at 2048 kbit/s 8192/df.

Multiframe Buffers

In the transmitting direction the signalling data is directed through the same buffer as the time slot data. The signalling multiframe of the frame to be transmitted is synchronized to the multiframe clock of the X-bus. The cross-connect unit supplies frame signalling data together with other time slot data of the frame. The QMH unit generates a synchronization time slot in the first frame of the signalling multiframe. Thus the signalling data and time slot data have equal delays in the transmitting direction.

In the receiving direction the phase of the received signal multiframe usually differs from the phase of the X-bus multiframe. Thus the received signalling data has to be buffered until the cross-connect unit performs the cross-connect function for the concerned data. There are two alternatives for the multiframe buffer length: two and four multiframes. The multiframe buffer length depends on the selected length of the frame buffer.

Multiframe Buffers			
Frame buffer mode	**Multiframe buffer mode**	**MFr-Rx delay**	**MFr-Tx delay**
2 frames	2 MFr	0º2 MFr	0 Fr
4º8 frames	2 MFr	0º2 MFr	1 Fr
64 frames	4 MFr	1º3 MFr	1 Fr

The length of a frame is 125 ms; the multiframe length is 2 ms.

In both multiframe buffer modes the centring is triggered if the distance between the received multiframe phase and the X-bus multiframe phase is less than one frame. In a buffer with two multiframes the centring is made by moving the write address one multiframe further, which means that the information of one multiframe is lost or repeated. In a buffer with four multiframes the centring means that the information of two multiframes is lost or repeated.

In QMH and cross-connect units the time slot data and signalling data have separate buffers. Therefore there are different delays in the processing of signalling data and time slot data. This means that the signalling data and time slot data which are placed in a transmitted frame do not necessarily originate from the same frame.

6.17.2.5 QMH Operating Modes

Trunk interfaces and user access interfaces are the two categories of DXX node interfaces. Trunk lines are lines connecting the DXX nodes, and the trunks are always framed interfaces. User access interfaces connect lines from users to a node. The user access interfaces can be channel interfaces or framed channel interfaces. QMH units can be used as trunk interfaces or user access interfaces. The user interface presents a G.704 framed channel interface to the user. The most important difference between the trunk mode and the user mode is that the use of time slots in the trunk interface is determined by the Network Management System whereas the use of time slots in a framed channel interface is determined by the user.

QMH Unit as a Trunk

2048 kbit/s Trunk

When a line is used as a trunk line, a part of the frame is dedicated to transfer internal system information. This information will contain data on e.g. network management channels that use the HDLC format. The transmitter will always regenerate the frame synchronization word and the CRC check in a trunk line.

The framing and CRC check have to be selected when a trunk line connection is established. The corresponding HDLC channel has to be activated and bits B5ºB8 in time slot ts0 are recommended bits for the link. The trunk buffer is short in order to ensure minimal delay trough the node. It is recommended to activate the signalling time slot CAS of the trunk so that it is always reserved for signalling and not used as a data time slot by the Network Management System.

Split Trunk Lines

A split trunk line can be used to combine several parallel 2048 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the n x 64 kbit/s is connected through physically separated cables. The split trunk mode can be used for line speed 2048 kbit/s when a frame with CRC4 is used. The split trunk mode always requires long buffers (eight frames). One of the interfaces will function as a master and the others as slaves. All split components must have same bit rate.

The interfaces are synchronized to each other by their CRC4 multiframe structure. In the transmitting direction the interface transmit buffers and Tx frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will center their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the SXU unit of the receiving node.

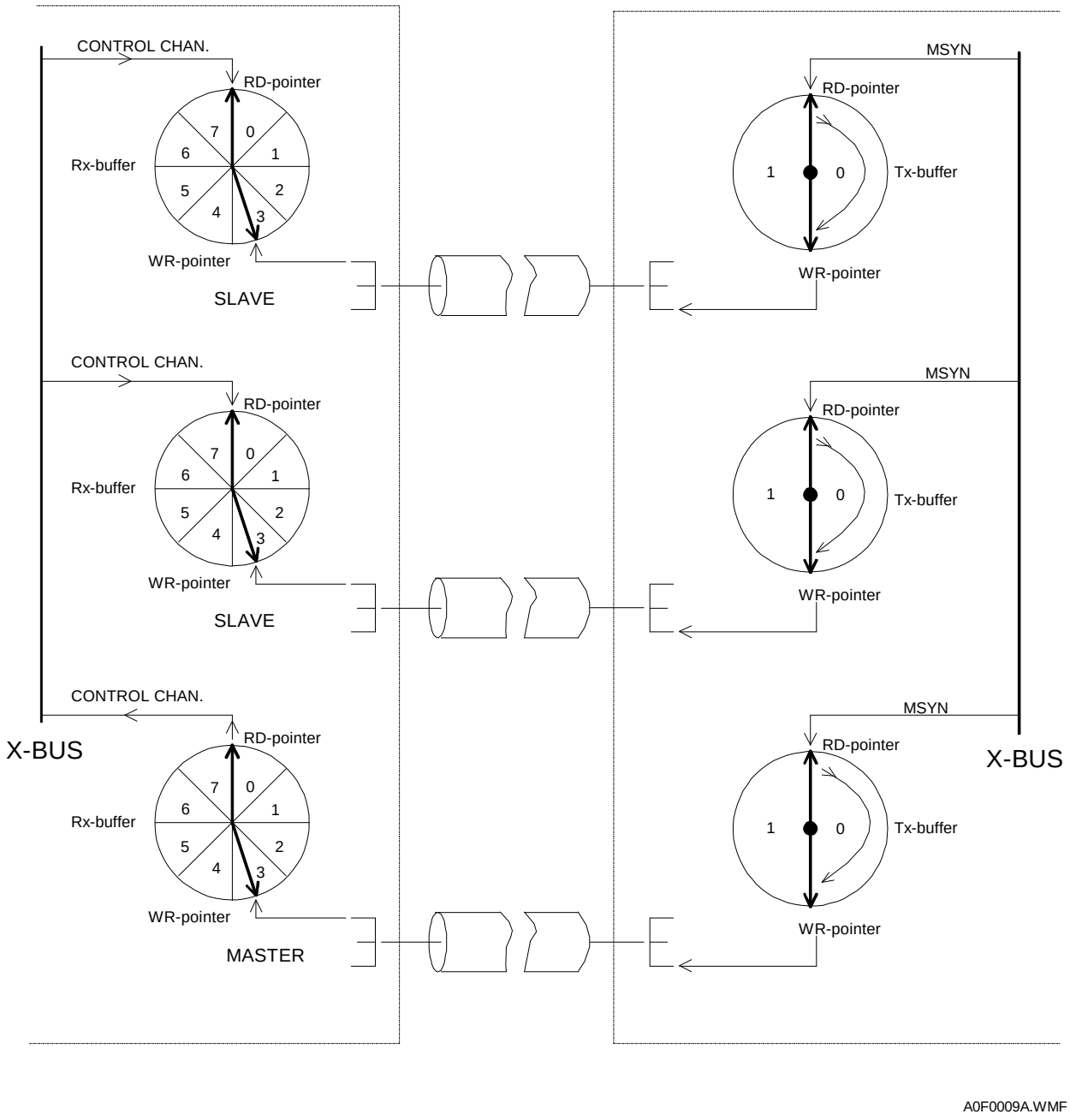


Fig. 155: Split Trunk Line Operating Principle

Theoretically, the maximum delay allowed between lines in a split trunk line is 0.5 frames: due to the centring the master read address occurs when the write address is in the area 6º2. Due to technical reasons, however, the maximum delay is 50 ms.

Each line of a split trunk line will handle its own signalling data. Those lines which carry one or more data channels with signalling data will use the last time slot or ts16 if it is possible as a signalling channel with a multiframe structure. It is not necessary to use a CAS time slot for lines that do not include data channels with signalling.

QMH as User Access Point

The QMH unit can provide a G.704 framed channel interface to the user. The framed user access point has the same features as a corresponding trunk interface. The special bits are used in accordance with customer requirements. There are many possibilities to use the QMH unit as a user access point. Some examples are discussed below.

Framed; With or Without CRC

This is the basic way to connect pieces of equipment which use the G.704 frame structure to a DXX node. Only the data channels in time slots ts1°ts31 is transmitted over the network together with signalling data in the time slot ts16, if required.

The framing structure is demultiplexed at the interface point and only payload data will be supplied to the cross-connect system for further processing. In the transmitting direction the whole framing structure and the frame synchronization word are created in the interface and payload data from the cross-connect is added to the frame. The user equipment to be connected has usually no information about the protocol of the DXX system control channel. Therefore the HDLC channel will not be connected to the interface (with the exception of some DXX system modems). The free bits in time slot ts0 can be set to a state required by the user equipment. The synchronization remote end alarm indication bit RAI may be used, if required by the equipment to be connected. It is recommended to use the CRC check in the interface when the user equipment supports the use of CRC. Some equipment use the CRC E bits in a way not conforming to standards and in such cases unnecessary alarms can be avoided by setting the bits in a fixed state, usually 1.

When individual channel signalling is used, the multiframe structure in the receiving direction is demultiplexed in the interface and the signalling for each channel is transferred to the cross-connect for further processing. In the transmitting direction the multiframe synchronization time slot is created in the interface and stuffed with free bits. Signalling data from the cross-connect is placed into the signalling time slot. The free bits usually have the Permanent 1 state. If no signalling is used, then also time slot ts16 may be used to transmit payload data.

Framed; Transmission of Free Bits in ts0 Through the Network

It is possible to transmit the free bits of time slot ts0 through the DXX network when the equipment connected to a DXX node can utilise these free bits. Other functions may be the same as in the previous example. The free bits of time slot ts0, which are utilised by the application and transmitted through the network, are set to the X-conn state when the QMH unit parameters are defined. The unit will then transmit these bits in the same state as it receives them from the cross-connect. Accordingly, bits received in time slot ts0 are supplied to the cross-connect in the same state as they are received.

On the transmission line the data transmission capacity is 4 kbit/s for one free bit in time slot ts0 due to the frame alternation. The total data transmission capacity of all five bits B4ºB8 is thus 20 kbit/s. However, the DXX system utilizes a format where one free bit of time slot ts0 uses a capacity of 8 kbit/s on those connections on which it is transmitted through the network. Thus, a total capacity of 40 kbit/s is required to transmit all bits B4ºB8 through the network. Transmission of the free bits of time slot ts0 always uses 64 kbit/s of the DXX node internal X-bus capacity for each interface, regardless of the number of transmitted bits.

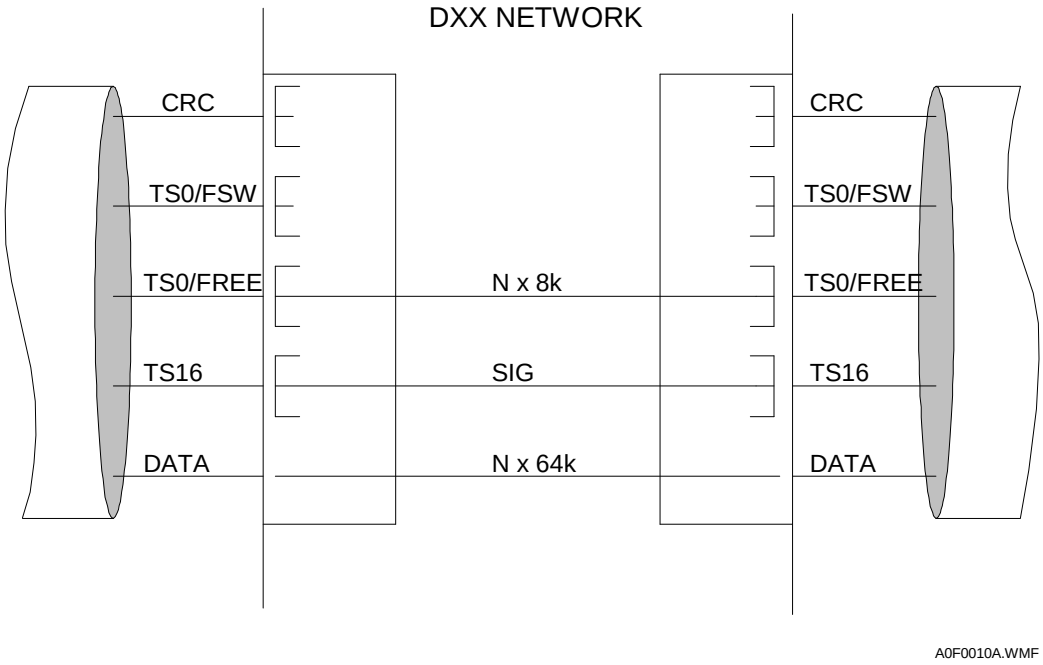


Fig. 156: TS0 Free Bits Connected Through the Network

Framed; Transmission of Time Slot ts0 Through the Network

It is possible to use the frame synchronization word to monitor the complete connection through the DXX network. In this case the whole time slot ts0 is directed via the cross-connect and transmitted to the far-end equipment. In this case the frame synchronization word, the free bits of time slot ts0 and the frame remote end alarm are transmitted over the whole connection. If it is required to connect signalling data separately over this connection, then the CRC check has to be regenerated in the user access interface. A new CRC check sum has to be calculated because the frame contents will change due to the different treatment of signalling data and normal data. The CRC check may be inactivated when the user equipment does not support the use of CRC.

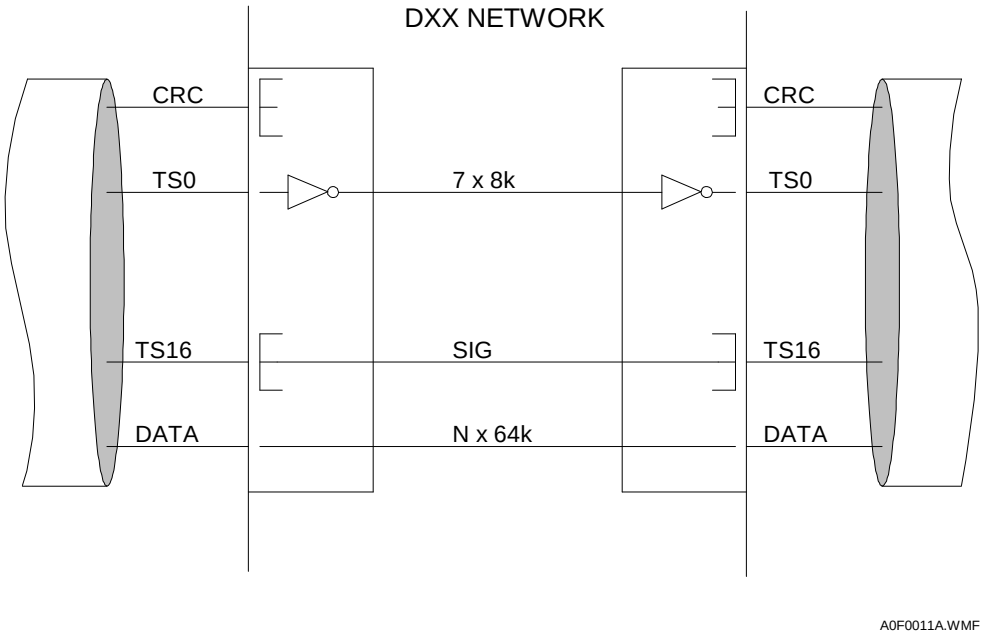


Fig. 157: Ts0 Connected Through the Network

When it is connected to the transmission network, the time slot ts0 is inverted in the receiver before it is forwarded to the cross-connect. The time slot is in the inverted state when it is transmitted through the network, and in the far-end user access interface it is again inverted into its original format and then added to the frame as the synchronization time slot. The time slot ts0 is inverted so that it cannot cause false synchronization of the trunks when it propagates through the network. A trunk capacity of 56 kbit/s is used in order to transmit the whole time slot ts0 through the network. The transmission of the time slot ts0 uses 64 kbit/s of DXX node internal X-bus capacity for each interface.

When the interface parameters are set (during commissioning), the Fault consequence BER 10E-3 should be set Off. This causes received data with a bit error rate worse than 10E-3 (calculated with the aid of the frame synchronization word) to be connected through the network, and not to be set AIS as in normal transmission.

When the time slot ts0 is transmitted through the network, the user access interface will respond to errors in a way that is different from the normal. The remote end frame level alarm bit is not activated when the user access interface receiver detects a serious frame error, because this error will cause the remote end user equipment to respond, e.g. through the AIS, and to activate the remote end alarm bit. The remote end alarm bit is then transmitted back to the near-nd user equipment. Moreover, the QMH unit will not respond to a received FrFEA bit. If an interruption occurs in the transmission network and an AIS is given instead of a payload signal to the interface, then this condition will be detected in the transmitter and an AIS is sent to the user equipment. The interface simultaneously activates the AIS from X-bus alarm.

Framed; Ts0 and CRC Connected Through the Network

It is possible to monitor the quality of the user's connection over the whole network with the aid of the CRC check. To enable this, a combination of the time slot ts0 and the CRC check is sent through the network from the near-end user equipment to the far-end user equipment. The CRC check sum is calculated for the total signal. In order to get equal results in the unit creating the CRC check sum and in the unit evaluating the CRC check sum, all bits must have the same state at both locations. The receiver will receive signalling data and payload data through different delays, and therefore it is not possible to use cross connected channel signalling, if the CRC check is transmitted over the connection. The idle data of possibly unused time slots has to be the same at both ends of the connection.

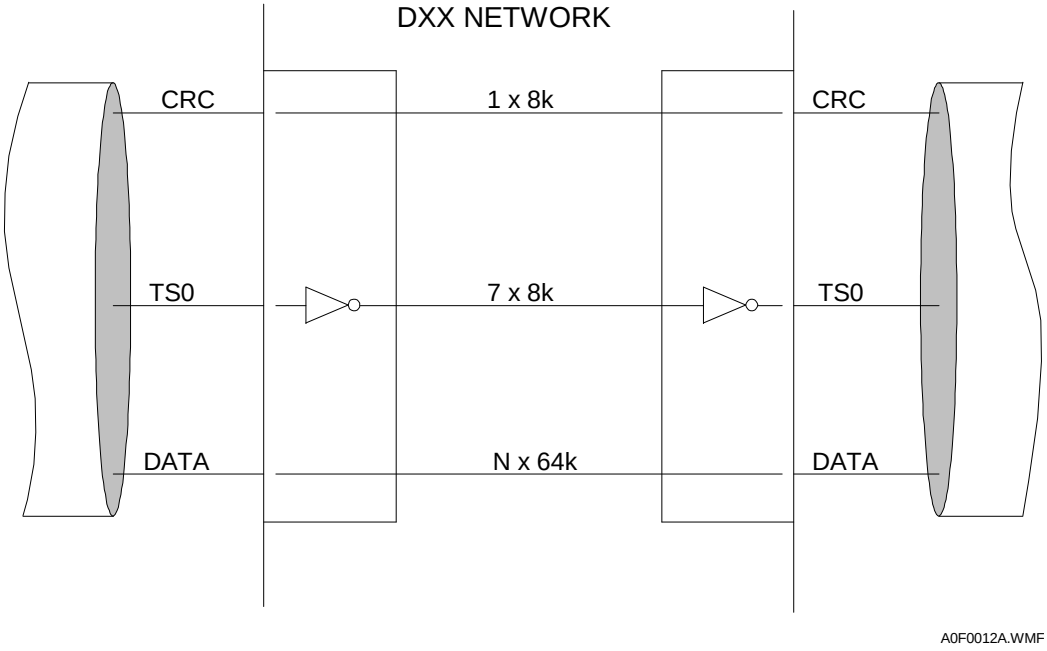


Fig. 158: TSO and CRC Connected Through the Network

The time slot ts0 is inverted before it is transferred to the transmission network. A capacity of 64 kbit/s is used on a trunk line to transmit the combination of time slot ts0 and the CRC check, and 64 kbit/s of the internal DXX node cross-connect bus. CRC check E-bits indicating remote end block errors are also connected through the network. If these bits are not used they must set to the state 1. The interface responds to errors in the same way as when only time slot ts0 is connected through the network.

Transparent Without Frame

The interfaces of a QMH unit can also operate in a transparent mode. In this mode the received signal is connected through the network without any manipulations. The receiver is not synchronized to the incoming signal frame structure; no additions to the output signal are made in the transmitter. However, the receiver does cut the signal into slices of eight bits, which are transmitted through the network and from these slices a signal conforming to the original signal is then reconstructed in the receiver. In the transmission network a transparent signal requires a capacity according to its interface bit speed.

In order to use the interface in the transparent mode the interface parameter Framing must be set Off during parameterization. No frame errors are detected in the transparent mode, as the frames are not processed in any way. An alarm for error rate 10E-3 will be calculated only from code errors, whereas the error rate in a normal mode is calculated using also frame synchronization word errors.

Transparent With CRC Monitoring

The interface can be set to a function mode, in which the signal is transparently connected through the network, but in which the user access interface receiver synchronizes to the received signal frame structure and performs a CRC check on the signal. In the transmit direction the signal contents is not changed. The interface is set into this mode by defining the Framing parameter as CRC monitor during parameterization. The interface will also output framing error information, but actions on these errors are prevented.

6.17.2.6 Loops in QMH

The NMS is able to control several loops in the QMH unit. Loops are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop time-out control which will turn off a loop when the user-defined time has come to an end.

Interface Loop

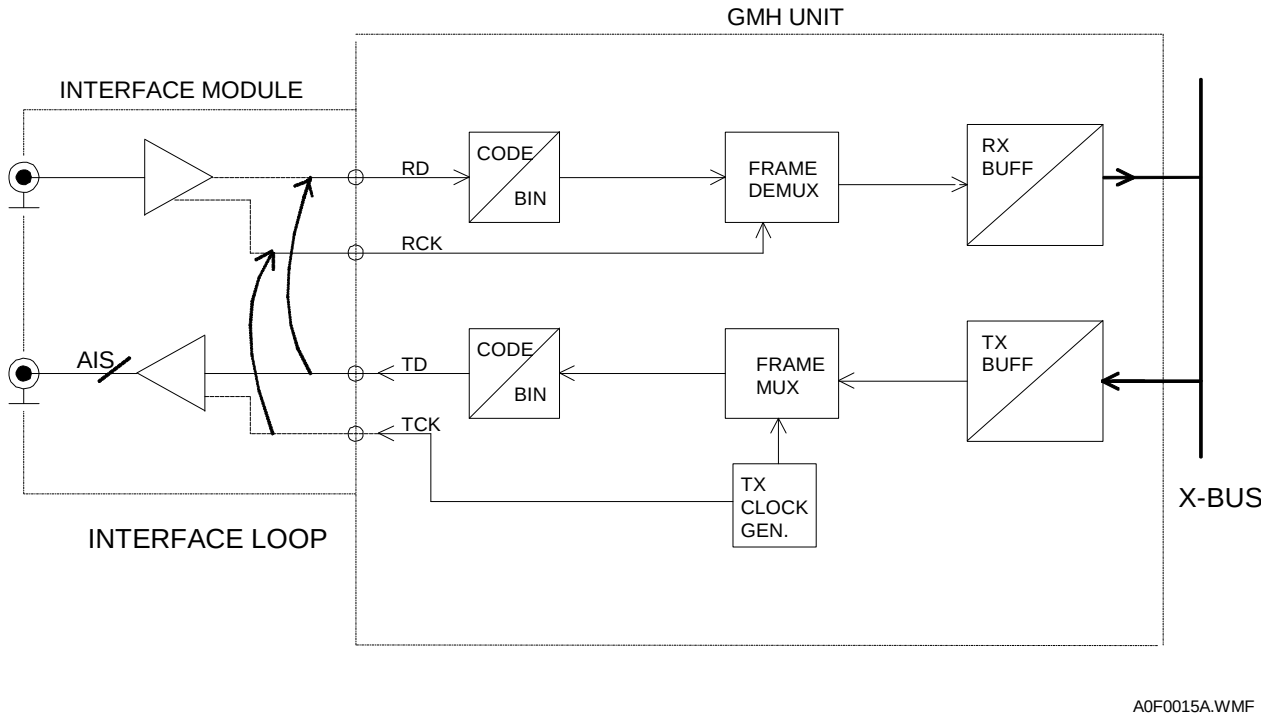


Fig. 159: Interface Loop

An interface loop is created in the interface module. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm LED is switched on.

The type of the module determines the point where the loop is created in the module. In most cases, due to technical reasons, the loop is not made using a signal with line level. The loop will, however, always test the interface module control bus and connectors and a part of the module logic. The line coder and decoder as well as the frame multiplexer and demultiplexer are also tested in the loop. There should be no other faults in the unit's fault list when the loop is created.

Equipment Loop

In an equipment loop the transmit data from the G.704 multiplexer before the interface module is looped back to the demultiplexer. The interface sends an AIS and the yellow alarm LED is switched on.

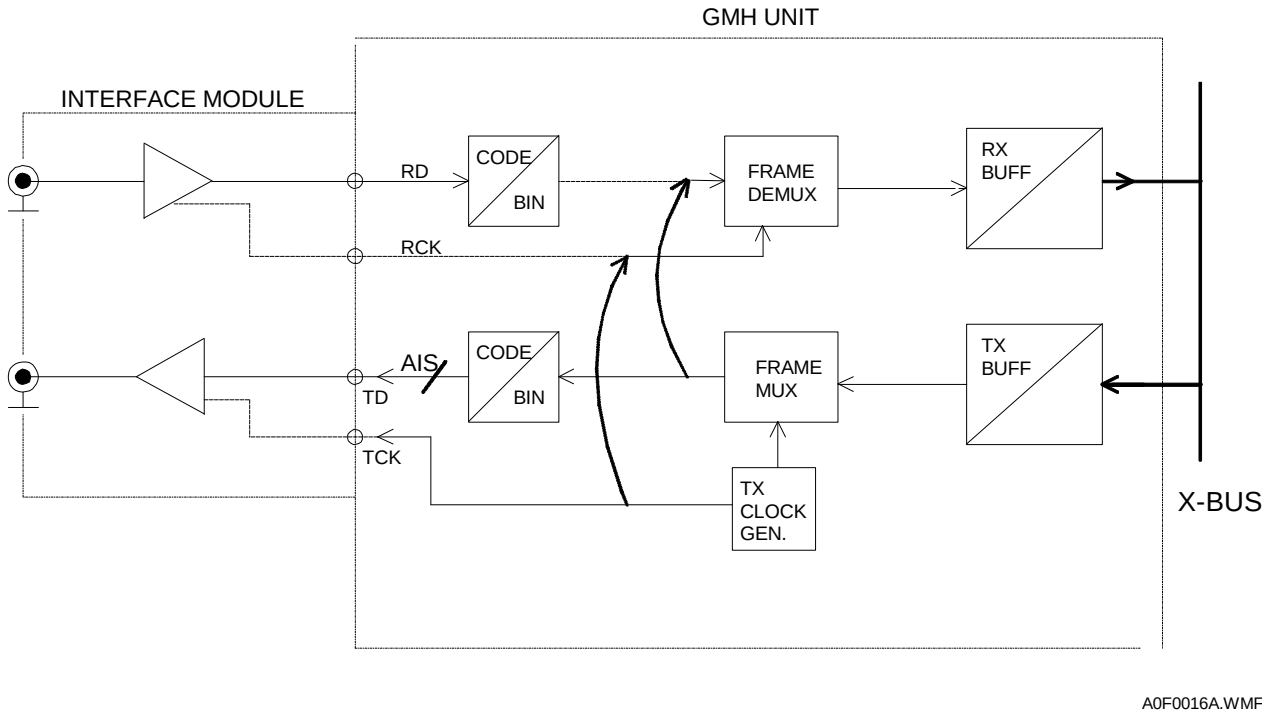


Fig. 160: Equipment Loop

The equipment loop is made in the unit. This loop tests the frame multiplexer and demultiplexer. Neither the line coder/decoder nor the interface module are included in the loop. It is also possible to detect faults in the transmitting and receiving buffers when a test signal from a measurement equipment is added to the signal passing through the looped channel. If no problems are detected with the interface loop, it is suggested to perform a test with the equipment loop to ensure that the module is in order.

Line Loop

In the line loop the Rx data received by the interface module is looped back to the interface transmitter. The received clock signal is used as the transmitter clock. AIS is connected to the X-bus instead of the received signal. The yellow alarm LED is switched on.

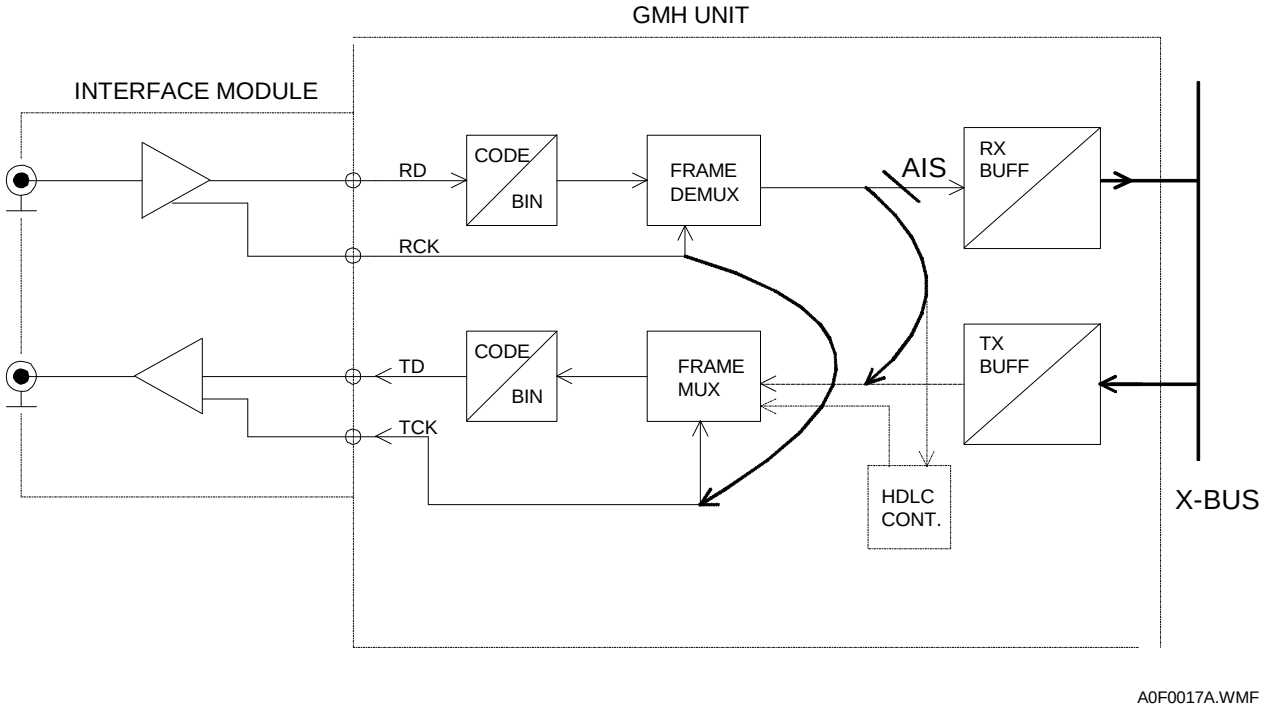


Fig. 161: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the Line Loop Test. When it is used, the HDLC controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made, the yellow LED of the unit which controls the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

Clock RAI

The QMH unit can employ a dedicated bit of the frame structure as a far-end clock alarm bit. When a node loses the synchronization with the network, it activates the alarm bit. When the node receiving synchronization from the faulted node detects the alarm state of this bit, it can cease to use the corrupted clock and select the next clock source from the fallback list.

The NMS is able to select the bit used as a clock RAI. The user must choose a time slot and a bit for the clock RAI. The clock RAI time slot cannot be used for payload data. Special bits like HDLC can, however, be used in the same time slot with the clock RAI. The user must also select the polarity (active state).

The interface activates the clock RAI in the transmitting direction when it receives an alarm message from the SXU unit via the control bus. The clock RAI is inactivated in a corresponding manner.

In the Rx direction the clock RAI bit is separated from the incoming data and sampled by the processor with a sampling period of about 10 ms. The state of the bit is preserved when two consecutive equal states are detected. When a unit in the active state receives the clock RAI bit, it will cut off the SYB clock if it has one. If the SXU loses the SYB clock, it will select the next clock source in the fallback list. If the clock signal is lost for a short period, the QMH unit returns the clock to the SYB bus when the clock RAI is inactivated and then the SXU unit again will use the clock. If the synchronization is lost for a longer period, the SXU unit will remove the faulted interface from the SYB bus by a command through the control bus; thereafter the SXU directs a command to the next object in the fallback list without an SYB bus to have it connect the clock to the cleared SYB line.

6.17.2.7 1+1 Protection

The interfaces 1 and 2 of the same unit can be 1+1 protected. Interfaces 3 and 4 can not be protected. In protected mode both channels must have the same speed and framing mode settings. A unit working in the protected mode will look like a cross-connect port towards the X-bus. In the protected mode both channels transmit the same data signal coming from a buffer. Both channels use their own frame mux to create the frame structure. The receiving direction includes a change-over switch that selects the active receiver. Rx signal faults are classified into several categories. The switch uses fault categories to select the interface to be used. The fault categories are indicated in the fault table. For example 1.x means first category (worst or most serious fault).

The operating modes of the change-over switch are:

— normal operation
— prefer operation
— forced operation

In the normal operating mode the switch will automatically switch to the other interface if the Rx signal fault category (1, 2, 3, 4, 5, OK) of the active interface continuously is worse than the fault category of the other interface, for a longer period than the given time delay. No switchover operation is activated when the categories are equal for both interfaces.

In the prefer operating mode a switch-over is triggered if there is a difference between the interface fault categories; the better interface is switched active. In a situation with equal fault categories for both interfaces the switch selects the preferred interface.

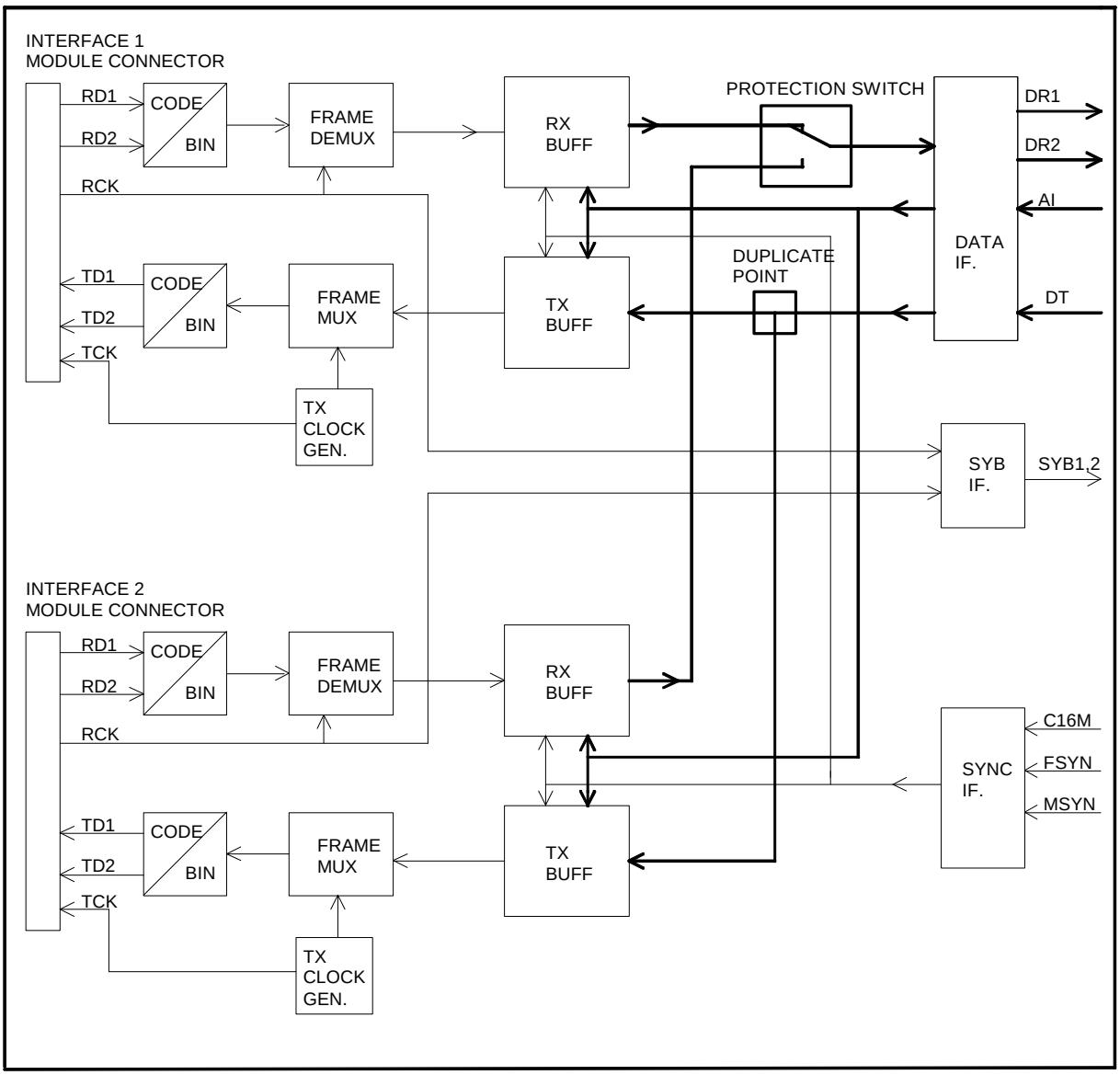


Fig. 162: Block Diagram of Protection

In forced operating mode the switch is forced to switch over without delay. Received data from the active interface is immediately connected to the X-bus. In this situation the Protection switch forced fault message with status MEI appears, and the red LED is turned on.

A switch operating time delay is defined for the prefer operating mode and the normal operating mode. The delay is defined as n x 10 ms, where n=0º6000; i.e. the delay is 0º1 minutes. The delay defines the allowed fault duration before the switch is triggered to switch over.

Fault and Service Status (PMA, DMA, MEI, S) in 1+1 Mode

In principle both interfaces generate their own alarms (alarm messages with fault status). PMA and S statuses are processed in this mode.

PMA Status Processing:

In the protection mode the normal PMA status is changed to the DMA status and there is an additional fault condition, Loss of protected signal, with a PMA status. In normal or prefer operating modes this special condition is created when both interfaces have a fault with fault category 3 or worse. In the forced operating mode this condition occurs if the forced interface has a fault with fault category 3 through 1. The inactive interface is not able to generate a fault with the PMA status.

S Status Processing:

In the protection mode an S status is generated only in the Loss of protected signal fault condition.

Far-End Alarms in 1+1 Mode

A far-end alarm indicates that the Rx signal is out of service (S status)

FrFEA = Rx frame out of service

MFrFEA = Rx multiframe out of service

Tx far-end alarms (FrFEA, MFrFEA) of both interfaces are generated assuming a fault status of the active interface. During a short period, when the change-over switch is in a transition phase, the far-end may generate an alarm even if there is no fault in the better interface. In forced operating mode only the active forced interface can cause far-end alarms to be sent.

RxAIS Processing

RxAIS and RxAIS to SigTS are always generated when FAE or MFrFAE is sent. AIS generating depends on the fault status of the selected interface.

6.17.3 Interface modules for QMH interface unit

General

The modules used for the QMH interface unit are:

— G703-75-Q
— G703-120-Q

6.17.4 QMH Faults and Actions

6.17.4.1 Terminology

The following acronyms will be used in the tables below:

- PMA = Prompt Maintenance Alarm
- DMA = Deferred Maintenance Alarm
- MEI = Maintenance Event Information
- S = Service Alarm
- R = Red alarm LED
- Y = Yellow alarm LED
- RB = Red alarm LED blink
- TxAIS = AIS insertion to Tx signal
- RxAIS = AIS insertion to Rx signal
- TxTS-AIS = AIS insertion in time slots of Tx signal
- FrFEA = Frame level far-end alarm (ts0/B3 in 2Mbit/s frame, ta66/B7 in 8 Mbit/s frame)
- MFrFEA = Multiframe level far-end alarm (FR0/ta sig/B6)

MFrFEA is also transmitted if FrFEA is transmitted.

6.17.4.2 Tx Signal Faults (Block 1,2,3,4)

Fault Condition	Status	LED	Tx signal
Tx Clock fault (PLL)	PMA, S	R	TxAIS
Bus faults IA activity missing Bus sync. fault (block 0)	 PMA, S PMA, S	 R Y	 TxTS-AIS TxTS-AIS
AIS from X-bus	MEI, S	Y	TxAIS[a]
BTE Tx line test	MEI, S	Y	Test pattern

a Only when FAS is transferred through the network

6.17.4.3 Rx Signal Faults (Block 1,2,3,4)

Signal & Frame Faults	Status	LED	Rx signal	Tx signal
1.1 Interface module missing	PMA, S	R	RxAIS	-
1.2 Wrong interface module	PMA, S	R	RxAIS	Tx signal cut
1.3 Rx signal missing	PMA, S	R	RxAIS	FrFEA
1.4 Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
1.5 Loss of frame alignment 1.5.1 Frame alignment lost 1.5.3 Frame alignment lost by CRC > 915/1000 errored CRC-blocks 1.5.2 CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
1.6 BER 10-3 - frame alignment word (normal error response) - line code errors	PMA, S	R	RxAIS	FrFEA
1.7 Wrong input signal 1.7.1 Own NNM messages received 1.7.2 Wrong IDs in NNM messages (detection can be inhibited) 1.7.3 No response to NNM message	 PMA, S PMA, S PMA, S	 R R R	 RxAIS RxAIS RxAIS	 - - -

Signal & Frame Faults	Status	LED	Rx signal	Tx signal
1.8 NTU problems 1.8.1 NTU power off/local loop 1.8.2 NTU line break 1.8.3 NTU short circuit	MEI MEI MEI MEI	Y Y Y Y	- RxAIS - -	- - - -
1.9 ASIC register error	PMA, S	R	-	-

Loops	Status	LED	Rx signal	Tx Signal
2.1 Local loops 2.1.1 Interface back to equipment 2.1.2 MUX/DEMUX back to eq. 2.1.3 MUX/DEMUX back to line 2.1.4 Line loop made by neighbour	 MEI, S MEI, S MEI, S MEI, S	 Y Y Y Y	 - - RxAIS RxAIS	 TxAIS TxAIS - -
2.2 Remote loops 2.2.1 Remote controlled line loop (2.1.4)	MEI, S	Y	-	-

Multiframe level faults	Status	LED	Rx signal	Tx signal
3.1 Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
3.2 AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Multiframe faults of the 8 Mbit/s signal are detected separately in each of the four signalling time slots (groups).				

Far-end alarms	Status	LED	Rx signal	Note
4.1 Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
4.2 Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off

Degraded signal	Status	LED	RxAIS	FrFEA
5.1 Error rate 10-3 - frame alignment word (AIS insertion inhited)	DMA	R	-	-
5.2 Error rate 10-6 - CRC block errors - line code errors (used for speeds over 1 Mbit/s)	DMA	R	-	-
5.3 Excessive errors	Programble	R	Programble	Programble
5.4 Degraded errors	Programble	R	Programble	Programble
5.5 Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
5.6 Buffer slips/1 hour	MEI	RB	-	-

6.17.4.4 Miscellaneous Faults (Block 1,2,3,4)

Fault Condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

6.17.4.5 1+1 Protection Switch Fault Messages (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	- [a]	- [a]

a Signal action depend on actions of the protectec interfaces.

6.17.4.6 Common Logic Faults (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal	Note
Reset	PMA, S	R	Bus if off	Off	[a]
Power supply (5V,+12V,-10V)	PMA	R	-	-	(2)[b]
CPU memory faults RAM fault EPROM fault FLASH faults	PMA, S	R	-	-	-
Incompatible EPROM/FLASH SW	PMA	R	-	-	-
Check sum err in downloaded SW	PMA	R	-	-	-
SW unpredicted	PMA	R	-	-	-
Missing settings	PMA, S	R	-	-	-
Start request denied	PMA, S	R	Bus IF off	AIS	-
Tx RAM error	PMA, S	R	-	-	-
Rx RAM error	PMA, S	R	-	-	-

a Fault message (with delta event) appears when the unit starts to operate.

b Rx signal action depends on the frame level alarm of the corresponding interface.

6.17.5 Front Panel for QMH with G703-120-Q and G703-75-Q

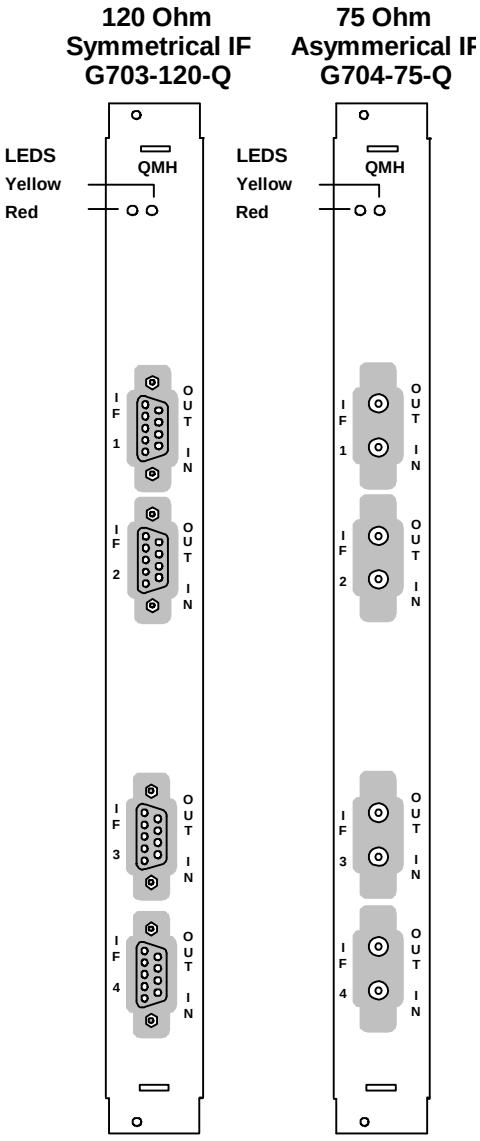


Fig. 163: Front Panel for QMH with G703-120-Q and G703-75-Q

D-9 female connector	
Pin	**Signal**
1	120 Ohm output
2	120 Ohm output
3	GND
4	120 Ohm input
5	120 Ohm input
6	GND
7	GND
8	GND
9	GND

G703-120-Q interface connectors are D-type 9 pin female connectors

G703-75-Q interface connectors are SMB-connectors

6.17.6 QMH Technical Specifications

6.17.6.1 Frame and Multiframe Operation

Filtering of FEA and MFrFEA bit:

The state of the alarm bit will switch if the opposite state is received three times consecutively.

AIS in frame 2048 kbit/s:

Signal containing two or less zeros in a 2-frame period is recognised as an AIS signal.

After AIS is detected, a signal containing three or more zeros in a 2-frame period is recognised not to be an AIS signal.

AIS in multiframe:

A signal in the signalling time slots containing one or no zeros in a multiframe period is recognised as an AIS signal.

Error rate 10E-3 limits from frame alignment word:

2048 kbit/s count time is four seconds	
Count to activate alarm:	94
Count to inactivate alarm:	17

Error rate 10E-3 limits from code errors:

Count time is one second		
Speed kbit/s	Activate	Inactivate
2048	1973	229

CRC spurious frame alignment limits:

speed kbit/s	values from 1000 counted to start a new frame search
2048	915

6.17.6.2 Power from Battery

The power may be calculated by adding values from the list below (values are prepared for calculating only, no absolute values)

QMH without modules	4,5 W
G703-75-Q	3,0W
G703-120-Q	3,0W

6.17.6.3 Mechanics

Weight:

- 410g with power module, without interface module
- 600g with G703-75-Q module
- 610g with G703-120-Q module

Unit dimensions:

- 25 x 160 x 233 mm

6.18 VCM Data Interface Unit

6.18.1 General

The VCM-10T-A/VCM-5T-A unit accesses unframed user signals at rates 1.2…2048 kbit/s. Newer HW/SW versions support rates up to 8448 kbit/s. It should be noted that when IF1/IF2 or IF3/IF4 rate exceeds 4224 kbit/s, it is not possible to lock the other port at any bit rate at all, this limitation is due to buffer space required. Rates equal or below 4224 kbit7s VCM-5-T/VCM-10-T support four independent data transmission interfaces. The unit can take two interface modules supporting two channel interfaces each. The available interface types support V.24, V.35, V.36, X.21 or G.703 interfaces (see Relevant Recommendations). User signals at bit rates below 64 kbit/s are rate-adapted according to the frame structure V.110/X.30. The V.110 signals are transported as 8, 16, 32 or 64 kbit/s across the DXX network. N x 64 kbit/s signals are transported at user rate across the network. Whenever required, the VCM supports end-to-end CRC supervision of the user signals and plesiochronous data timing. At rates below 64 kbit/s the CRC and plesiochronous timing features are supported in the V.110 frame. At higher rates an extra transmission capacity of 8, 16 or 24 kbit/s is required across the DXX network. Asynchronous start-stop signals are supported at bit rates below 256 kbit/s. VCM also includes a point-to-multipoint data bridge.

The VCM unit supports the full range of DXX user bit rates ≤ 600 bit/s…2048(8448) kbit/s. The available interface types allow for cable lengths of a few meters. The transformer coupled G.703 interface can be used up to a few hundred meters. The node with the VCM interfaces should normally be installed close to equipment in order to be accessed.

The VCM is used for point-to-point (pp) data circuits, and as a point-to-multipoint (pmp) server for point-to-multipoint circuits.

Typical applications for the low speed VCM interfaces V.24/V.28 (≤ 0.6…19.2, 38.4 kbit/s and n x 3.6 kbit/s) are:

— termination of pp circuits in a data processing centre
— termination of pmp circuits; master and slave ports
— pmp server
— transfer from pure digital transmission (DXX) to VF modems at e.g. the national border
— termination of V.110 formatted circuits

Typical applications for the medium speed VCM interfaces V.35, V.36 (≤ 9.6…38.4, 48, 56, and n x 64 kbit/s) are:

— termination of pp circuits in a data processing centre
— termination of pmp circuits; master and slave ports
— pmp server
— links for data multiplexers, PADs, LAN bridges and routers
— computer - computer data links
— trunks of low, medium capacity data networks

Typical applications for the high speed VCM interfaces V.36 (64…8448kbit/s) are:

— links for data multiplexers, PADs
— links for LAN bridges, routers
— computer - computer data links
— termination of pmp circuits; master and slave ports
— pmp server
— trunks of low or medium capacity data networks

Low speed VCM interfaces V.24/V.28 at rates n x 3.0 and n x 3.2 kbit/s may be used for access links to data networks using 6+2 (n x 3.2 kbit/s) or 8+2 (n x 3.0 kbit/s) signalling formats.

VCM interfaces X.21 at rates 0.6, n x 1.2, 48, 64 and (n x 64) kbit/s may be used for X.21 access links to X.21 or X.25 data networks. In X.21bis mode the X.21 interface may be applicable for a variety of applications with data multiplexers etc.

The G.703 interface may be used mainly for transfer between a DXX network and another transport network or switching system based on G.700 series ITU-T/CCITT Recommendations. Some computers and data multiplexers may also be equipped with 64 kbit/s G.703 interface.

The unit front panel holds two alarm LEDs, a red and a yellow, and cabling connectors for the user interface:

— one 25-pin D-type (ISO 2110) connector for each V.24/V.28 and IEC-530 interface
— one 34-pin ISO 2593 connector for each V.35 interface
— one 37-pin D-type (ISO 4902) connector for each V.36 interface
— one 15-pin D-type (ISO 4903) connector for each X.21 interface
— one 15-pin D-type (ISO 4903) connector for each G.703 interface
— one 9-pin D-type connector for each PDA G.703 interface

6.18.2 Operation

6.18.2.1 Mechanical Design

The mechanical design of the VCM unit is based on the standard DXX system mechanics. The unit VCM-5T-A occupies one (V.24, X.21 and G.703 interfaces) and VCM-10T-A two unit slots (V.35, V.36 interfaces). A unit can occupy any card slot in the subrack; however, the general recommendations for subrack equipping should be followed.

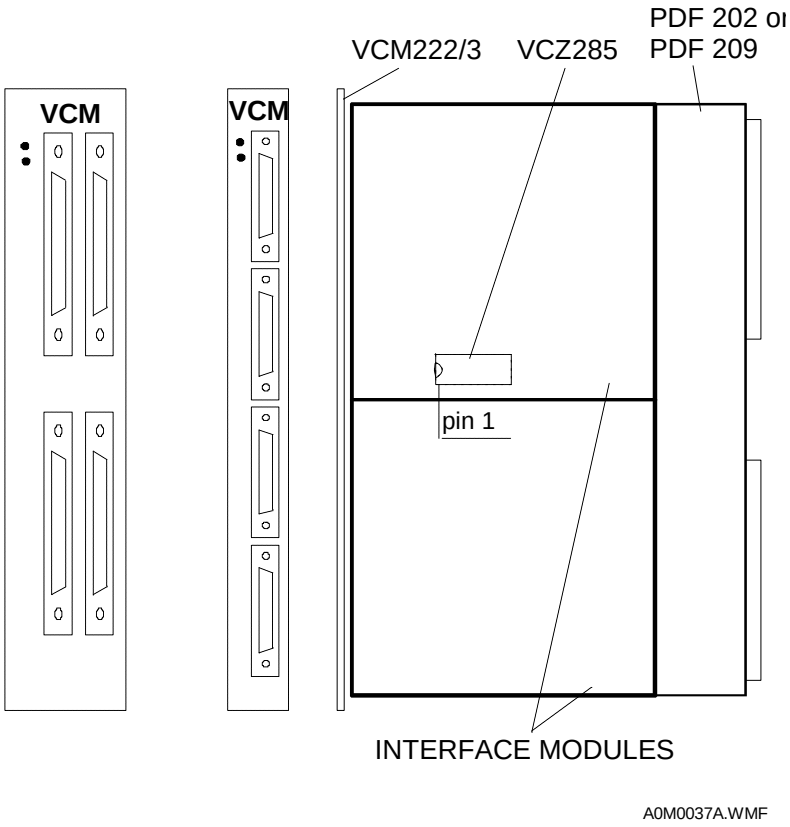


Fig. 164: VCM-10T-A/VCM-5T-A Unit Equipped with IF Modules

The body of the VCM unit consists of an E2-sized VCM base unit, a unit power supply module PDF 202/209, and a program memory VCZ 285A. The base unit can be equipped with two interface modules, each providing two physical user interfaces supporting the particular applications.

Functional Structure

The basic functional blocks of the VCM unit are:

— data formatting circuitry
— X-bus interface
— controller, control bus interface
— interface modules
— power supply

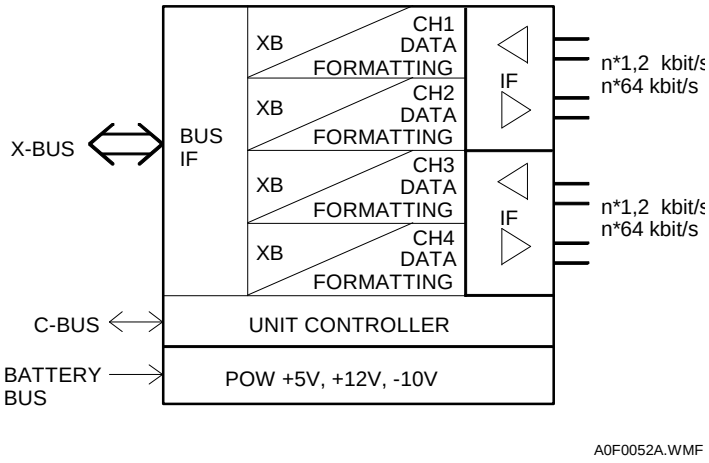


Fig. 165: Functional Structure of the VCM Unit

Block Diagram

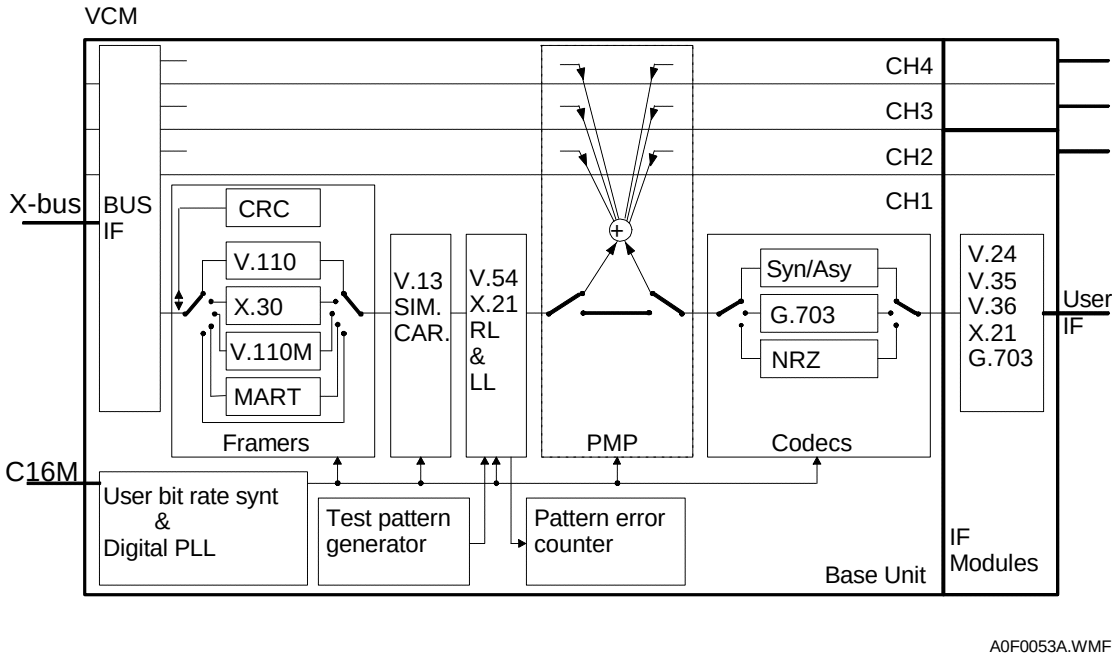


Fig. 166: Functional Block Diagram of the VCM-10T-A Unit

6.18.2.2 Data Formatting Circuitry

The data formatting circuitry determines a majority of the characteristics of the data interfaces provided by the VCM and provides the main data processing functions: Rate adaptation and framing, CRC monitoring V.13 simulated carrier, bit rate generation, user interface signal coding (e.g. G.703), Synch/async conversion; point-to-multipoint bridge function, V.54 and X.21 test loops, and test pattern generation and error counting. Some of these functions are described in detail below.

6.18.2.3 Rate Adaptation and Framing

Bit Rates ≤ 64 kbit/s

Data bit rates ≤ 64 kbit/s are, using ITU-T Method V.110, rate adapted to 8, 16, 32 or 64 kbit/s which can be handled by the cross-connect unit and routing tools. The V.110 frame is transparently transported through the DXX network and can be used for end-to-end monitoring of the channel quality.

The V.110 frame offers three channels, called SA, SB, and X, for transfer of control signals. The channel SA carries signal 108/107, SB 105/109, and X carries both signal 106 and the far-end-alarm.

106 is either derived locally from 105 or from channel X received from the far-end. When 105 is turned ON the locally generated 106 signal is delayed until 105 is sampled by the framer. This generates the minimum 106 delay which guarantees that 109 turns ON before the first data bit is received at the far end.

When 107/108 transfer is not required, both SA and SB (SA + SB = S) may carry the 105/109 or C/I signal, enabling minimum control signal delay. The S signal is sampled once for each byte of user data. This mode is recommended for PMP applications. In the management menus this mode is called V.110S or X.30 and the basic V.110 mode simply V.110.

The V.110 or V.110S configurations use bit oriented data buffering with ± 2 bits jitter/wander margin. Byte oriented data buffering is used in X.21 applications or cases where octet timing is desired. Byte oriented buffering and minimum control signal delay is called X.30 as the mode conforms to ITU-T Recommendation X.30.

User data rates ≤ 600 bit/s are transferred by sampling at rate 4800 bit/s.

Rates 0.6 kbit/s and n x 1.2 kbit/s (up to 38.4 kbit/s) and 48 kbit/s are supported in V.110, V.110S and X.30 modes. User rates n x 3.0 kbit/s (data network formats 8+2 bits), n x 3.2 kbit/s (data network formats 6+2 bits) and n x 3.6 kbit/s (including rates 3.6, 7.2, 14.4 and 28.8 kbit/s) are supported in modes V.110 and V.110S.

At rate 56 kbit/s both ITU-T V.110b and V.110c (b,c refer to table 7b/V.110 and table 7c/V.110) framing is supported.

Bit Rates n x 8 kbit/s

At rates 8, 16, 32 kbit/s user data is transferred on 1, 2 or 4 bits of a time slot. At rates 72 and 80 kbit/s data is transferred using one full time slot and 1 or 2 bits of another one. Rates 144 and 160 kbit/s need two full time slots and two or four bits of a third one. No data framing is needed for the data transfer. Rates 48 kbit/s and 56 kbit/s are selected as 6 x 8 and 7 x 8 kbit/s in the Management menu.

Bit Rates n x 64 kbit/s

At n x 64 kbit/s rates 64…2048/(8448) kbit/s the unframed user data is transferred on 1…32/(132) time slots. The data buffer length may vary from three to 64 /(128) bytes. The nominal buffer length selection allows for ± 18 μs or at minimum 1 byte of jitter and wander.

Bit Rates n x 64+8 kbit/s

The n x 64+8 kbit/s rate is basically intended for the T1 rate 1544 kbit/s. Some other n x 64+8 kbit/s rates are also supported. This mode uses n full time slots and 1 extra bit.

6.18.2.4 CRC Monitoring

The VCM can support end-to-end CRC monitoring of the user data. The CRC-4 procedure used is similar to the one for G.704 2 Mbit/s frames. At rates ≤ 1.2, n x 1.2, n x 3.0, n x 3.2, n x 3.6 kbit/s the CRC check sum is transferred on the last five bits of frame alignment signal of the V.110 or X.30 frame. A modified V.110 frame is used at rates 48 and 56 kbit/s. When transferring the CRC check sum, the frames are called V.110M or X.30M as the corresponding ITU-T frames do not support CRC monitoring.

At n x 8 kbit/s, n x 64 kbit/s, n x 64+8 kbit/s the CRC check sum is transferred end-to-end in a proprietary frame, called , and using 8 kbit/s extra XB capacity. It is not possible to use CRC monitoring at rates 8, 16 or 32 kbit/s because these rates are connected directly to the X-bus without formatting the V.110 frame.

End-to-end performance monitoring is based on end-to-end CRC monitoring, when activated. Channel associated end-to-end CRC monitoring is the only way to get accurate performance characteristics for a channel. The performance data are expressed in terms of G.821 parameters.

The data from the last 24-hour period is stored for transfer to the DXX performance data base after midnight (00.00) each day. The performance data of the last 15-minute period are recorded separately. If the 15-minute performance degradation exceeds a preset limit, a transfer to the performance database is requested by the unit.

Control Signals

The VCM supports control signals for the user channels:

— 105/109 transfer at all bit rates (X.21bis)
— 108/107 transfer at V.110 based frames (X.21bis)
— 106 locally generated
— 106 transfer from the far-end (V.110 only) (X.21bis)
— C/I at X.21 interfaces and bit rates 0.6, n x 1.2, 48 and n x 64 kbit/s

The control channels can be transferred in several ways depending on the user bit rate. The SA, SB and X bits are normally exploited (selection V.110, X.30) with V.110, V.110M, X.30, X30M frames. The V.13 simulated carrier or an 8 kbit/s channel are used at n x 8 and n x 64 kbit/s rates.

The 8 kbit/s channel requires additional transmission capacity but it offers a continuous channel required for e.g. X.21 applications.

6.18.2.5 V.13 Simulated Carrier

The V.13 simulated carrier is an inband transfer method, which does not require extra capacity. When 105 is turned OFF, the user data is substituted by a pseudo-random pattern. After reception of 48 bits of that pattern 109 is turned OFF and the user data (104) is blocked to OFF state. When 105 turns ON the pattern generator input is changed from 1 to 0 for 8 bits. Thereafter 106 turns ON and the channel is ready to transfer user data.

If, due to transmission errors, the receiving end misses the turn on sequence, it will automatically return to ON state when more than 31 errors have been detected in the pseudo-random pattern during a certain time period.

106 Delay

Normally, the minimum 106 delay, required to guarantee proper operation, is used. Whenever required, additional delay may be selected in the range of 8…8000 bits. The delay is expressed in time units at the management interface.

105 Supervision

In some applications 105 should continuously stay in ON condition. If desired, the VCM can monitor the 105 state and generate an alarm if 105 goes OFF. In PMP applications the length of the talk period may be limited. When talk period supervision is activated, VCM will block OFF the interface upon detecting a 105 ON period longer than the selected value.

6.18.2.6 Bit Rate Generation

A variety of bit rates are required for the VCM user interfaces. The data timing signals are derived from the 16896 kHz system clock by built in programmable frequency synthesizers. There is a synthesizer for each channel and each transmission direction.

Timing Sources

Depending on the configuration, the timing signal for the incoming data (Tx direction) can come from the user equipment or from the clock source of the VCM. The clock for the outgoing data (Rx direction) can come from VCM or it can be taken from the Tx clock received from the user.

Plesiochronous Clocking

When the user data clock cannot be synchronized to the DXX clock, plesiochronous operation (same nominal bit rate) is required. VCM supports transfer of plesiochronous clocking at all bit rates except for 0.6, 1.2, 2.4, 8, 16 and 32 kbit/s.

Plesiochronous transfer is supported in the standard ITU-T V.110 Frame at rates n x 1.2, n x 3.2, n x 3.6. A modification of V.110 (V.110M) also supports plesiochronous clocking at n x 3.0, 48 and 56 kbit/s. An extra 8 kbit/s channel with frame is required at rates n x 8 kbit/s and n x 64 kbit/s. The 8 kbit/s channel supports both CRC monitoring and plesiochronous timing at bit rates up to and including 512 kbit/s. Above 512 kbit/s plesiochronous clocking requires two 8 kbit/s channels, one for the frame and the other for the plesiochronous clock.

The V.110 method of transferring the data phase and ± stuffing is used at all bit rates. The synthesizers operate in a digital PLL mode with jitter slight filtering of the input clock before phase comparison with the system reference clock. At the receiving end the synthesizer adjusts its phase according to the value received from the far-end. The phase adjustments take place in small steps in order to minimize the phase jitter amplitude and frequency spectrum.

At plesiochronous clocking the V.110 data buffer operates in bit mode. At n x 64 kbit/s rates the data buffer operates in a so called frame synchronous mode where the data transferred during one X-bus frame forms a block. The stuffing bits are deleted and inserted at the border between two blocks.

6.18.2.7 Coding of Interface Signals

G.703 Co- and Contradirectional Interface

Contra- and codirectional G.703 interfaces are supported at bit rate 64 kbit/s.

In contradirectional mode, both transmit and receive clocks are generated and transferred to the user equipment on separate interface pairs as 50% AMI signals. A polarity inversion violation is sent each eight clock period indicating the last bit of an octet. The 100% AMI coded data signals use separate pairs.

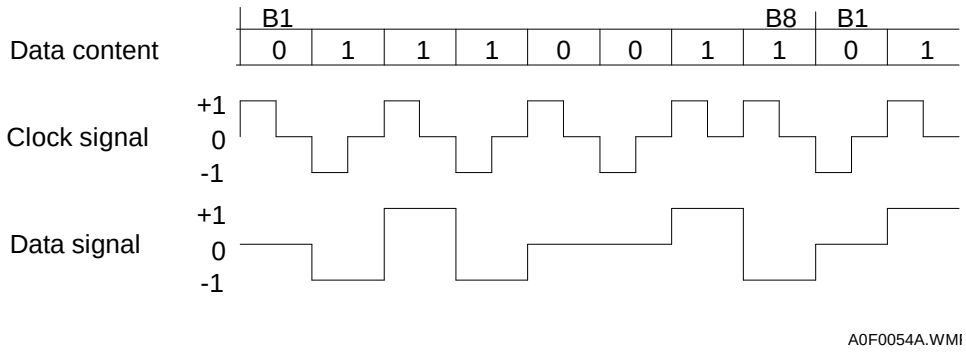


Fig. 167: Signal Coding at Contradirectional G.703 Interface

In codirectional mode is used one signal pair per direction. Data, clock and octet timing are coded into one three-level signal. Zeroes are coded to pattern 1010 and ones to 1100. Consecutive patterns are of different polarity. Octet timing is indicated by violation of polarity changes.

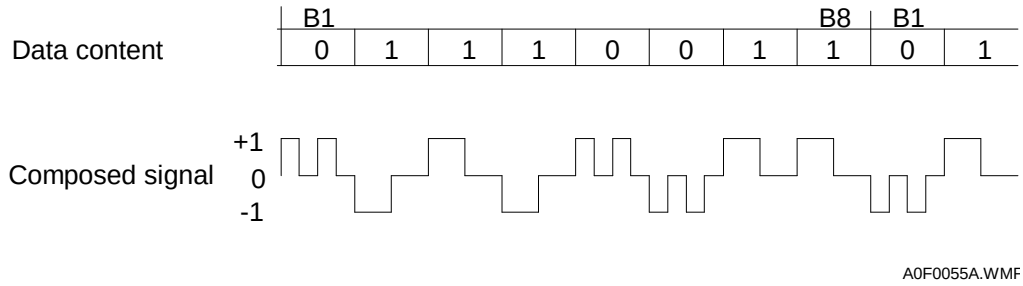


Fig. 168: Signal Coding at Codirectional G.703 Interface

6.18.2.8 Async/Sync Conversion

The asynchronous/synchronous converter samples the incoming signal at 16 times the user rate. The converter recognizes the start-stop pattern which may have start-stop bits and 6, 7, 8 or 9 data bits. Each detected wrong pattern start-stop is considered as an input signal code error.

In the case of overspeed stop bits are deleted with certain intervals. The receiving side adds the deleted stop bits and compensates for the overspeed by shortening the stop bits of the eight consecutive characters. The method allows for 1.25% overspeed. At underspeed additional stop characters are inserted. In extended operation mode, stop bits can be deleted from every forth character enabling 2.5% overspeed.

The async converter can be used at bit rates 600 bit/s…64 kbit/s, 128 kbit/s and 256 kbit/s. At bit rates below 600 bit/s the async converter is by-passed and the user data is sampled at the rate 4800 bit/s.

Data InterfacesV.24/V.28, V.35, V.36 Interfaces

The interface signals of V.24/V.28, V.35, V.36 and X.21 interfaces are NRZ coded. Data and control signals can change their states at the edge of a clock period. The clock signal has a falling edge at the beginning of a period and a rising in the middle of the period. The interface modules convert the CMOS level signals to appropriate interface signals.

Signal Name	Interface Type V.24/V.28	V.35	V.36	X.21
103	V.28	V.35	V.11	V.11
104	V.28	V.35	V.11	V.11
105	V.28	V.28	V.11	V.11
106	V.28	V.28	V.11	V.11
107	V.28	V.28	V.11	V.11
108	V.28	V.28	V.11	V.11
109	V.28	V.28	V.11	V.11
113	V.28	V.35	V.11	V.11
114	V.28	V.35	V.11	V.11
115	V.28	V.35	V.11	V.11
140	V.28	V.28	V.28	-
141	V.28	V.28	V.28	-
142	V.28	V.28	V.28	-

The data and clock signals for G.703 outputs come as positive and negative CMOS level pulses from the base unit. The control signals are converted to G.703 signals by the aid of drivers and transformers. The G.703 input signals are converted to CMOS signals using comparators.

6.18.2.9 Test Loop Functions

VCM is equipped with V.54 test loop functions supporting local loop (loop3, LL) and remote loop (loop2, RL). X.21 loop functions (LL, RL, RLB) are supported with the X.21 interface module. The loops can be controlled by the user and the operator. When the V.54 loop is ON, test loop indication signal 142 goes ON. Thereafter the loop tests can be started. A loop2 (RLB) activated from the far-end turns signal 142 ON and sets received data to OFF. In case of X.21 the loop2 activated at the far-end sets received data to OFF or pattern 1010… The duration of the loop can be limited to a configurable value. In general, the loops should be enabled in the equipment which are as close as possible to the user interfaces and disabled in all intermediate equipment.

The loops are visible in the **Loop** window of the DXX management workstation or service computer. The operator can also, close to the X-bus interface, make a line loop towards the user interface or close to the physical user interface a network loop back towards the network.

Test Functions

The VCM has built-in per channel test pattern generators and pattern error detectors. The test pattern is CCITT 511. Typically, a test is performed with the remote loop activated at the far-end. A unit level test window facilitates activation of the test resources and presentation of the test results.

Normally the operator activates the test resources using the test functions of the Ericsson DXX Manager. The test functions utilize either the test resources of the interface units or the common test resource of the SCU.

6.18.2.10 X-Bus Interface

The X-bus interface performs the adaptation between the data formatting circuitry and the data bus and address bus of the back plane of the DXX subrack. The X-bus interface utilizes the lower rear connector. The main signals of the X-bus interface are:

Signal	Signal Description
C16M	Internal timing signal for the node
FSYN, MSYN	Frame and multiframe alignment signals
DR10 - 17	8-bit wide data bus VCM towards SXU
DR20 - 27	8-bit wide duplicate of the data bus VCM towards SXU
T0 - 7	8-bit wide data bus SXU towards VCM
BAD0 - 7	8-bit wide addressing bus SXU to VCM

The X-bus interface transmits and receives one byte of data each time an interface of the unit is addressed by the BAD0 - 7 bus. For each 125 µs bus frame the interface can be addressed once or several times depending on the XB capacity. The X-bus connection type is uneven. A channel with less than 64 kbit/s bit rate is transferred between VCM and the cross-connect unit SXU using one byte per frame (64 kbit/s). 1, 2, 4, or 8 bits of the byte are utilized. The SXU maps only the used bits to the trunk.

6.18.2.11 Unit Controller

The unit is controlled by an 80C188 microprocessor. The basic unit software is stored in an interchangeable EPROM memory identified as VCZ 285A. The application programs are stored in an EPROM memory or in a non-volatile FLASH memory supporting remote controlled downloading of the application SW. The non-volatile memory also stores the configuration parameters and the HW and SW identifications of the unit. The interface modules are also controlled, monitored and identified by the unit controller. In the case of a power interruption the unit automatically restores the configuration prevailing before the interruption.

The unit communicates with other units of the subrack and with the service and management computers of the DXX network via the control bus interface, including a HDLC controller. Each unit position in the subrack has an individual address which is read from the back plane connector. This address is a part of the unit identification address used by the DXX communication network. The functions of the unit are presented as manageable objects to the Network Management System of the DXX network.

6.18.2.12 A/D Converter

The unit includes a multichannel analog-to-digital converter (A/D) which measures the operating voltages +5 V, +12 V, -10 V and the +5 V bus interface voltage of the back plane and analogue signals from modules e.g. power-off condition of the input signal (V28, V35, V36, X21).

6.18.2.13 Power Supply

The replaceable DC/DC power supply module PDF 202 or PDF 209 provides the operating voltages +5 V, +12 V and -10 V for the VCM unit. The power supply operates directly on the station battery voltage which is supplied via the fuse unit and the back plane of the DXX subrack. The X-bus interface circuits are powered from the back plane of the subrack during unit start-up conditions. The operating voltages of the unit are monitored, including the +5 V back plane voltage. An alarm is generated if a voltage is out of its limits.

6.18.2.14 Timing Modes

The clocking mode of data interfaces depend on the type of interface, type of equipment interfaced and on the operation mode. The user clock may be considered as locked to the DXX timing source if:

— the user equipment uses the clock supplied by the DXX interface
— if the user system and DXX use the same timing source e.g. a national timing distribution network
— if both the user system and DXX are locked to timing source in accordance with CCITT Recs. G.811, ITU-T G.823.

V Series Interfaces

In most cases the V series interface (V.24/V.28, V.35, V.36) of VCM is connected to a DTE as if it were a data modem (DCE). The data interface is clocked from the DXX network. The clocking method can be used when the transfer delay between DCE and DTE is below 0,15 bit (L < 30/(bit-rate) m); bit-rate in Mbit/s). The timing mode is called synchronous 114/115.

— data in direction DCE to DTE (104) is clocked by timing signal 115
— data in direction DTE to DCE (103) is clocked by timing signal 114 from the DCE (VCM)

At longer DTE-DCE distances and in applications where the DTE terminates a data circuit with clock looping at the far-end or clocked by a timing source locked to the same source as the DXX network clock 113 is used in direction DTE-DCE instead of 114. The signals in the direction DTE-DCE may contain jitter and wander referred to the DCE-DTE timing. The timing mode is called 113/115 mesochronous.

— data in direction DCE to DTE (104) is clocked by timing signal 115
— data in direction DTE to DCE (103) is clocked by timing signal 113

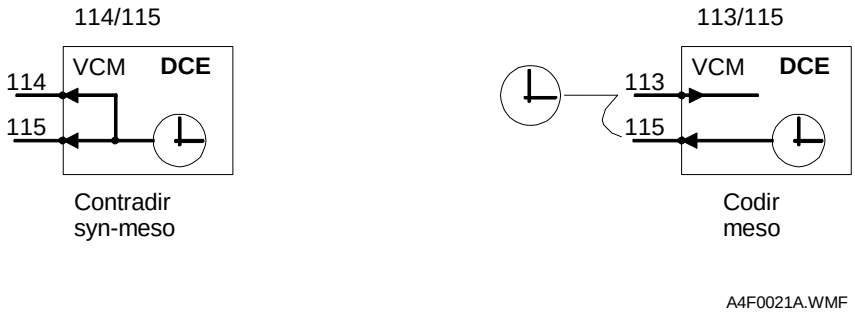


Fig. 169: Contradirectional Synchronous and Codirectional Mesochronous Timing of a VCM Data Interface in DCE Mode

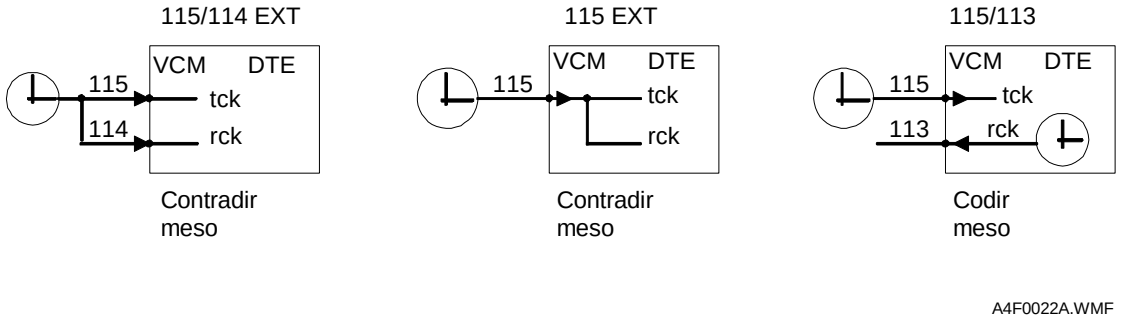


Fig. 170: Contradirectional Synchronous and Codirectional Mesochronous Timing of a VCM Data Interface in DTE Mode

When interfacing a DCE, the VCM may operate either as a DCE (signals cross-connected in the interface cable) or as a DTE (without signal cross-connection in the interface cable). The timing signals may, in contradirectional mode, come from the DCE to VCM (cases 115/114 EXT or 115 EXT) or, in codirectional mode, from both the DTE and DCE (115/113). For the time being only V.24 DTE interface modules are available.

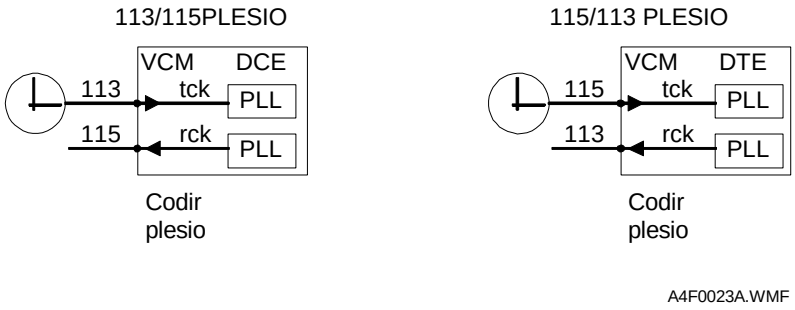


Fig. 171: Codirectional Plesiochronous Timing of a VCM Data Interface

A data source (DTE or DCE) which cannot be synchronized to the DXX network is accessed using plesiochronous timing. In plesiochronous mode only codirectional timing is supported.

Asynchronous V Series Interface

Asynchronous operation is supported at bit rates up to 256 kbit/s. The timing signals are switched off in asynchronous mode.

X.21 Interface

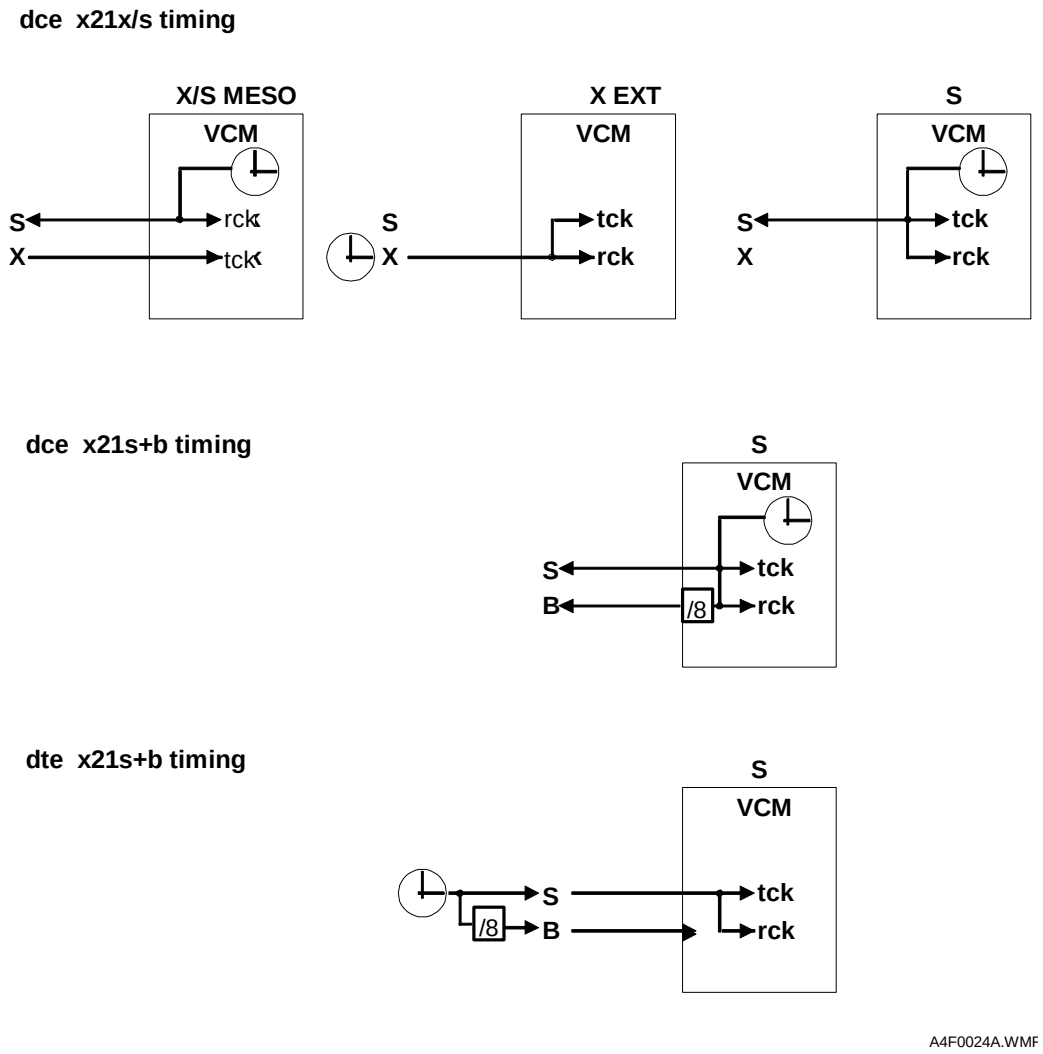


Fig. 172: Timing of a X.21 VCM Data Interface

Only one clock signal is used in X.21 mode. The clock comes either from VCM or towards VCM and it is always locked to the same source as the DXX clock. When required, octet timing may also be used.

G.703 Interface

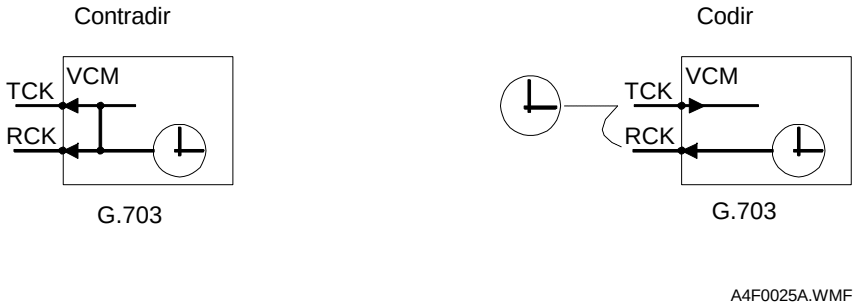


Fig. 173: Timing of a 64 kbit/s G.703 VCM Data Interface

The G.703 interface at 64 kbit/s supports co- and contradirectional operation. Octet timing is also supported.

6.18.2.15 Rate Adaptation and Mapping

The frame structures used are described in Appendices. The signals and control signals are rate-adapted and mapped as follows in the VCM unit:

Rate Adaptation and Mapping at Bit Rates ≤ 48 kbit/s

User Rate kbit/s	Rate Adapt. Method	XB Mapp. kbit/s	Control Signals	Plesio. Clocking
< 0.6	V.110	1x8	SA, SB, X	No
0.6, 1.2, 2.4	V.110	1x8	SA, SB, X	No
0.6, 1.2, 2.4	X.30	1x8	S	No
4.8	V.110	1x8	SA, SB, X	Yes
4.8	X.30	1x8	S	No
9.6	V.110	2x8	SA, SB, X	Yes
9.6	X.30	2x8	S	No
19.2	V.110	4x8	SA, SB, X	Yes
19.2	X.30	4x8	S	No
38.4	V.110	8x8	SA, SB, X	Yes
38.4	X.30	8x8	S	No
3	V.110	1x8	SA, SB, X	Yes
6	V.110	2x8	SA, SB, X	Yes
12	V.110	4x8	SA, SB, X	Yes
24	V.110	8x8	SA, SB, X	Yes
3.2	V.110	1x8	SA, SB, X	Yes
6.4	V.110	2x8	SA, SB, X	Yes
12.8	V.110	4x8	SA, SB, X	Yes
25.6	V.110	8x8	SA, SB, X	Yes
3.6	V.110	1x8	SA, SB, X	Yes
7.2	V.110	2x8	SA, SB, X	Yes
14.4	V.110	4x8	SA, SB, X	Yes
28.8	V.110	8x8	SA, SB, X	Yes

NOTE!

End-to-end CRC monitoring can be supported at all bit rates above. ITU-T Rec. V.110 and X.30 do not support CRC monitoring. The frame type is renamed to V.110M or X.30M when CRC is activated.

Rate Adaptation and Mapping at Bit Rates ≥ 48 kbit/s

User Rate kbit/s	Rate Adapt. Method	XB Mapp. kbit/s	Control Signals	CRC Supp.	Plesio. Clocking
48	V.110	1x64	SA, SB, X	No	No
48	V.110M	1x64	SA, SB, X	Yes	Yes
56	V.110/7b	1x64	-	No	No
56	V.110/7c	1x64	SA, SB, X	No	No
56	V.110M	1x64	SA, SB, X	Yes	Yes
64	-	1x64	-	No	No
64		1x64+ 8 + 8	SB	Yes	Yes
72	-	1x64+1x8	-	No	No
72		1x64+1x8+ 8 + 8	SB	Yes	Yes
80	-	1x64+2x8	-	No	No
80		1x64+2x8+ 8 + 8	SB	Yes	Yes
144	-	2x64+3x8	-	No	No
144		2x64+3x8+ 8	SB	Yes	Yes
160	-	2x64+4x8	-	No	No
160		2x64+4x8+ 8 + 8	SB	Yes	Yes
Nx64	-	Nx64	-	No	No
Nx64		Nx64+ 8 + 8	SB	Yes	Yes N ≤8
Nx64		Nx64+ 8 + 8	SB	Yes	N N > 8
Nx64		Nx64+ 24	SB	Yes	Yes N > 8
1544	-	Nx64+8	-	No	No
1544		Nx64+8+ 8 + 8	SB	Yes	No
1544		Nx64+8+ 24	SB	Yes	Yes

NOTE!

V.110/7b refers to ITU-T Rec. V.110 Frame Table 7b and V.110M/7c is a slightly modified V.110 frame. is a V.110 (56 kbit/s) like specific frame. 8, 16 denotes extra capacity carrying CRC with plesiochronous timing control. SA, SB and X refer to SA, SB, X bits in the frame.

At all data rates the channels can support simulated carrier according to V.13 for transfer of the 105/109 signal. V.13 is mostly used at rates n x 64 kbit/s.

6.18.2.16 Performance

VCM supports circuit performance monitoring separately for each channel. When V.110, X.30 or framing is activated with CRC transfer VCM performance signal quality monitoring according to G.821. The performance data are collected in three ways:

- The unit collects the G.821 data for 24-hour periods starting at 00:00 hours. The 24-hour data are available for automatic transfer to the DXX performance data base during the next day.
- If activated, the unit also calculates performance data for 15-minute time periods. If the signal impairments exceeds a selected limit during a period, the data is transferred to the performance database.
- A third set of performance counters is available for the network operator. He/she can start and terminate error monitoring at any time and gain performance data for periods from seconds to days or months. The results are shown as error counts and as G.821 parameters.

Error Counters

VCM can count by using SW and HW counters:

- number of frame losses (frame from net, C2)
- number of multiframe losses (frame from net, C2)
- number of frame word errors (frame from net, C2)
- number of CRC block errors
- code errors in the user interface (G.703, Start-Stop format)
- buffer slips and adjustments

G.821 Statistics

The error counts are transformed to CCITT G.821 parameters

- total time (seconds)
- unavailable time (seconds)
- errored seconds
- severely errored seconds
- degraded minutes

6.18.3 Interface Modules for VCM Data Interface Unit

6.18.3.1 General

The unframed data interface modules used in the VCM unit are:

- V24-DCE
- V24-DTE
- V24-PMP
- V35
- V36
- X21
- G703-64
- V35-IEC
- V36-IEC

The unit accesses the physical interfaces via the interface modules. The interface modules convert the CMOS level data, timing and control signals to balanced or unbalanced V.11, V.28, V.10, V.35 or G.703 according to the requirements for each interface type. The receiver circuits convert the incoming signal levels to CMOS level data, clock and control signals.

The IF module monitors the existence of the received signal level; if the signal is missing, a power-off signal indication is reported to the unit controller.

Interface signal coding (e.g. G.703 co- and contradirectional operation or synch/async converter) is performed in the base unit.

There is an additional 16-bit input buffer on the V24-DTE module. This buffer can be used if buffer in the base unit is not long enough (e.g. analog PMP circuit connected to VCM).

As an addition to the V24-DCE module, the V24-PMP module includes a V.13 simulated carrier tail eater circuit in 104 signal. The function of this circuit is to prevent V.13 simulated carrier pattern access to DTE when 109 signal is OFF. The tail eater circuit can be controlled by NMS and when the circuit is OFF, the V24-PMP module acts similarly as a V24-DCE module.

The G703-PDA module consists of G.703 codirectional interface, coder/decoder and of adaption logic for PDA 64 interface. This module can be used when the circuit goes through both DXX system and PDA 64 system.

Available Interface Modules

Type	Name	Interface type	Buffer
V35	V.35 interface module	DCE	No
V36	V.36 interface module for bit rates up to 2 Mbit/s	DCE	No
V24-DCE	V.24/V.28 interface module for bit rates up to 64 kbit/s	DCE	No
V24-DTE	V.24/V.28 interface module for bit rates up to 64 kbit/s	DTE	16 bit
V24-PMP	V.24/V.28 point to multipoint master interface module	DCE	72 bit
X21	X.21 interface module for bit rates up to 2 Mbit/s	DCE/DTE	No
V35-IEC	V.35 IEC-530 interface module	DCE	No
V36-IEC	V.36 IEC-530 interface module	DCE	No
G703-PDA	Special G.703 64kbit/s interface module for PDA 64 system		
G703-64	G.703 64 kbit/s interface module for co- or contradirectional operation		

Interface to the Back Plane of the Subrack

The unit accesses the back plane of the DXX subrack through two euro connectors. The back plane supplies battery voltage to the power supply module, access to the control bus of the subrack and access to the 64 Mbit/s data cross-connect bus (X-bus). The X-bus interface uses the lower rear connector.

6.18.4 Fault Conditions

6.18.4.1 Signals and Directions of Fault Conditions

VCM holds four identical interface blocks numbered 1 and 4. The common parts are named block 0. The signals and directions are identified as follows:

Reference Point	Signal Description
UI1	Input signal at the receive part of the user interface
UI2	Output signal at the transmit part of the user interface
C1	XB output signal towards the X-bus interface
C2	XB input signal from the X-bus interface, net side signal

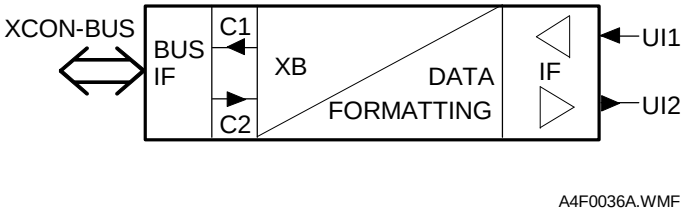


Fig. 174: Naming of Signal Reference Points

The following acronyms will be used in tables below:

PMA= Prompt Maintenance Alarm
DMA= Deferred Maintenance Alarm
MEI= Maintenance Event Information
S= Service Affecting Fault
R= Red alarm LED
Y= Yellow alarm LED
AIS= Signal substituted by AIS
RAI= Remote alarm indication (bit X in V.110, X.30 or frame)

Common Parts (Block 0)

Faults in Common Parts (Block 0)

Power supply

Fault Condition	Status	LED	UI2	C1
Power supply				
+5 V,+12 V,-10 V	PMA	R	-	-
+5 V back plane voltage	PMA	R	-	-

Memory faults

Fault Condition	Status	LED	UI2	C1
RAM, EPROM fault	PMA, S	R	-	-
FLASH fault	PMA, S	R	-	-

Check sum error in

Fault Condition	Status	LED	UI2	C1
- FLASH memory	PMA, S	R	-	-
- downloaded SW	PMA, S	R	-	-
Incompatible SW revisions	PMA, S	R	-	-
RL program error	PMA, S	R	-	-

Operating status faults

Fault Condition	Status	LED	UI2	C1
Unit reset	PMA, S	R	OFF	OFF
Unit unregistered	PMA, S	R	-	OFF
Setup parameter error	PMA, S	R	-	-

X-bus fault

Fault Condition	Status	LED	UI2	C1
Timing fault	PMA, S	R	AIS	AIS
No interface (IA) activity	PMA, S	R	AIS	AIS
Fault masking	MEI, -	Y	-	-

Interface Blocks (Block 1-4)

General IF Faults (Block 1-4)

Fault Condition	Status	LED	UI2	C1
Missing or wrong IF module	PMA, S	R	-	OFF/-
Power-OFF on input	MEI, -	Y	-	AIS
ASIC error	PMA, S	R	OFF	OFF

IF Signal Faults (Block 1-4)

Fault Condition	Status	LED	UI2	C1	Note
Input signal faults (UI1)					
Loss of input signal	PMA, S	R	-	AIS	

IF Signal Faults (Block 1-4)

Fault Condition	Status	LED	UI2	C1	Note
Signal 105 OFF	MEI, -	Y	-	AIS	Used when 105 should be continuously on
Timing errors					
Input signal (UI1) buffer slip	DMA	R	-	AIS	
Output signal (UI2) buffer slip	DMA	R	AIS	-	

Net Side Signal Faults (Block 1-4)

Fault Condition	Status	LED	UI2	C1	Note
Input signal from net side (C2)					
AIS from net side	MEI, S	Y	AIS	-	V.110, X.30 or framing in use
Loss of frame alignment	PMA, S	R	AIS	RAI	V.110, X.30 or framing in use
Loss of multiframe alignment	PMA, S	R	AIS	RAI	Used at bit rates $\leq$ 2.4 kbits.
Far end alarm (RAI) received	MEI, S	Y	-	-	V.110, X.30 or framing in use

Performance Conditions (Block 1-4)

Fault Condition	Status	LED	UI2	C1	Note
Performance conditions					
G.821 unavailable state	PMA, S	-	-	-	Available when end-to-end CRC monitoring is activated
G.821 data for last 15 minutes	DMA, S	-	-	-	Available when end-to-end CRC monitoring is activated
CRC errors detected	DMA	R	-	-	Available when end-to-end CRC monitoring is activated
Frame alignment signal error	PMA	Y	-	-	V.110, X.30 or framing in use

Test Loop Activation (Block 1-4)

Fault Condition	Status	LED	UI2	C1
Manager activated loops				
- interface loop	MEI, S	Y	AIS	-
- line, local loop	MEI, S	Y	-	AIS
User activated loop	MEI, S	Y	-	-

6.18.5 Front panel of VCM-10T Unit with V35 Interface Module

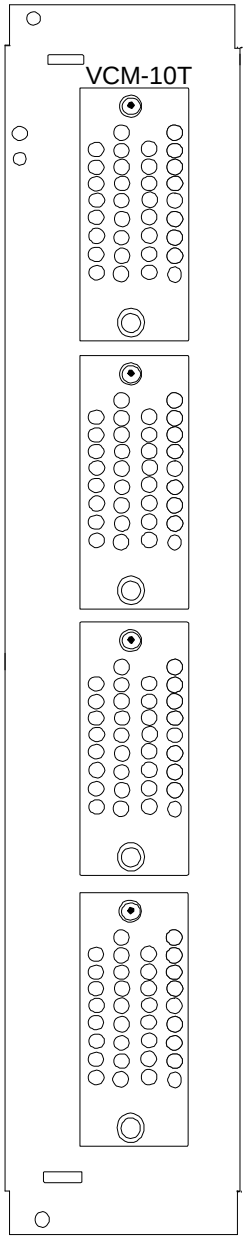


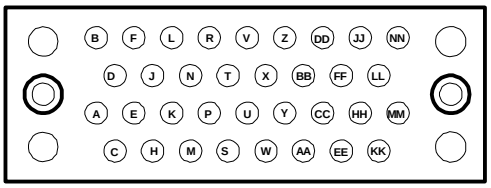
Fig. 175: Front panel of VCM-10T Unit with V35 Interface Module

34-pin female connector (ISO 2593)

Pin Number	ITU-T V.35 circuit no.	Input/Output	Signal	Signal Level
A	---		Cable shield	
P	103A	input	Transmitted data	V.35
S	103B	input	Transmitted data	V.35
Y	114A	output	Transmitted data timing from VCM	V.35

34-pin female connector (ISO 2593)

Pin Number	ITU-T V.35 circuit no.	Input/Output	Signal	Signal Level
AA	114B	output	Transmitted data timing from VCM	V.35
R	104A	output	Received data	V.35
T	104B	output	Received data	V.35
C	105	input	Request to send	V.28
V	115A	output	Received data timing from VCM	V.35
X	115B	output	Received data timing from VCM	V.35
D	106	output	Ready for sending	V.28
L	141	input	Local loopback	V.28
E	107	output	Data set ready	V.28
H	108	input	Data terminal ready	V.28
F	109	output	Signal detector	V.28
N	140	input	Remote loopback	V.28
U	113A	input	Transmitted data timing from terminal equipment	V.35
W	113B	input	Test indicator	V.28
NN	142	output	Test indicator	V.28
B	102		Signal ground	V.28



A1C0006A.WMF

Fig. 176: ISO 5293 compatible 34-pin female connector

6.18.6 Front Panel of VCM-10T with V36 Interface Module

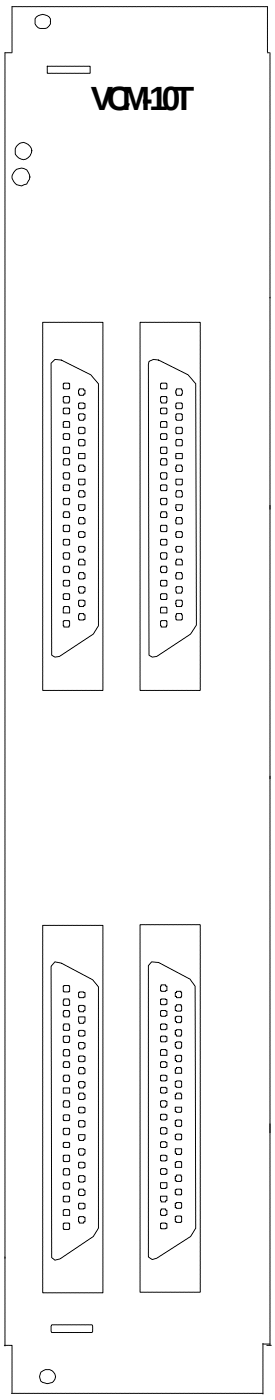


Fig. 177: Front Panel of VCM-10T with V36 Interface Module

D-type 37-pin female connector (ISO 4902)

Pin Number	ITU-T V.36 circuit no.	Input/Output	Signal	Signal Level
1	---		Cable shield	
2	103A	input	Transmitted data	V.11
22	103B	input	Transmitted data	V.11
5	114A	output	Transmitted data timing from VCM	V.11
23	114B	output	Transmitted data timing from VCM	V.11
6	104A	output	Received data	V.11
24	104B	output	Received data	V.11
7	105A	input	Request to send	V.11
25	105B	input	Request to send	V.11
8	115A	output	Received data timing from VCM	V.11
26	115B	output	Received data timing from VCM	V.11
9	106A	output	Ready for sending	V.11
27	106B	output	Ready for sending	V.11
10	141	input	Local loopback	V.28
11	107A	output	Data set ready	V.11
29	107B	output	Data set ready	V.11
12	108A	input	Data terminal ready	V.11
30	108B	input	Data terminal ready	V.11
13	109A	output	Signal detector	V.11
31	109B	output	Signal detector	V.11
14	140	input	Remote loopback	V.28
17	113A	input	Transmitted data timing from terminal equipment	V.11
35	113B	input	Transmitted data timing from terminal equipment	V.11
18	142	output	Test indicator	V.28
19	102		Signal ground	
20	102		Signal ground	

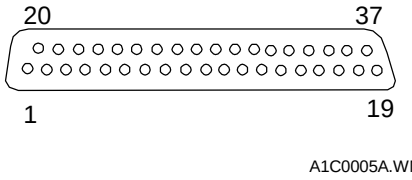


Fig. 178: D-type 37-pin female connector

6.18.7 Cabling for VCM-10T with V36

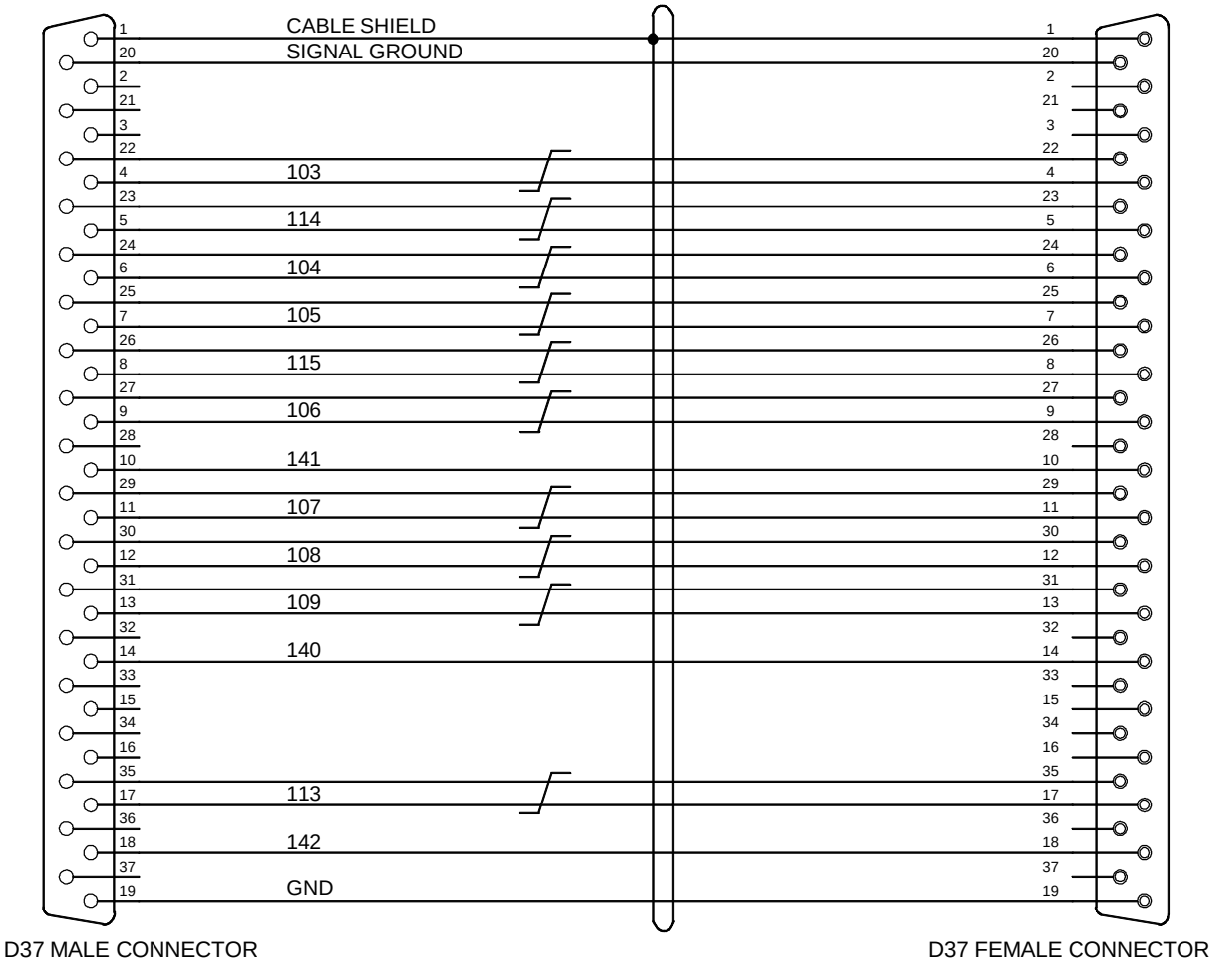


Fig. 179: V36 DCE/DTE Cabling

6.18.8 Front panel of VCM-5T with V24-DCE, V24-DTE, V24-PMP Interface Modules

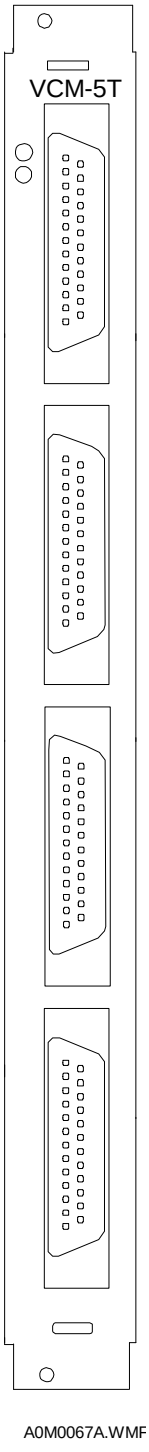


Fig. 180: Front Panel of VCM-5T

D-type 25-pin female connector (V.24/V.28 Interface Module V24-DCE)

Pin Number	ITU-T V.24 circuit no.	Input/Output	Signal
1	---		Cable shield
7	102		Signal ground
2	103	input	Transmitted data
3	104	output	Received data
4	105	input	Request to send
5	106	output	Ready for sending
6	107	output	Data set ready
8	109	output	Signal detector
20	108	input	Data terminal ready
24	113	input	Received data timing from terminal equipment
15	114	output	Received data timing from VCM
17	115	output	Received data timing from VCM
21	140	input	Remote loopback
18	141	input	Local loopback
25	142	output	Test indicator
9	---	output	+ 10 output from 321R
10	---	output	- 10 output from 321R
11-14			No connection
16, 19			No connection
22, 23			No connection

D-type 25-pin female connector (V.24/V.28 Interface Module V24-DTE)

Pin Number	ITU-T V.24 circuit no.	Input/Output	Signal
1	---		Cable shield
7	102		Signal ground
2	103	output	Transmitted data
3	104	input	Received data
4	105	output	Request to send
5	106	input	Ready for sending
6	107	input	Data set ready
8	109	input	Signal detector
20	108	output	Data terminla ready
24	113	output	Transmitted data timing from VCM
15	114	input	Transmitted data timing from DCE
17	115	input	Received data timing from DCE
21	140	output	Remote loopback
18	141	output	Local loopback
25	142	input	Test indicator

D-type 25-pin female connector (V.24/V.28 Interface Module V24-DTE)

Pin Number	ITU-T V.24 circuit no.	Input/Output	Signal
9	---	output	+ 10 output from 321R
10	---	output	- 10 output from 321R
11-14			No connection
16, 19			No connection
22, 23			No connection

D-type 25-pin female connector (V.24/V.28 Interface Module V24-PMP)

Pin Number	ITU-T V.24 circuit no.	Input/Output	Signal
1	---		Cable shield
7	102		Signal ground
2	103	input	Transmitted data
3	104	output	Received data
4	105	input	Request to send
5	106	output	Ready for sending
6	107	output	Data set ready
8	109	output	Signal detector
20	108	input	Data terminal ready
24	113	input	Transmitted data timing from terminal equipment
15	114	output	Transmitted data timing from VCM
17	115	output	Received data timing from VCM
21	140	input	Remote loopback
18	141	input	Local loopback
25	142	output	Test indicator
9	---	output	+ 10 output from 321R
10	---	output	- 10 output from 321R
11-14			No connection
16, 19			No connection
22, 23			No connection

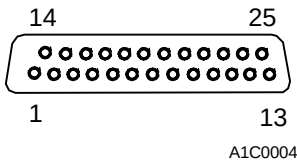


Fig. 181: D.type 25-pin female connector

6.18.9 Front Panel for VCM-5T with G703-64

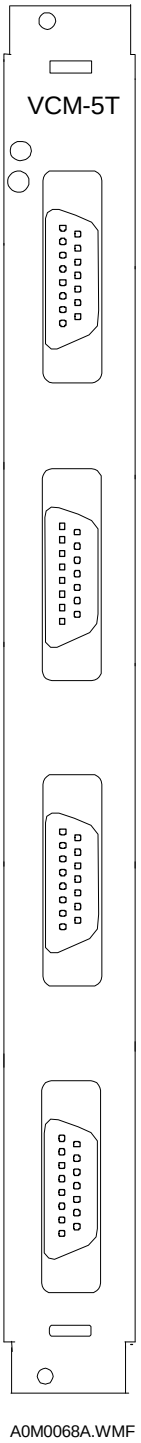
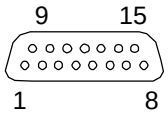


Fig. 182: Front Panel of VCM-5T with G703-64

D-type 15-pin female connector

Pin Number	Input/Output	Signal
1	output	Transmit data (A)
2	output	Transmit data (B)
3	input	Receive data (A)
4	input	Receive data (B)
5	output	Transmit data timing (A)
6	output	Transmit data timing (B)
7	output	Receive data timing (A)
8	output	Receive data timing (B)
9…15		GND



A1C0008A.WMF

Fig. 183: D-type 15-pin female connector

6.18.10 Technical Specifications

6.18.10.1 Power Requirements And Mechanical Data

DC Supply

Input voltage: -30…-60 V DC

Mechanical Dimensions

Width:

-VCM-5T-A: 25 mm (0.98")
-VCM-10T-A: 50 mm (1.97")

Depth: 160 mm (6.30")

Height: 244 mm (9.6")

6.18.10.2 DCE Interfaces

Timing Signals	
Transmit side output to DTE (114)	
Rate accuracy	better than ±100 ppm, locked to the node clock
Transmit side input from DTE (113)	
Maximum allowed jitter	± 0.4 UI (20 Hz…f/20 kHz); f = f_{data}
Receive side output to DTE (115)	
Maximum jitter	0.1 UI p-p
Loop-back to circuit 113	allowed
Interface Types	V.35 (ISO 2593), synch.
	V.36 (ISO 4902), synch.
	V.24/V.28 (ISO 2110), synch./async.
	X.21/V.24 (ISO 4903), synch.
V Series Interfaces	
Interface circuits	102,103, 104, 105, 106, 107, 108, 109, 113, 114, 115, 140, 141, 142
Circuit levels	V.10, V.11, V.28 and V.35
Simulated Carrier Function	V.13
Asynchronous Operation	
At bit rates ≥ 600 bit/s	V.14
Data bits	6, 7, 8 or 9
Rate accuracy	
- basic mode	+ 1,25/- 2,5 %
- extended mode	± 2,5 %
At bit rates < 600 bit/s	
- sampling rate	4.8 kHz
X.21 Interface	
Interface circuits	G, T, R, C, I, S, B/X
Circuit level	X.27 (V.11)

G.703 Interface

Nominal bit rate	64 kbit/s
Signals	64 kbit/s information
	64 kHz timing
	8 kHz octet timing
Maximum output jitter	± 0.05 UI
Contradirectional Interface	
Electrical interface	2 symmetrical pairs per direction
Attenuation	< 3 dB; @ 32 kHz
Signal coding	
- information	100 % AMI
- timing	50 % AMI, octet timing by AMI violation
Maximum allowed input jitter	±0.4 UI (10 Hz…3 kHz)
Codirectional Interface	
Electrical interface	1 symmetrical pair per direction
Attenuation	< 3 dB; @ 128 kHz
Signal coding	
- binary one	1100 block during a 64 kbit/s period
- binary zero	1010 block during a 64 kbit/s period
- octet timing	violation of polarity inversion of consequtive blocks
Maximum allowed input jitter	G.823 §3.1.1, 64 kbit/s
Electrical Characteristics	
Output pulse voltage	1 + 0.1 V; @ when terminated into 120 Ω
Pulse or space overshoot	< + 0.1 V; @ when terminated into 120 Ω
Input impedance	120 Ω
Input return loss	≥ 12 dB; @ 1.6…3.2 kHz ≥ 18 dB; @ 3.2…256 kHz ≥ 14 dB; @ 256…384 kHz
Longitudinal balance	≥ 50 dB; @ 1.6…128 kHz

6.19 VMM Framed Interface Unit

6.19.1 General

The VMM unit processes framed signals at n x 64 kbit/s (n = 1…32). The unit includes two independent transmission channels to carry data and also to provide an internal communication link of the DXX system. The transmission channel interfaces are independent of each other and they are V.11 level NRZ interfaces supporting data and clock signals in both transmission directions. The frame structure is proprietary frame using only 8 kbit/s for framing.

6.19.2 Operation of VMM Framed Interface Unit

6.19.2.1 Mechanical Design

The mechanical design of the VMM unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the subrack; however, the general recommendations for subrack equipping should be followed.

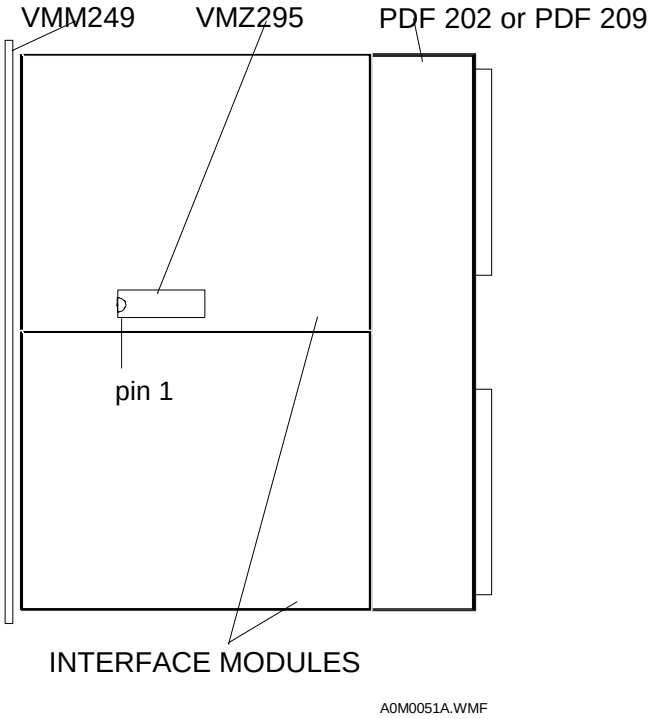


Fig. 184: VMM Unit Equipped with Modules

A minimum configuration of the VMM unit consists of a VMM 249 base unit, a unit power supply PDF 202 or PDF 209, program memory VMZ 295 and for both channels a VMM unit interface module. The interface modules are selected to suit the particular application in order to provide the physical interface to the transmission line. The two channels can have interface modules of a different type.

The unit front panel houses alarm LEDs. The front panel openings are suited for all available interface modules.

The unit is connected to the DXX subrack X-bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal subrack control bus and for the data transmission processing.

Functional Structure

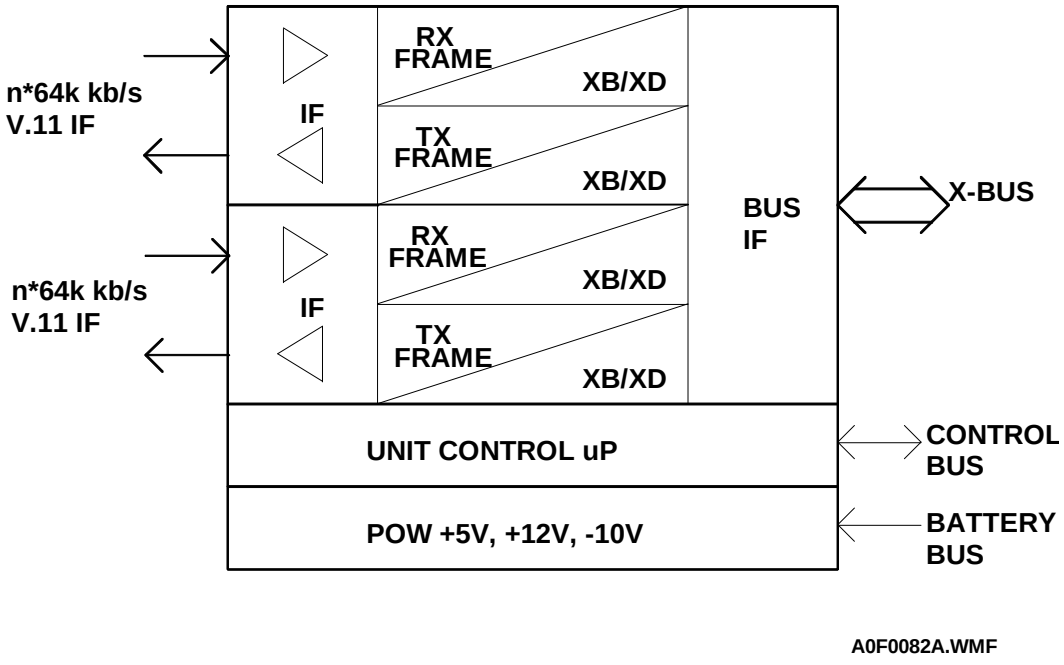


Fig. 185: Functional Structure of the VMM Unit

The main functional blocks of the VMM unit include the power supply, the processor and its peripheral circuits, line interfaces for both channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for both channels.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to the control and monitoring is transmitted on an internal control bus of the subrack. Through this control bus the unit can communicate with other units in the subrack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analog line signals to/from signals suited for the unit's digital circuits. In the transmitting direction data pulses are created in a form suitable for transmitting in the required format. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic. The line interfaces are realized as interface modules so that a unit can have two interface modules of different types at the same time. The available data transmission speeds of the unit can be programmed.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx-frame and Rx-frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC checksum, and by generating the HDLC channel at a required position within the frame with the aid of the processor. In the receiving direction the Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the Rx-frame block can extract the data

transmission time slots, check the CRC checksum, and recover and supply the HDLC channel to the processor. The frame structure and the use of the special bits in the frame depend on the transmission speed.

The transmit buffers of the channels are used to store data received from the cross-connect via the X-bus, so that there is always a time slot available for transmit by the Tx-frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that required time slots are always available to the cross-connect unit. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation it is desired to have slips occurring as seldom as possible.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the subrack slot, or when it is removed from the subrack, and also if the unit fails.

Block Diagram

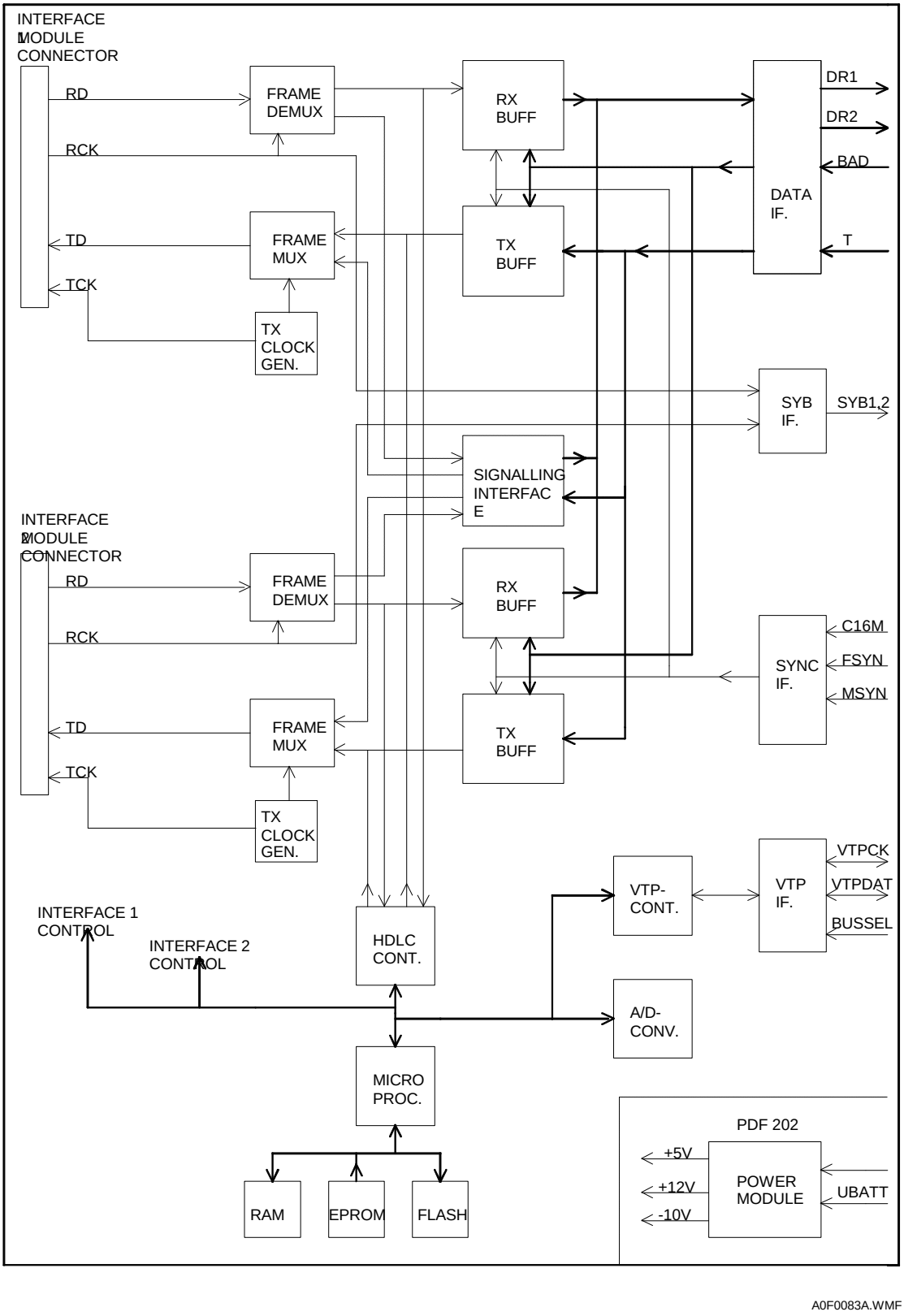


Fig. 186: Functional Block Diagram of the VMM Unit

6.19.2.2 Power Supply

A unit receives its operating voltage from the power supply module PDF 202 or PDF 209. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in the place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage, which during startup conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset-circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D-converter. An alarm is generated if a voltage exceeds its limits.

6.19.2.3 Unit Controller

The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM-memory identified as VMZ 295. Part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in case of power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parametrization. The RAM-memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC-links and the frame control bus.

6.19.2.4 Control Bus

The unit communicates with other units in the subrack via the subrack control bus. Each unit position in the subrack has an individual address which is registered by the unit when it is inserted into the subrack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

6.19.2.5 A/D-Converter

The unit includes a multichannel analogue to digital converter (A/D) which monitors the operating voltages and also the control voltage from the interface module connectors. The control voltage is for instance a voltage received from a baseband module which controls the baseband line power-off situation.

6.19.2.6 X-Bus Interface

The cross-connect unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack which is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface units by placing a channel address on the X-bus that activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. The receiving data bus DR1 is secured with the data bus DR2. The cross-connect unit decides with the aid of the BUS test which bus to use and this information is supplied to other units via the control bus. The VMM unit receives from the cross-connect unit the time slot address which directs the bus data transmission to one selected time slot at a time.

The main signals of the X-bus interface are:

Signal	Signal description
C16M	Internal timing signal for the node
FSYN, MSYN	Frame and multiframe alignment signals
DR10 - 17	8-bit wide data bus VMM towards SXU
DR20 - 27	8-bit wide duplicate of the data bus VMM towards SXU
T0 - 7	8-bit wide data bus SXU towards VMM
BAD0 - 7	8-bit wide addressing bus SXU to VMM

The X-bus interface transmits and receives one byte of data each time an interface of the unit is addressed by the BAD0 - 7 bus. For each 125-us bus frame, the interface can be addressed once or several times depending on the XB capacity (N x 64 kbit/s). A channel below the bit rate 64 kbit/s is transferred between VMM and the cross-connection unit SXU using one byte per frame (64 kbit/s) and utilizing only one or several of the 8 data bits, 8 kbit/s each, of the byte. SXU maps only the used bits to the connection.

Bus functions are monitored also by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the alarm 'IA Activity Missing', if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing, the unit will activate the alarm 'Bus Sync Missing'. The 'Bus Sync Missing' alarm inhibits the missing channel address alarm.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern which the receiver will search for in the received serial data flow. When the receiver finds the frame alignment signal it is synchronized and therefore able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a structure defined for each transmission speed. In the DXX system the bus frame repetition frequency is always 8 kHz. Several consecutive bus frames are combined into a bus multiframe. For instance signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz. The proprietary framing of the VMM unit is based on the DXX system frame/multiframe timing so that the frame frequency is 500 Hz and framing bit's frequency is 8 kHz. So the proprietary trunk frame length is equal to one DXX-bus multiframe and to a 16 DXX-bus frame.

A more reliable receiver synchronization is achieved when a CRC checksum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference between the results, the received data block contains one or more errors. The CRC can be made for a data block of one frame.

The CRC checksum is used to check the reliability of the synchronization by counting how many blocks containing errors are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called 'simulating frame synchronization word'.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC checksum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a two channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units in which the messages are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels is 4 kbit/s.

6.19.2.7 Buffers

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control the write and read operations so that they do not simultaneously address the same time slot. In the VMM unit the following method is used to avoid such conflict situations:

The transmit buffer length is two DXX-bus frames. The frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one bus frame or 125 μs.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the cross-connect unit via the X-bus requests data from the interface units it also specifies the time slot concerned. Usually the phase of the received frame does not coincide with the frame phase of the X-bus and on the other hand the receiver writes time slot data into the Rx-buffer clocked by the received frame. Therefore the Rx-buffer has to control that the read and write operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the VMM unit the centring is made by changing the read address, the change being always one bus frame or a multiple of a bus frame. The centring causes a certain number of frames to be lost or retransmitted; the number is proportional to the distance which the read address is moved.

Centring is required when the equipment is powered up, when a received signal contains disturbances or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

The buffers have one operating mode:

Rx Buffer	Rx delay	Tx length	Tx delay
16 Bus Fr=1 trunk Fr	3…13 Bus Fr	2 Bus Fr	1 Bus Fr

16 Fr Rx Buffer

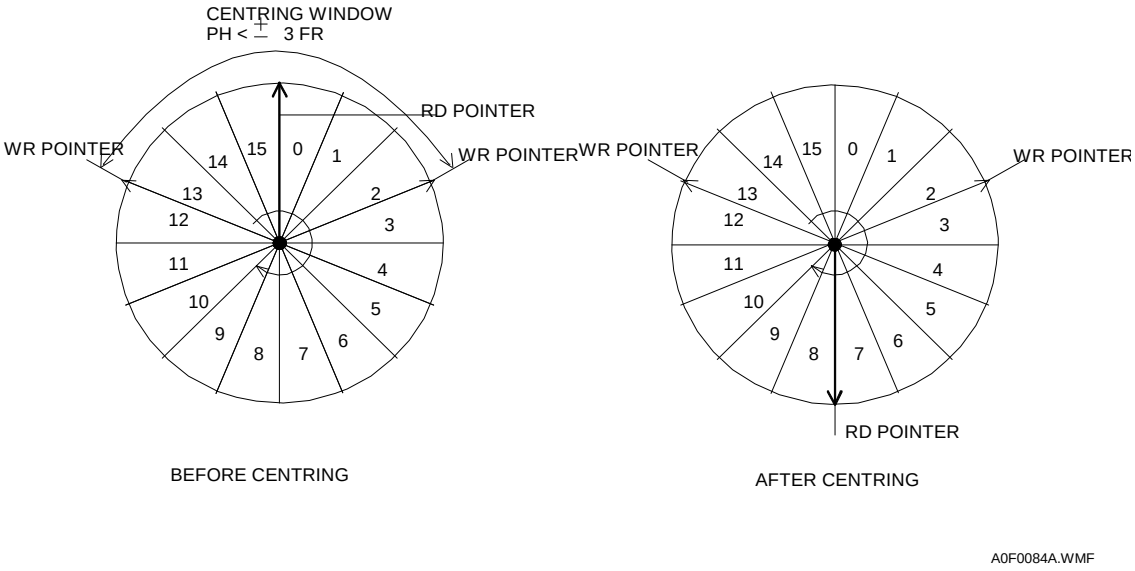


Fig. 187: Centring in an Rx-Buffer of 16 Frames

In an Rx-buffer of sixteen bus frames (equal to one low overhead trunk frame) the allowed distance between read and write addresses is three bus frames. If a shorter distance is detected by the check, the read address is moved to a new position half trunk frame farther away. In this case centring means that half of the trunk frame is either lost or repeated once. The sixteen bus frame buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure or a n x 64 kbit/s framing structure is used.

In a plesiochronous system the interval between centring situations is:

at n x 64 kbit/s 5.33 x n x 8/df

where df is the frequency difference between the signal received from the line and the receiving frequency generated by the X-bus clock frequency.

A buffer with a length of 16 DXX-bus frames is also used for the 'Split Trunk' operation.

Split Trunk Lines

A split trunk line can be used to combine several parallel n x 64 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the n x 64 kbit/s is connected through physically separated cables. One of the interfaces will function as a master and the others as slaves. The split components can have different bit rates.

Theoretically the maximum delay allowed between lines in a split trunk line is 0.1875 trunk frame: due to the centring the master read address occurs when the write address is in the area 13…3. However, due to technical reasons the maximum delay is 350 μs.

The interfaces are synchronized to each other by their frame structure. In the transmitting direction the interface transmit buffers and Tx-frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same DXX-bus multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will centre their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the SXU-unit of the receiving node.

Each line of a split trunk line will handle its own signalling data.

6.19.2.8 Loops in VMM

The NMS is able to control several loops in the VMM unit. Loops are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop timeout control which will turn off a loop when the user-defined time has come to an end.

Interface Loop

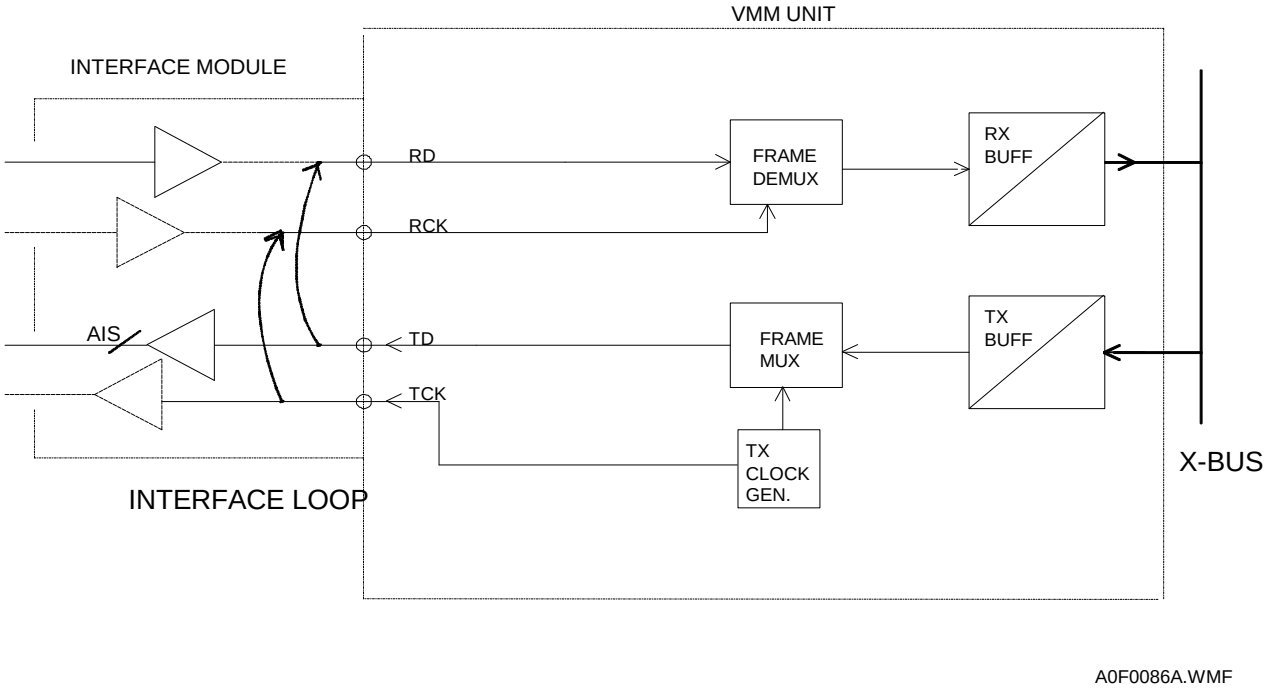


Fig. 188: Interface Loop

An interface loop is created in the interface module. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm led is switched on.

The type of the module determines the point where the loop is created in the module. In most cases, due to technical reasons, the loop is not made using a signal with line level. The loop will however always test the interface module control bus and connectors and a part of the module logic. Of course the line coder and decoder as well as the frame multiplexer and demultiplexer are also tested in the loop. There should be no other faults in the unit's fault list when the loop is created.

Line Loop

In the line loop the Rx-data received by the interface module is looped back to the interface transmitter. The yellow alarm LED is switched on.

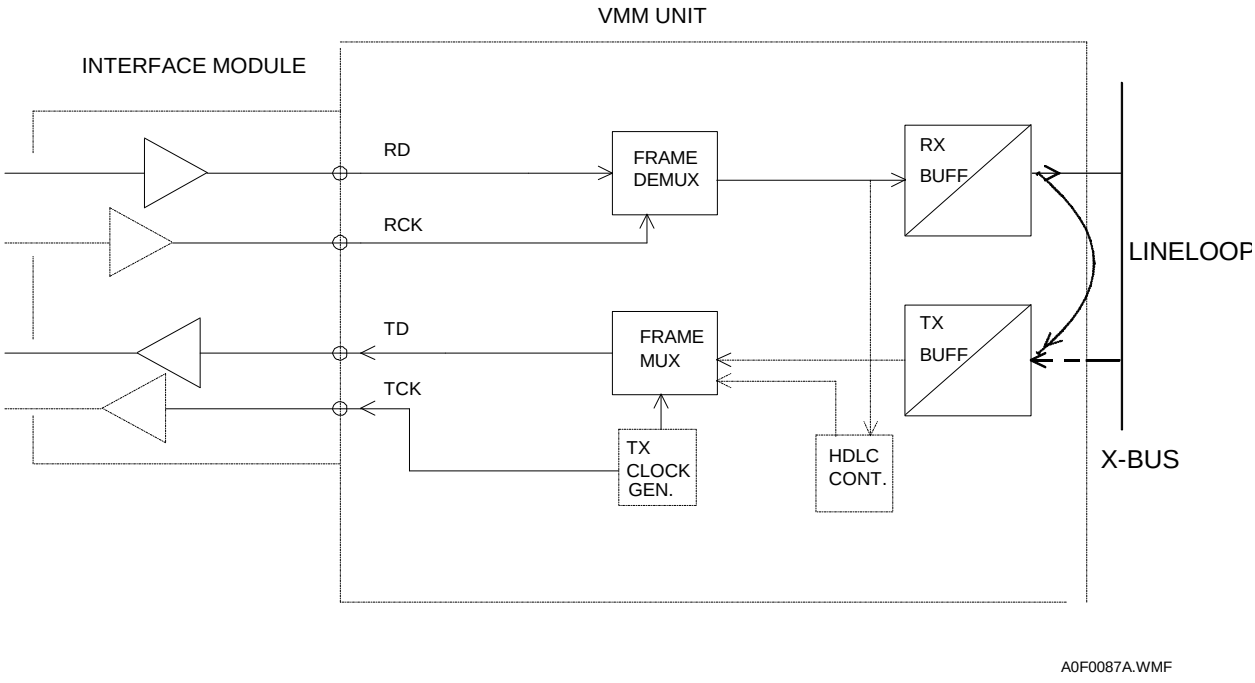


Fig. 189: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the line loop test. the HDLC-controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC-channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made the yellow LED of the unit controlling the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

6.19.2.9 Performance

The VMM unit supports trunk performance monitoring separately for each interface. The performance signal quality monitoring is according to G.821. Performance data is collected in three ways:

The unit collects the G.821 data for 24-hour periods starting at 00:00 hours. The 24-hour data is available during the next day for automatic transfer to the DXX performance database.

If activated, the unit also calculates performance data for 15-minutes time periods. If the signal impairments during a 15-minute period exceeds a selected limit, the data is transferred to the performance database.

A third set of performance counters is available for the network operator. The operator can start and terminate error monitoring at any time and gain performance data for periods that can be selected from seconds to days or months. The results are shown as error counts and as G.821 parameters.

Error Counters

The VMM unit is able to count, using SW and HW counters:

— number of frame losses (frame from the network side, C2)
— number of frame word errors (frame from the network side, C2)
— number of CRC block errors
— buffer slips and adjustments

G.821 Statistics

The error counts are transformed into CCITT G.821 parameters (see Relevant Recommendations).

— total time (seconds)
— unavailable time (seconds)
— errored seconds
— severely errored seconds
— degraded minutes

6.19.3 Module Interfaces X21-G704-S, V35-G704-BS for VMM Framed Interface Unit

6.19.3.1 General

A unit is connected to a transmission line through interface modules. The interface modules contain the analog components required for the interface and also the analog components needed to generate input and output clocks. The signals between the unit and the interface module are digital signals which are converted to the transmission line level in the module. Each module type supports defined transmission speeds which can be selected with the service computer. The codes and the available transmission speeds are described in the functional description of the respective units.

The processor bus is connected to both interface module connectors. Through this bus it is possible to detect the module type and to read data regarding the module status, e.g. regarding a missing incoming signal. Parameters which define the module functions, e.g. the transmission speed and possible looping commands, can be selected through the bus.

In the receiving direction the interface module monitors the level of the received signal; if it is too low or if it is completely missing, the module sets an AIS signal to the unit and at the same time it activates a missing signal alarm via the processor bus.

The receiving direction clock (receive clock) in the V-series modules is received from circuit 113 of the line. The alarm of a missing signal with V-series modules is based on detecting the incoming clock signal.

The received clock from both channels is connected to the SYB interface, where the processor can select a desired clock for either SYB-bus to be used as the frame synchronization signal. The clock to the SYB-bus is disconnected if there is a received signal failure.

The unit generates the frame structure for the data in the transmitting direction. NRZ data for interfaces is connected to the interface module, where it is coded and transformed into a line level signal.

The transmitting direction clock is phase-locked to the C16M frame clock received from the X-bus.

The transmitting direction clock for V35-G704 and V36-G704 modules is generated by dividing the C16M clock with suitable divider. This clock is used as the transmit clock of the module in circuit 115.

Because of the dividing process there may be some jitter in the clock in this case. If the C16M clock is missing no signal or clock is sent from the module.

6.19.4 Faults and Actions in VMM Framed Interface Unit

6.19.4.1 Fault Conditions

VMM holds 2 identical interface blocks numbered 1 and 2. The common parts are named block 0. The signals and directions are identified as follows:

The following acronyms will be used in the tables below:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Affecting Fault
R = Red alarm LED
Y = Yellow alarm LED
AIS = Signal substituted by AIS

Reference point	Signal description
UI1	Input signal at the receive part of the trunk interface
UI2	Output signal at the transmit part of the trunk interface
C1	XB output signal towards the X-bus Interface
C2	XB input signal from the X-bus interface, net signal

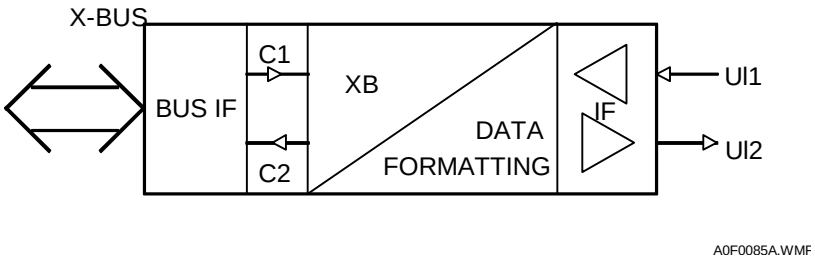


Fig. 190: Naming of Signal Reference Points

Faults In Common Parts (Block 0)

Fault condition	Status	LED	UI2	C1
Power supply				
+5V,+12V,-10V	PMA	R	-	-
+5V back plane voltage	PMA	R	-	-
Memory faults				
RAM, EPROM fault	PMA, S	R	-	-
FLASH fault	PMA, S	R	-	-
Check sum error				
- in FLASH memory	PMA, S	R	-	-
- in downloaded SW	PMA, S	R	-	-
Incompatible SW revisions	PMA, S	R	-	-
Operating status faults				
Unit reset	PMA, S	R	OFF	OFF
Unit unregistered	PMA, S	R	-	OFF
Setup parameter error	PMA, S	R	-	-
X-bus fault				
Timing fault	PMA, S	R	AIS	AIS
No interface (IA) activity	PMA, S	R	AIS	AIS
Fault masking	MEI, -	Y	-	-

General IF Faults (Block 1,2)

Fault condition	Status	LED	UI2	C1
Missing or wrong IF module	PMA, S	R	-	OFF/-
ASIC error	PMA, S	R	OFF	OFF

IF Signal Faults (Block 1,2)

Fault condition	Status	LED	UI2	C1	Note
Input signal faults (UI1)					
- Loss of input signal	PMA, S	R	-	AIS	
Timing errors					
- Input signal (UI1) buffer slip	DMA	R	-	-	
- Output signal (UI2) buffer slip	DMA	R	-	-	

Signal Faults on the Network Side (C2) (Block 1,2)

Fault condition	Status	LED	UI2	C1	Note
AIS from net side	MEI, S	Y	AIS	-	
Loss of frame alignment	PMA, S	R	AIS	RAI	

Performance Conditions (Block 1,2)

Fault condition	Status	LED	UI2	C1	Note
G.821 unavailable state	PMA, S	-	-	-	
G.821 data for last 15 min	DMA	-	-	-	
CRC errors detected	DMA	R	-	-	
Frame alignment signal error	PMA	Y	-	-	

Test Loop Indications (Block 1,2)

Loop condition	Status	LED	UI2	C1
Operator activated loops				
- interface loop	MEI, S	Y	AIS	-
- line loop	MEI. S	Y	-	AIS

6.19.5 Technical Specifications for VMM Framed Interface Unit

Trunk Line Interfaces

Line rate (kbit/s): n x 64 kbit/s (N=1…32)

Input to DXX

rate accuracy mesochronous operation	clock frequency locked to DXX or better than $\pm 10^{-9}$

Output from DXX

rate accuracy mesochronous operation	clock derived from the DXX node

6.19.5.1 Power Requirements and Mechanical Data

DC Supply

input voltage: -30…-60 Vdc

Mechanical Dimensions

width: 25 mm (0.98 in.)

depth: 160 mm (6.30 in.)

height: 244 mm (9.6 in)